

Xpedition Standard 2604 Update & Demo

이디앤씨 / 허소은 대리



Agenda

Xpedition Standard

Xpedition Standard – 5가지 주요 기술 요소

Xpedition Standard 2604 Update & Demo

Summary

Agenda

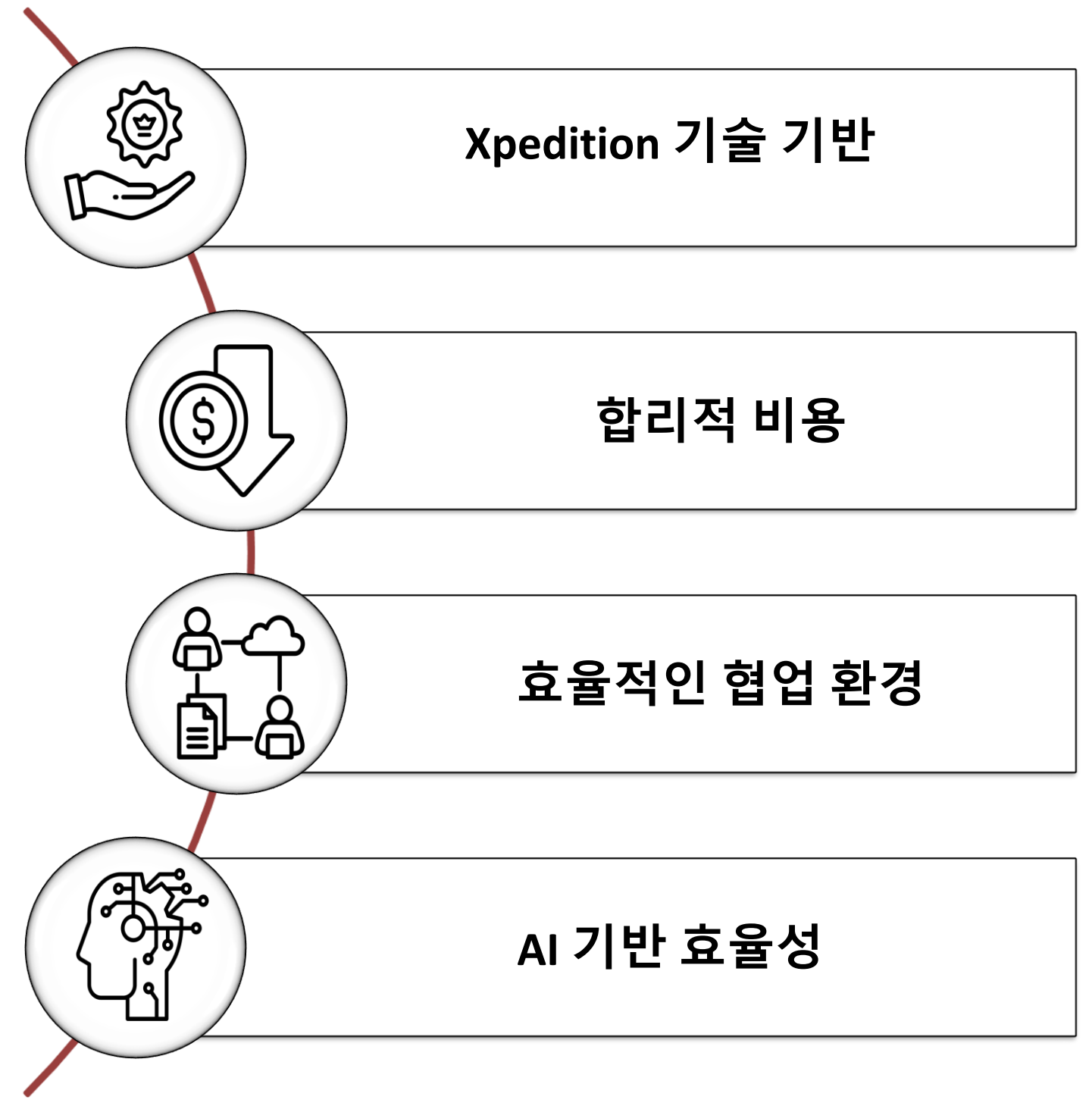
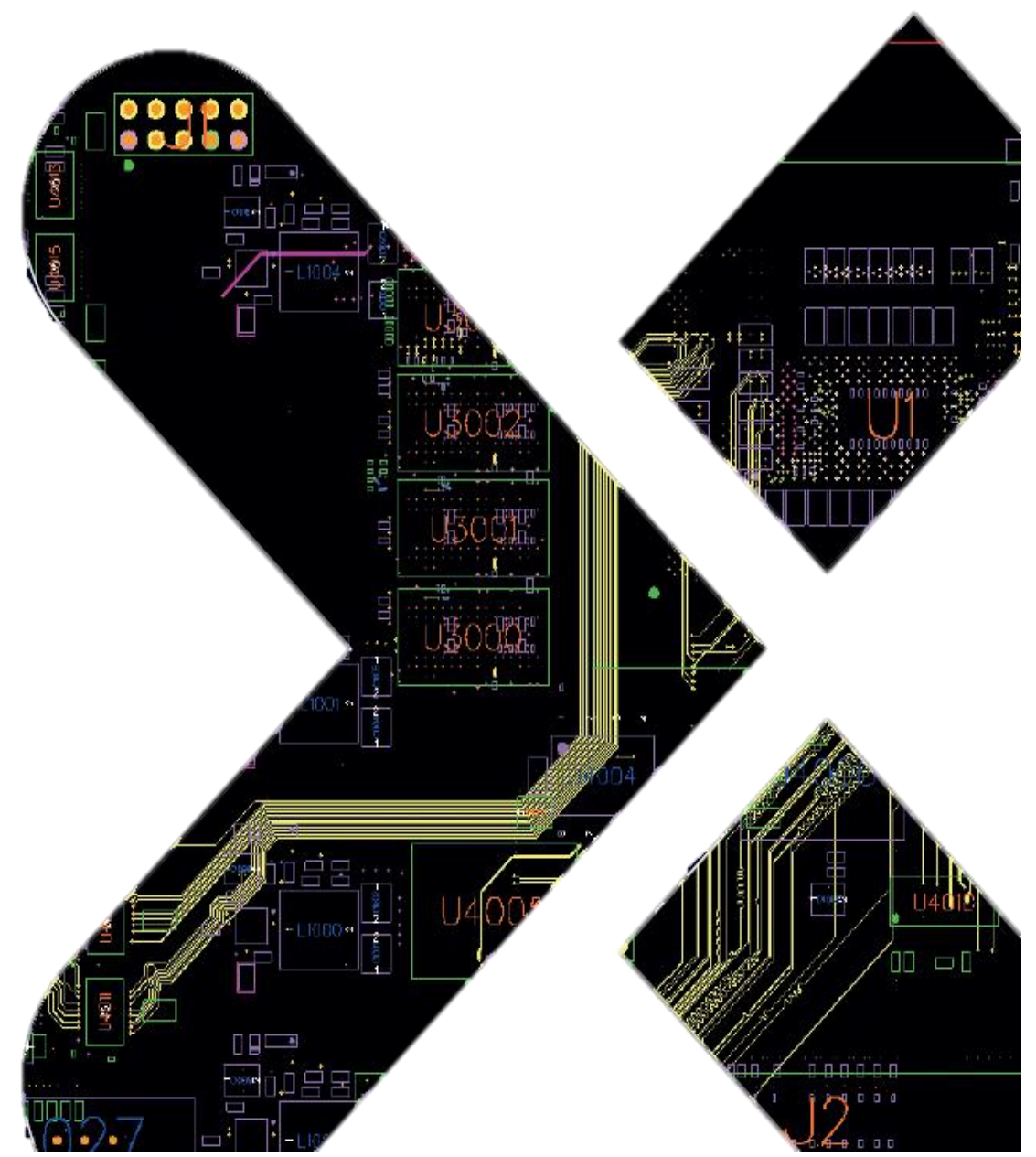
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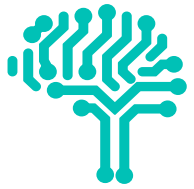
Summary

Xpedition Standard – 5가지 주요 기술 요소



Intuitive

Modern UX를 활용한 생산성 향상



AI-infused

설계 최적화 및 자동화



Cloud-connected

데스크톱 툴과 클라우드 연결



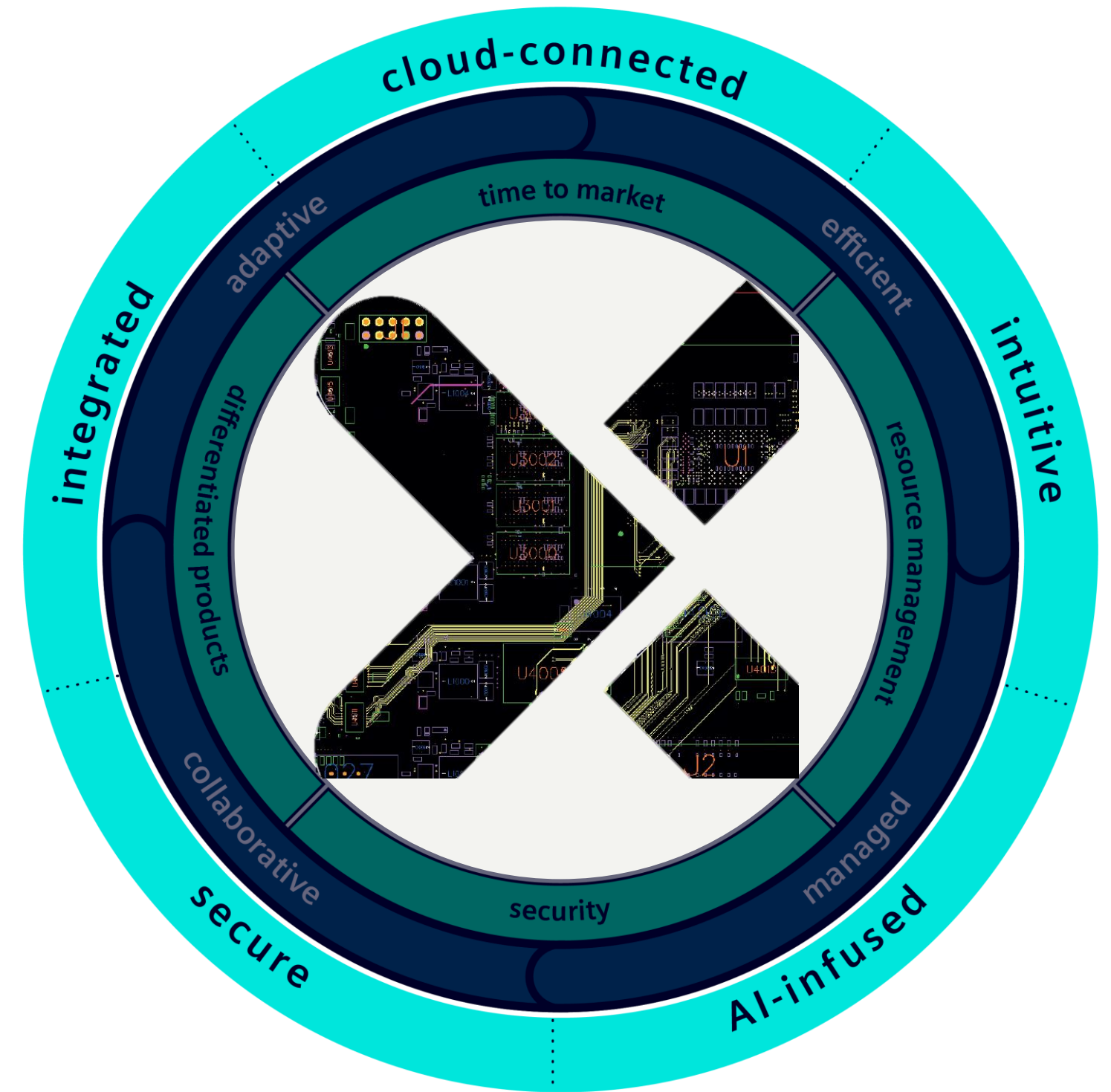
Integrated

PCB 설계 프로세스 통합



Secure

중요한 설계 IP 보호



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Summary

Named user licensing

SIEMENS

Products & services Solutions Industries op1 Industries op2

Siemens Xcelerator Admin Console

Administrators manage product subscriptions in Admin Console. You must have a Siemens account to log in.

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Strategy

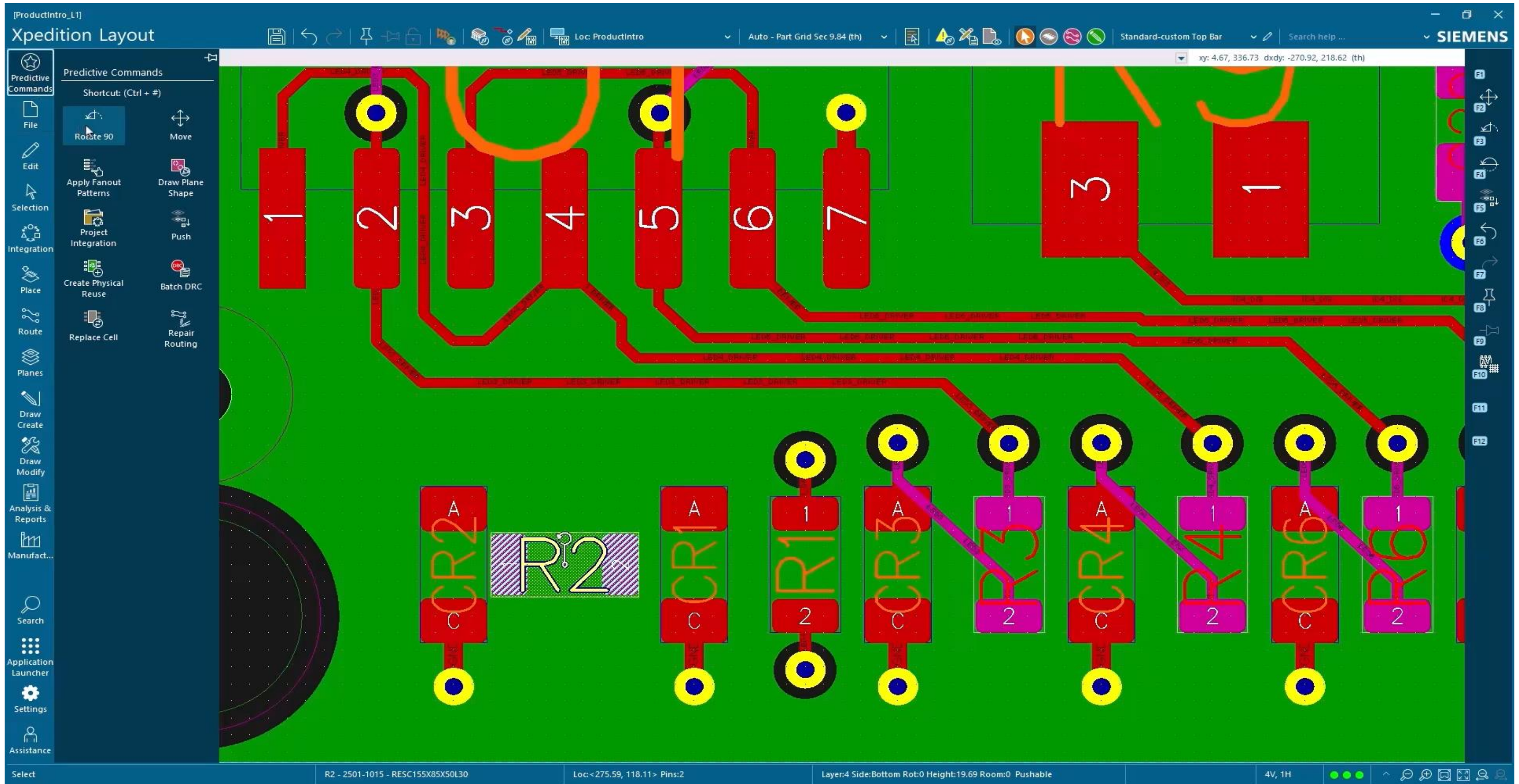
GET IN TOUCH
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Worldwide offices

CAREERS
Jobs & careers
Open roles

Token-based add-ons



Global search and AI command prediction



Product support copilot

The screenshot displays the Siemens Xpedition Layout software interface. The main workspace shows a complex PCB layout with various components, traces, and pads. A large orange 'IC2' label is visible in the center. The interface includes a top toolbar with navigation and editing tools, a left sidebar with predictive commands (File, Edit, Selection, Integration, Place, Route, Planes, Draw Create, Draw Modify, Analysis & Reports, Search, Application Launcher, Settings, Assistance), and a right sidebar with a Product Support Copilot chat window.

The Product Support Copilot chat window is titled "How do i configure stackup layers?" and provides the following instructions:

To configure stackup layers in Siemens EDA tools like Xpedition, follow these steps:

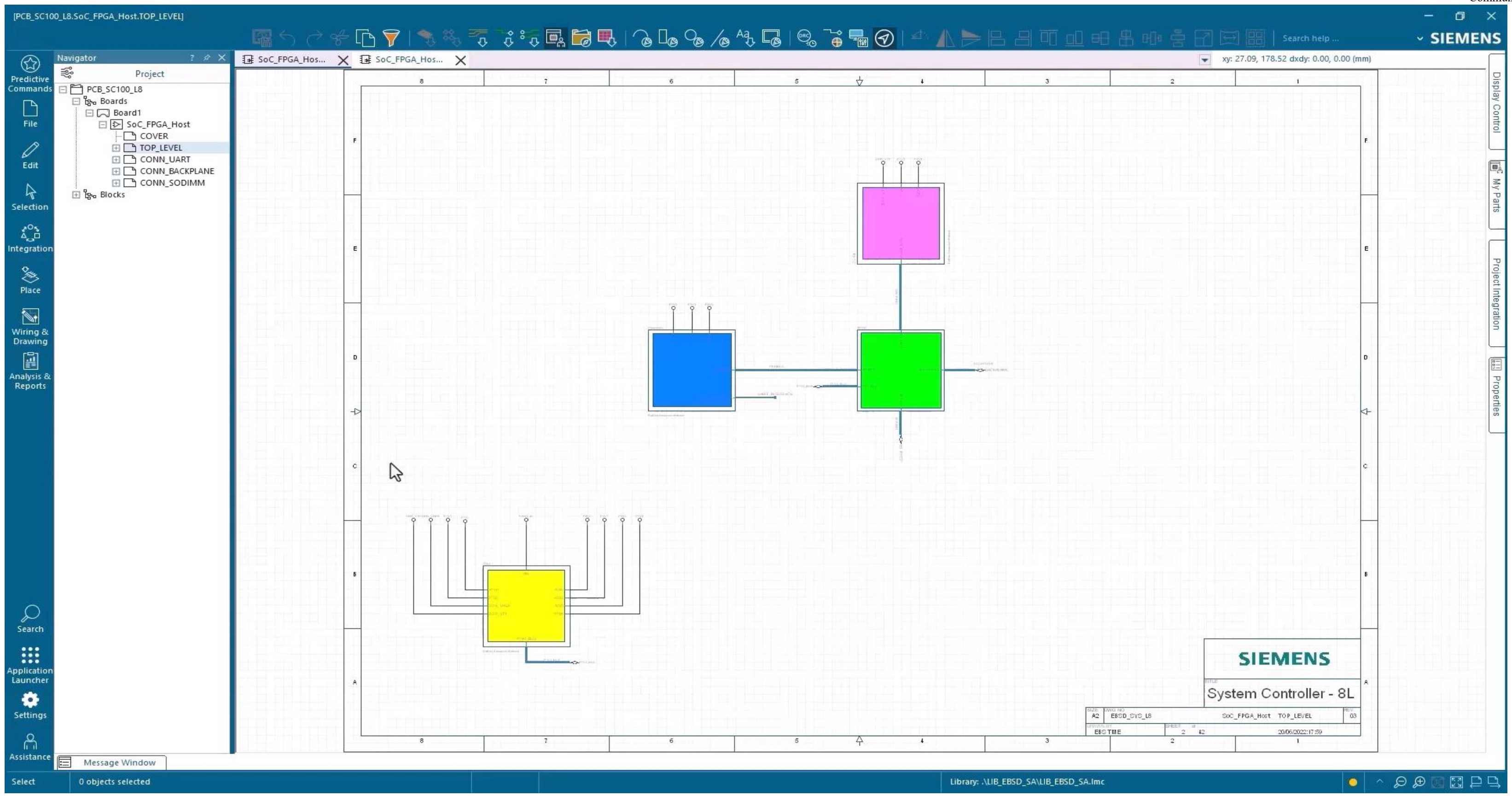
- 1. Access the Stackup Editor:**
 - On the Global bar, click Settings > Design category > General group > Stackup Editor.
- 2. Edit the Stackup:**
 - If you are working with a single board design:
 - Open the Stackup Manager by clicking Design Setup > Stackup group > Open Stackup Manager.
 - Select a stackup from the table and click Edit.
 - If you are working with a multiple-board design:
 - Enable multiple stackup support by clicking Design Setup > Stackup group > Enable Multiple Stackups.
 - Open the Stackup Manager and select the desired board from the list.
- 3. Add or Modify Layers:**
 - To add a new layer:
 - Right-click the spreadsheet row next to where you want to add the layer.
 - Select Insert Above or Insert Below and choose the layer type.
 - If you add a signal or plane layer, the software will automatically add a dielectric layer to separate it from other metal layers.
- 4. Define Layer Properties:**
 - For HyperLynx SI/PI users:
 - If the added layer does not have the correct properties, you can edit the default stackup properties. On the Global bar, click Settings > Stackup group, then update the metal and dielectric options as needed.
- 5. Special Considerations for Flex PCB Designs:**
 - If you are working on a flex PCB design:
 - Create a master stackup that includes all layers required for both rigid and flex portions of the design.
 - For each board outline, define the stackup layers by selecting either "All" (to include all master stackup layers) or "Custom" (to select specific layers for the sub-stackup).
- 6. Review and Save:**
 - Correct any warnings or errors displayed in the status line of the Stackup Editor to preserve the integrity of the stackup.
 - Save your changes once the stackup configuration is complete.

Was the generated information helpful?

How can I help you today?

This content is generated by an AI system. Content should not be relied upon as a substitute for professional advice.

Schematic capture



Component sourcing and research

The screenshot displays the Siemens Xpedition Designer interface. The main workspace shows a schematic diagram with components like resistors (R10, R11, R12), capacitors (C2, C7), and a discharge network (DISCH, Trig). The left sidebar contains a Project Navigator with a tree view of the design hierarchy. The right sidebar features the PartQuest component search tool, which is currently displaying search results for the part number 'NE555DR'.

PartQuest Search Results:

MPN	ECAD Data	Supply Chain
NE555DR Texas Instruments	Details	PDF
NE555DRG4 Texas Instruments	Details	PDF
NE555DRE4 Texas Instruments	Details	PDF
NE555DRG3 Texas Instruments	Details	PDF
NE555DR1G4 Texas Instruments	Request	Details

Project Explorer Table:

Part Number	Symbol	Part Name	Part Label	Cell	Value	Tolerance	Rating
<all>	<all>	<all>	<all>	<all>	<all>	<all>	<all>
Partition: Capacitors							
2101-1081				CAPC100X50X55L30	10nF		
2101-1100				CAPC160X80X87L35N	22uF		
2101-1008				CAPC160X80X87L35N	10nF		
2101-1113				CAPC100X50X55L30	47nF		

Found: 140

AI-assisted smart datasheet research

The screenshot displays a web browser window with the PartQuest Portal. The main content area shows a PDF document titled "USB3300 Hi-Speed USB Host, D..." with a "Read Only" status. The document text includes:

Hi-Speed USB Host, Device or OTG PHY with ULPI Low Pin Interface

Datasheet

In some cases, a Link may be software configured and not have control of its STP pin until after the PHY has started. In this case, the USB3300 has an internal pull-up on the STP input pad which will pull STP high while the Link's STP output is tri-stated. The STP pull-up resistor is enabled on POR and can be disabled by setting the *InterfaceProtectDisable* bit 7 of the Interface Control register.

The STP pull-up resistor will pull-up the Link's STP input high until the Link configures and drives STP high. Once the Link completes its start-up, STP can be synchronously driven low.

A Link design which drives STP high during POR can disable the pull-up resistor on STP by setting *InterfaceProtectDisable* bit to 1. A motivation for this is to reduce the suspend current. In Low Power Mode, STP is held low, which would draw current through the pull-up resistor on STP.

WARM RESET

Designers should also consider the case of a warm restart of a Link with a PHY in Low Power Mode. Once the PHY enters Low Power Mode, DIR is asserted and the clock is stopped. The USB3300 looks for STP to be asserted to re-start the clock and then resume normal synchronous operation.

Should the USB3300 be suspended in Low Power Mode, and the Link receives a hardware reset, provision is made to allow the PHY to recover from Low Power Mode and start its clock. If the Link asserts STP on reset, the PHY will exit Low Power Mode and start its clock.

If the Link does not assert STP on reset the interface protection pull-up can be used. When the Link is reset, its STP output will tri-state and the pull-up resistor will pull STP high, signaling the PHY to restart its clock.

6.1.9.4 Minimizing Current in Low Power Mode

In order to minimize the suspend current in Low Power Mode, the OTG comparators can be disabled to reduce suspend current. During suspend, the VbusVId and SessEnd comparators are not needed and can be disabled using the USB Interrupt Enable Rise and USB Interrupt Enable Fall registers. By disabling the interrupt in BOTH the rise and fall registers, the SessEnd and VbusVId comparators are turned off. When exiting suspend, the Link should immediately re-enable the comparators if host or OTG functionality is needed.

In addition to disabling the OTG comparators in suspend, the Link may choose to disable the Interface Protect Circuit. By setting the Interface Control, bit 7, *InterfaceProtectDisable* high, the Link can disable the pull-up resistor on STP.

6.1.10 Full Speed/Low Speed Serial Modes

On the right side of the browser, an "AI Powered Search" interface is active. It shows a chat conversation with the AI:

- Question: "What is the Electrostatic Discharge (ESD) sensitivity or rating"
- Answer: "±8kV Human Body Model (HBM). Was this helpful?"
- Question: "what is the control interface of this device?"
- Answer: "The component uses the industry standard ULPI digital interface. Was this helpful?"
- Question: "what is its clock frequency?"
- Answer: "The clock frequency of the component with the ULPI digital interface is 60 MHz. Was this helpful?"
- Input: "is there any chance |"
- Buttons: "Send"

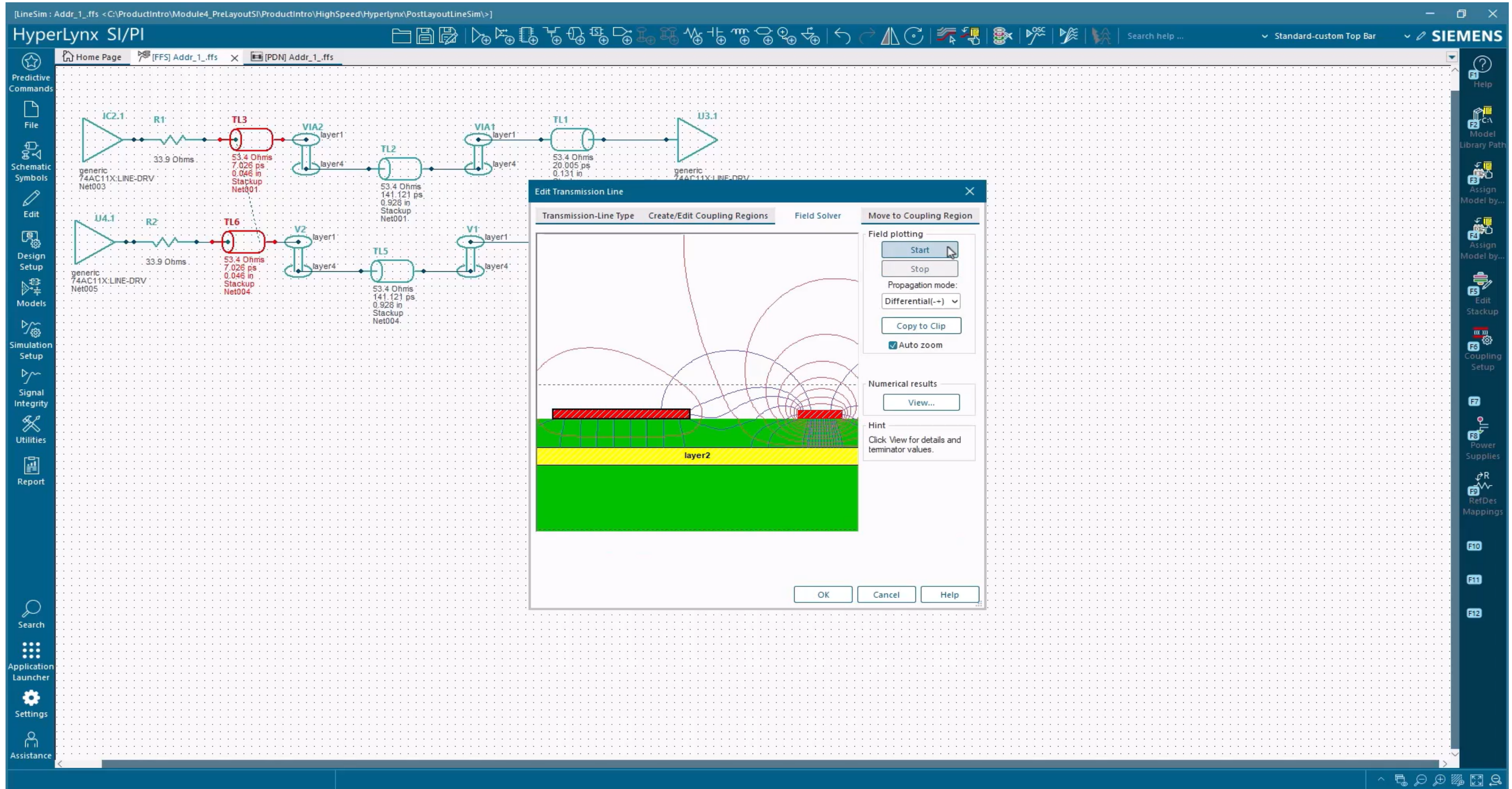
Integrated constraint management

The screenshot displays the Siemens Constraint Manager interface for a project named 'SoC_FPGA_Host'. The main window shows a table of constraint rules, organized into sections for different design classes. The table columns include Scheme/Net Class/Layer, Index, Type, Display Pattern, Via Assignments, Route, Trace Width (mm) (Minimum, Typical, Expansion), Typical Impedance (Ohm), and Differential (Typical Impedance, Spacing, Via Spacing).

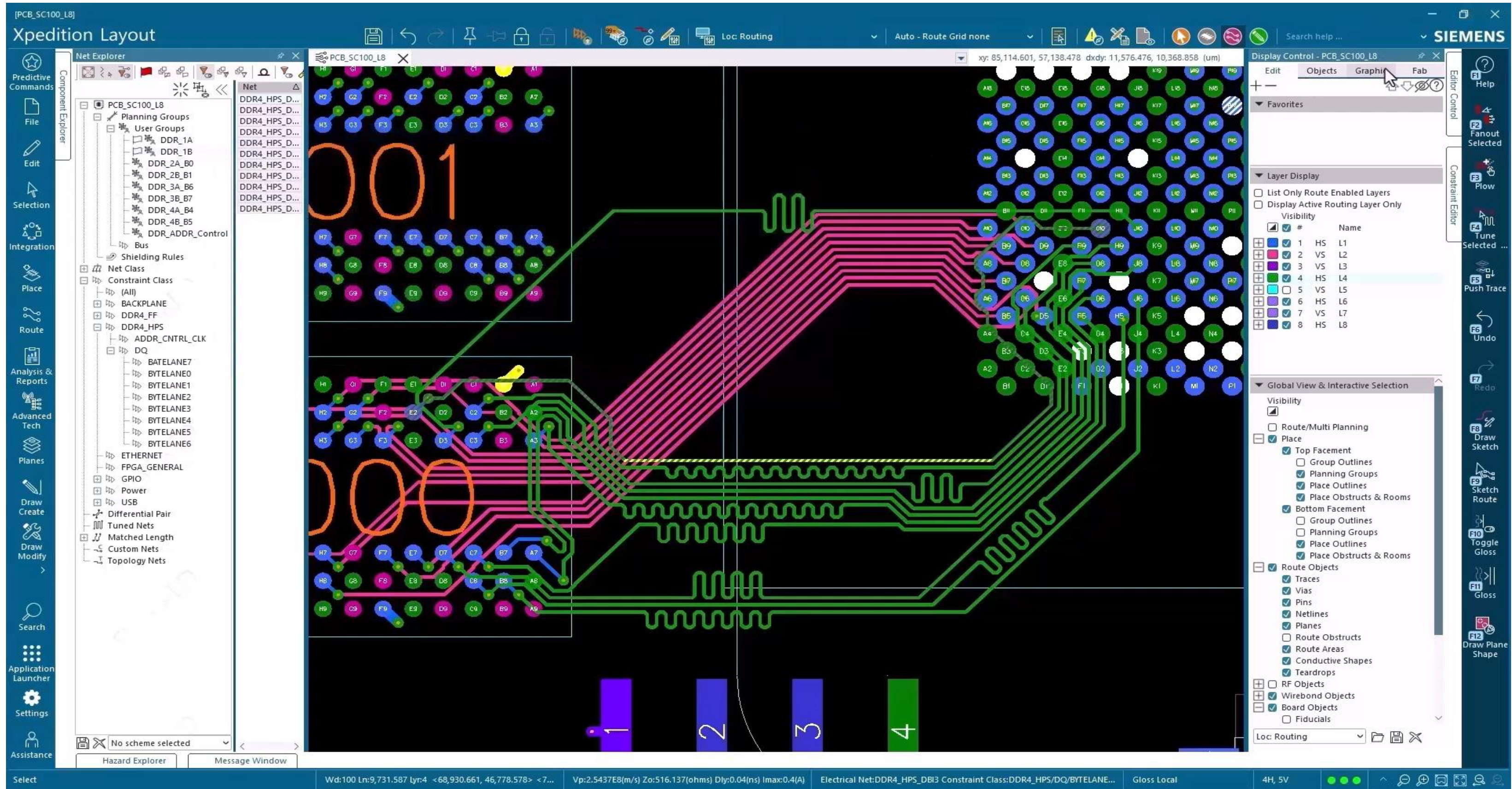
Scheme/Net Class/Layer	Index	Type	Display Pattern	Via Assignments	Route	Trace Width (mm)			Typical Impedance (Ohm)	Differential		
						Minimum	Typical	Expansion		Typical Impedance (Ohm)	Spacing (mm)	Via Spacing (mm)
(Master)												
(Default)			(None)	[default]	[checked]	0.1	0.3	0.3	50		0.127	
L8_GND3	8	Signal			[checked]	0.1	0.3	0.3	97.051..	97.809..	0.11	
L7_SIG5	7	Signal			[checked]	0.1	0.3	0.3	83.678..	154.97..	1	
L6_SIG4	6	Signal			[checked]	0.1	0.3	0.3	66.081..	126.2..	1	
L5_SIG3	5	Signal			[checked]	0.1	0.3	0.3	51.043..	99.148..	1	
L4_SIG2	4	Signal			[checked]	0.1	0.3	0.3	29.538..	52.909..	0.172	
L3_GND2	3	Plane			[checked]	0.1	0.3	0.3			0.172	
L2_SIG1	2	Signal			[checked]	0.1	0.3	0.3	34.381..	68.09..	1	
L1_GND1	1	Signal			[checked]	0.1	0.3	0.3	58.893..	83.696..	0.11	
Single_40_Diff_80			(None)	[default]	[checked]	0.1	0.1	0.1	50		0.1	
Power_L			(None)	[default]	[checked]	0.1	0.25	0.5	50		0.127	
Trace_Power			(None)	[default]	[checked]	0.2	0.3	1	50		0.127	
Power_P1V2			(None)	[default]	[checked]	0.1	0.3	0.5	50		0.127	
PWR_GND			(None)	[default]	[checked]	0.1	0.3	0.5	50		0.127	
(Minimum)												
(Default)						0.1	0.3	0.3	50		0.127	
Single_40_Diff_80						0.075	0.075	0.075	50		0.075	
Power_L						0.1	0.15	0.3	50		0.127	
Trace_Power						0.1	0.3	1	50		0.127	
Power_P1V2						0.1	0.3	0.5	50		0.127	
PWR_GND						0.1	0.3	0.5	50		0.127	
BGA												
(Default)				[default]	[checked]	0.1	0.3	0.5	50		0.127	
Single_40_Diff_80				[default]	[checked]	0.075	0.075	0.075	50		0.075	
Power_L				[default]	[checked]	0.1	0.15	0.3	50		0.127	
Trace_Power				[default]	[checked]	0.1	0.3	1	50		0.127	
Power_P1V2				[default]	[checked]	0.1	0.3	0.5	50		0.127	
PWR_GND				[default]	[checked]	0.1	0.3	0.5	50		0.127	
P1V2_V1												
(Default)				[default]	[checked]	0.1	0.3	0.5	50		0.127	
Single_40_Diff_80				[default]	[checked]	0.1	0.1	0.1	50		0.1	
Power_L				[default]	[checked]	0.1	0.25	0.5	50		0.127	
Trace_Power				[default]	[checked]	0.2	0.3	1	50		0.127	
Power_P1V2				[default]	[checked]	0.1	0.3	0.5	50		0.127	
PWR_GND				[default]	[checked]	0.1	0.3	0.5	50		0.127	

The interface includes a left-hand sidebar with navigation options like Predictive Commands, File, Edit, Integration, Manage Grid, Physical Rules, Electrical Rules, and Analysis & Reports. The bottom status bar shows 'Selected 1 from 36 rows. Net Class[1]' and the application name 'DxDesigner'.

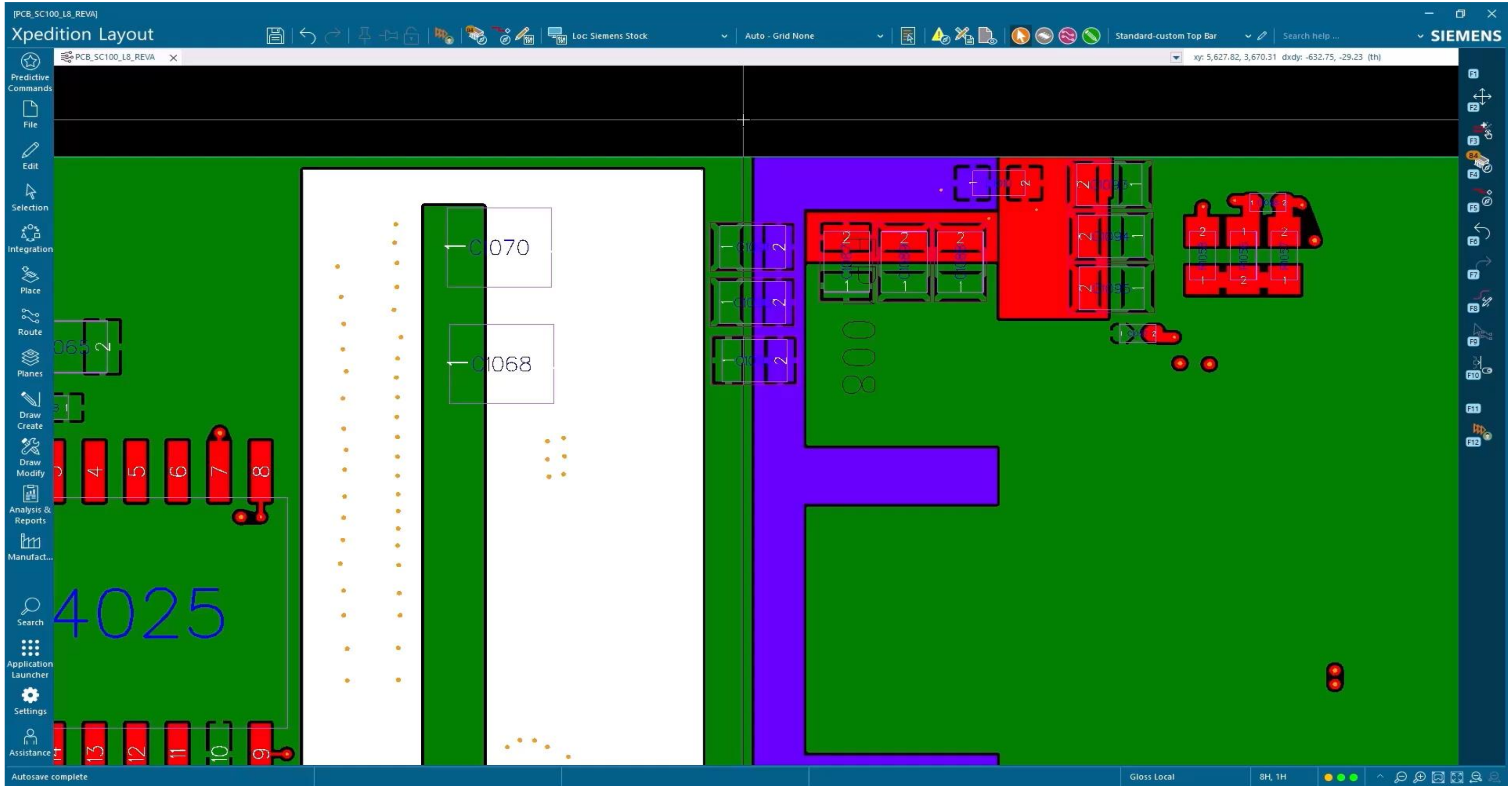
Pre-layout signal integrity



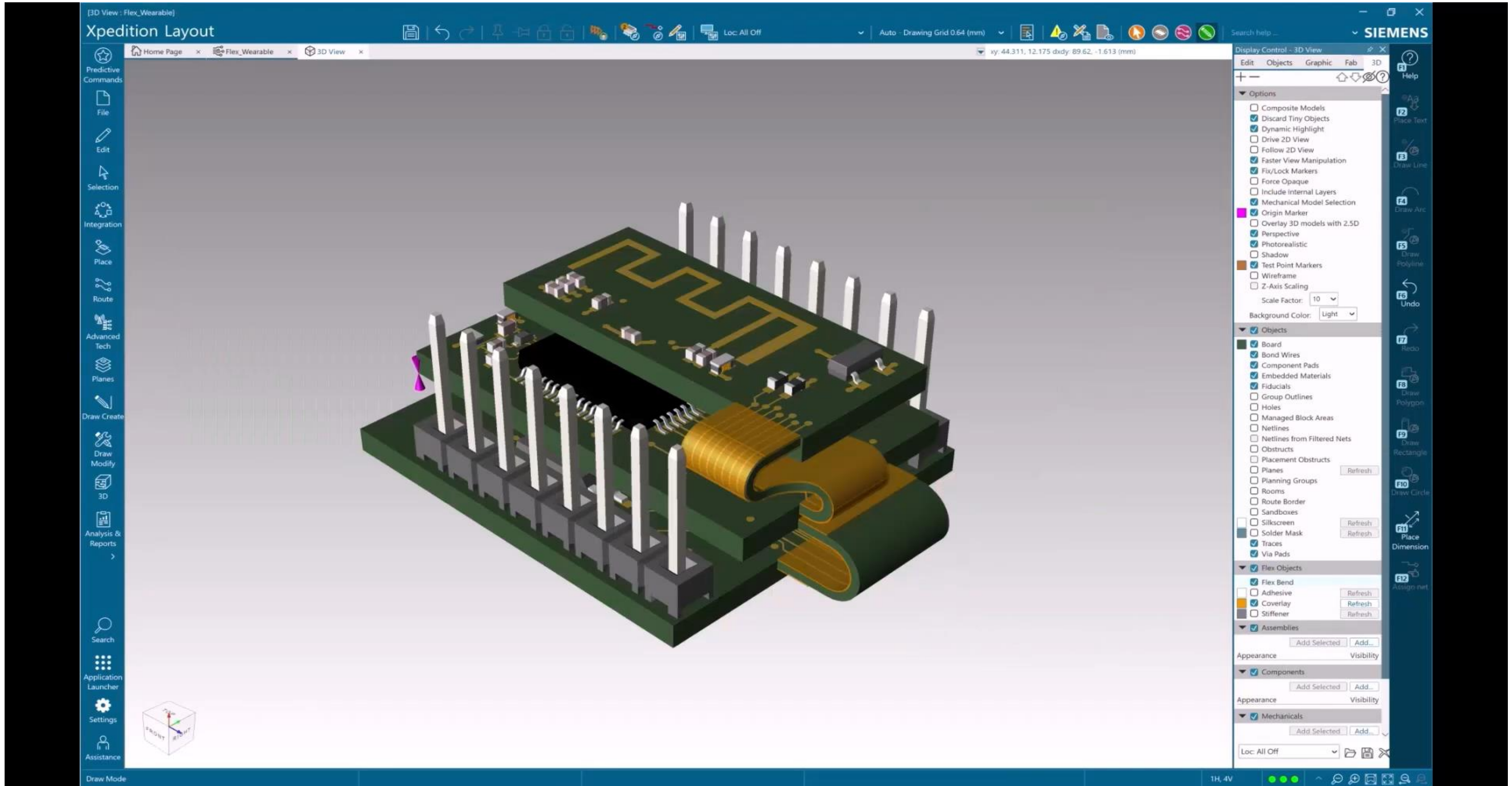
Connectivity routing



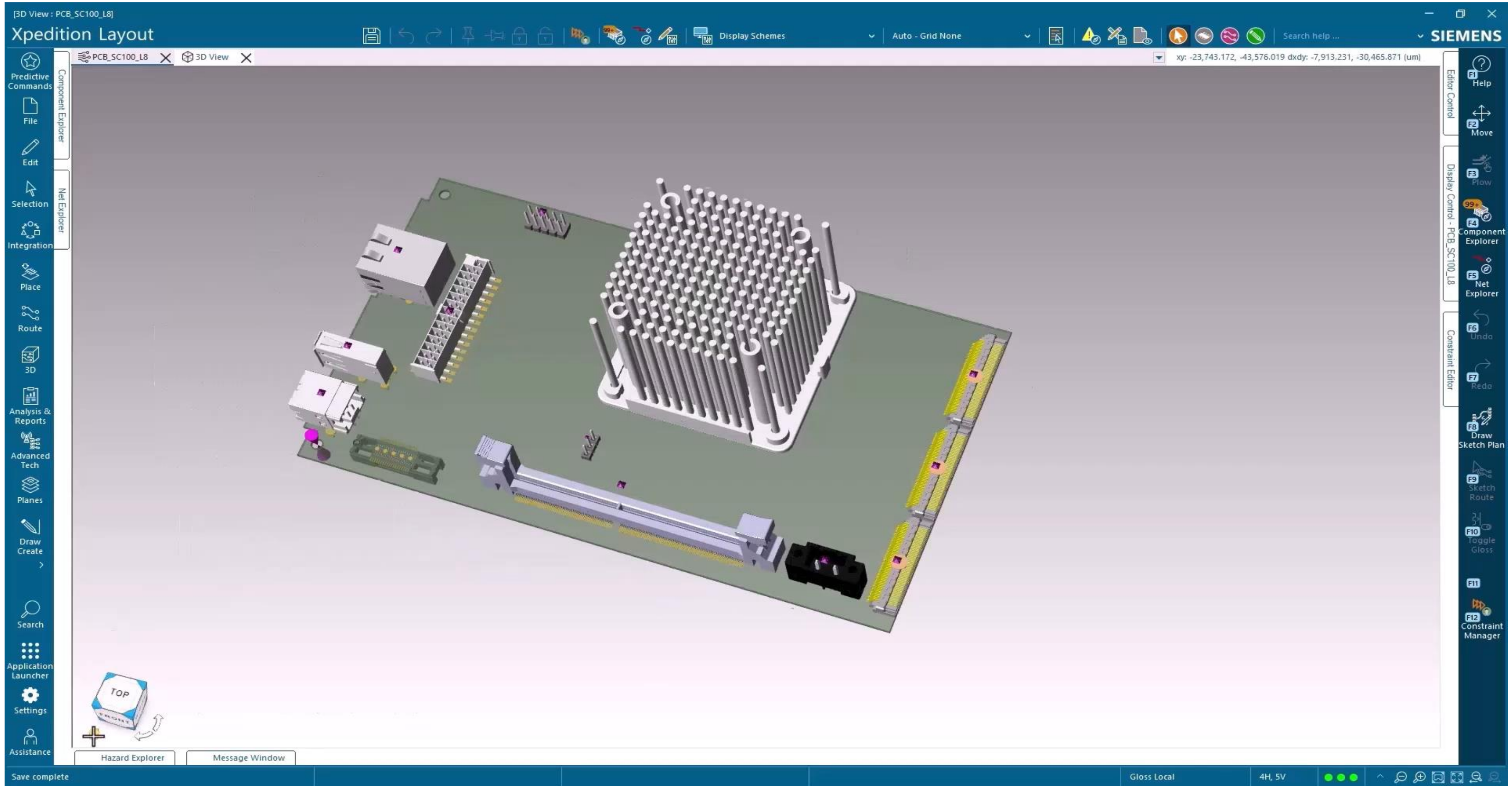
Physical reuse



Rigid-flex



ECAD/MCAD co-design



Actionable DFM analysis

The screenshot displays the PCBflow software interface. At the top left, the PCBflow logo is visible. The top right corner indicates it is powered by Valor NPI and features the SIEMENS logo. A vertical navigation bar on the left contains icons for Home, Projects, Manufacturer tools, Network, and Account Manager. The main content area is titled "Welcome to PCBflow, Aaron Rissler!" and asks "What do you want to do today?". Two primary options are presented: "Fabrication Analysis" (DFM (DFF) – Discover design faults that may cause problems during bare-board manufacturing) and "Assembly Analysis" (DFM (DFA) – Discover design or BOM faults that may cause problems during PCB assembly). Below these, a "More options" section is shown in a light blue box, containing "BOM Pricing" (Accurate and up-to-date information about component price and availability), "Projects" (Create and manage your projects. Review files and results, collaborate, or share project data.), and "QuickPrice" (Instant, accurate price estimates for manufacture and assembly). A mouse cursor is visible at the bottom center of the interface.

Agenda

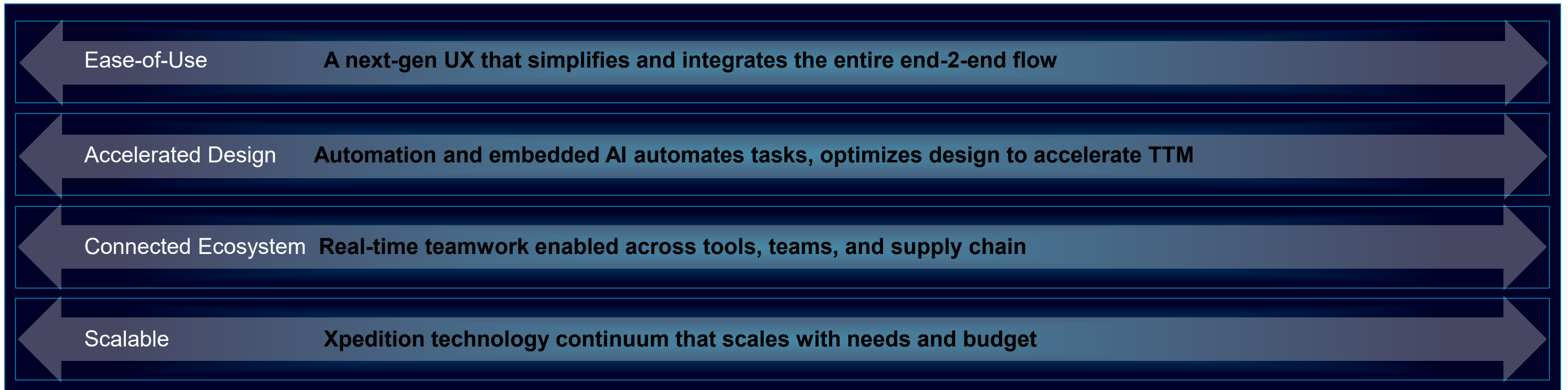
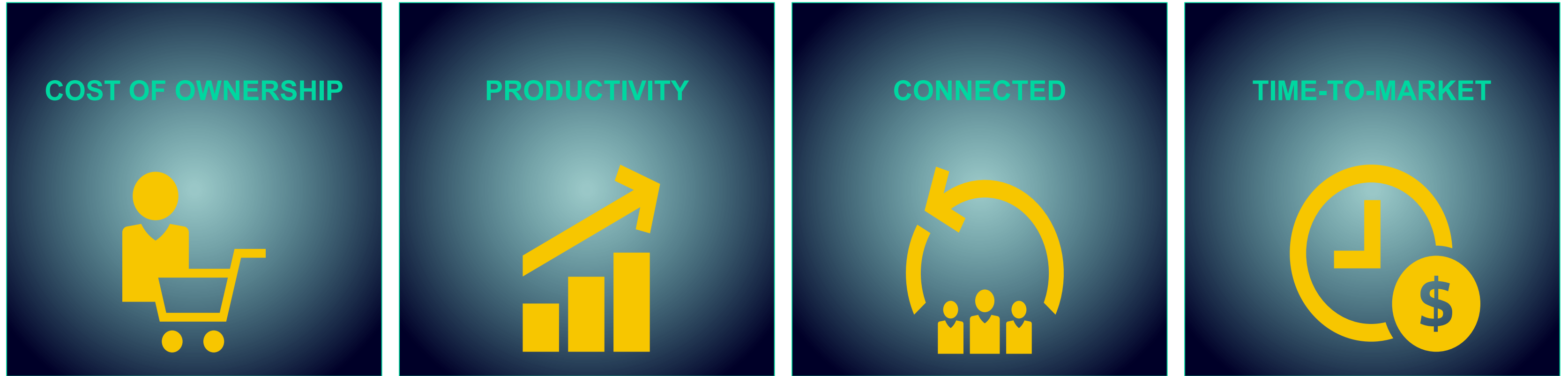
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감사합니다.