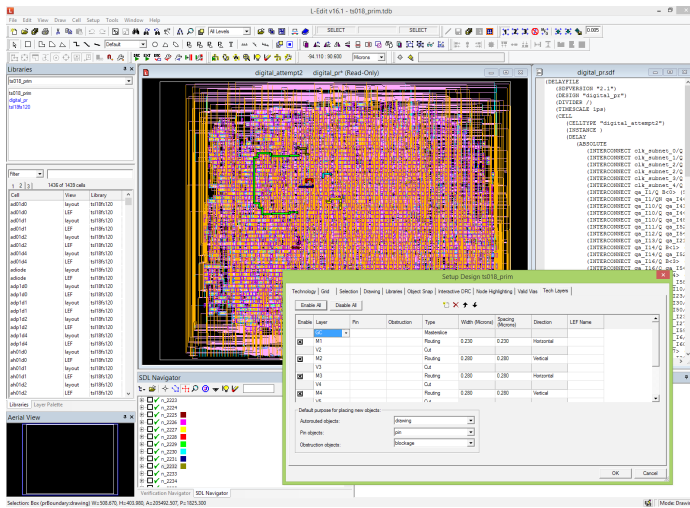


# Tanner Place and Route



Tanner Place and Route interface; the tool is optimized for the needs of big analog/little digital mixed-signal designs.

## A Complete RTL to GDS Flow

Tanner Place and Route can help whether you're designing an analog IC with a small amount of digital control or a more complex mixed-signal ASIC. The tool facilitates bringing together complex digital circuits with high performance analog interfaces, providing a flow that offers all the capabilities you need today. It is backed up with unparalleled support and can evolve to meet the needs of your designs for tomorrow.

No other EDA vendor offers a tool flow so closely aligned with the needs of big analog/little digital designs than Tanner EDA by Mentor Graphics, which focuses on supporting companies working in applications such as automotive, Internet of Things (IoT) imaging/display, industrial control, medical and power management.

Tanner Place and Route is a right-size place and route solution for big analog/little digital mixed-signal design, offering excellent performance, ease of use and value. The tool is optimized for analog specialty process technologies on nodes of 90 nm and above, with 10k-50k gates of digital logic. Tanner Place and Route is highly flexible, allowing the user nuanced control during every phase of the flow.

## Place and Route

Tanner Place and Route is optimized for the needs of big analog/little digital mixed-signal designs on typical analog process nodes. The tool completes the end-to-end flow for analog/mixed-signal designs offered by Tanner EDA by Mentor Graphics. Tanner Place and Route includes clock tree synthesis, SDF timing extraction and industry standard file format support.

## FEATURES AND BENEFITS:

- Cost-effective, integrated digital place and route tool for mixed-signal designs
- Clock tree synthesis
- SDF and SPEF timing extraction
- Support for standard digital formats, including LEF/DEF, Liberty, Verilog and SDF
- Interactive, integrated with Tanner L-Edit IC layout tool
- Platform independence on Windows or Linux
- Ease of use: Intuitive and quick learning curve
- Unparalleled customer support
- Flexible licensing

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## Features:

- Clock tree synthesis and delay-matched clock routing
- LEF/DEF support
- Optimized for 90 nm and above, 10k-50k gates
- Interactive/integrated with Tanner L-Edit IC layout tool

## Standards Support

Tanner Place and Route uses industry standard file formats for easy interoperability with libraries, tools and flows from any foundry or vendor. Formats include OpenAccess and GDSII for layout data, LEF/DEF for abstracts and routing, Liberty for timing data, SPEF for parasitics and SDF for timing annotation.

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**For the latest product information, contact us at: [www.mentor.com](http://www.mentor.com), (800) 547-3000**

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