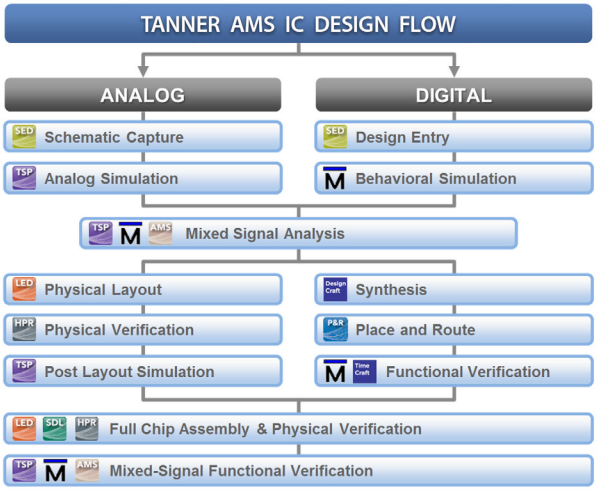
Tanner AMS IC Design Flow



End-to-end design flow for AMS IC design.

THE FULL-FLOW AMS SOLUTION

The Tanner AMS IC design flow is a complete end-to-end design flow for analog/mixed-signal (AMS) IC designs. The flow consists of highly integrated front and back-end tools, from schematic capture, mixed-signal simulation and waveform probing to physical layout and foundry-compatible physical verification. All the tools in the flow share a common architecture and user interface.

Considered together these tools comprise a suite that is interoperable with many popular industry tools and industry-standard netlists. The suite minimizes risk by providing foundry support, including many foundry-certified PDKs. The tools are intuitive, easy to use and accessible from anywhere because they are platform-independent, with versions available for both Windows and Linux.

FEATURES AND BENEFITS:

- Complete, full-flow analog/mixed-signal (AMS) IC design suite
- OpenAccess, LEF/DEF, Liberty and SDF support
- Simulate combined netlists at various abstraction levels: behavioral models, block-level RTL, gate- and transistor-level blocks
- Debugging and advanced verification with System Verilog, Verilog, Verilog-AMS, Verilog-A and VHDL
- Top-down, mixed-signal co-simulation
- Proven, compatible synthesis with DFT support
- High-speed timing analysis
- All-angle layout editor with interactive/real-time DRC
- Hierarchical DRC and netlist extraction with Calibre compatibility
- Productive place and route for AMS design
- Foundry PDK support
- Platform independence on Windows or Linux
- Intuitive and easy to use; quick learning curve
- Unparalleled customer support
- Flexible licensing

Tanner AMS IC Design Flow	
Schematic capture	✔
Waveform editor	✔
Spice simulation	✔
Behavioral modeling	✔
Mixed-signal analysis	✔
Digital RTL simulation	✔
Layout editor	✔
Interactive or real-time DRC	✔
Node highlighting	✔
Pad cross-reference extractor	✔
Schematic-driven layout	✔
Chip assembly router	✔
Analog layout acceleration	✔
Design rule checking, DRC & LVS	✔
2D parasitic extraction	✔
3D parasitic extraction	✔
Calibre interface	✔
Standard cell place & route	✔
Synthesis	✔
Static timing analysis	✔
Design for test	✔
Automatic test pattern generation	✔

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