Tanner AMS IC Design Flow

TANNER AMS IC DESIGN FLOW		
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ANALOG	DIGITAL	
Schematic Capture	Pesign Entry	
Analog Simulation	M Behavioral Simulation	
Mixed Signal Analysis		
Physical Layout	Synthesis	
Physical Verification	Place and Route	
Post Layout Simulation	Functional Verification	
Image: Second system Full Chip Assembly & Phy Image: Second system Image: Second system Image: Se	I	

End-to-end design flow for AMS IC design.

THE FULL-FLOW AMS SOLUTION

The Tanner AMS IC design flow is a complete end-to-end design flow for analog/mixed-signal (AMS) IC designs. The flow consists of highly integrated front and back-end tools, from schematic capture, mixed-signal simulation and waveform probing to physical layout and foundry-compatible physical verification. All the tools in the flow share a common architecture and user interface.

Considered together these tools comprise a suite that is interoperable with many popular industry tools and industry-standard netlists. The suite minimizes risk by providing foundry support, including many foundry-certified PDKs. The tools are intuitive, easy to use and accessible from anywhere because they are platform-independent, with versions available for both Windows and Linux. Analog/Mixed-signal (AMS) Design and Verification

DATASHEET

FEATURES AND BENEFITS:

- Complete, full-flow analog/mixedsignal (AMS) IC design suite
- OpenAccess, LEF/DEF, Liberty and SDF support
- Simulate combined netlists at various abstraction levels: behavioral models, block-level RTL, gate- and transistor-level blocks
- Debugging and advanced verification with System Verilog, Verilog, Verilog-AMS, Verilog-A and VHDL
- Top-down, mixed-signal co-simulation
- Proven, compatible synthesis with DFT support
- High-speed timing analysis
- All-angle layout editor with interactive/real-time DRC
- Hierarchical DRC and netlist extraction with Calibre compatibility
- Productive place and route for AMS design
- Foundry PDK support
- Platform independence on Windows or Linux
- Intuitive and easy to use; quick learning curve
- Unparalleled customer support
- Flexible licensing



Tanner AMS IC Design Flow		
Schematic capture	V	
Waveform editor	V	
Spice simulation	V	
Behavioral modeling	v	
Mixed-signal analysis	v	
Digital RTL simulation	V	
Layout editor	V	
Interactive or real-time DRC	~	
Node highlighting	v	
Pad cross-reference extractor	v	
Schematic-driven layout	v	
Chip assembly router	~	
Analog layout acceleration	v	
Design rule checking, DRC & LVS	V	
2D parasitic extraction	V	
3D parasitic extraction	v	
Calibre interface	v	
Standard cell place & route	~	
Synthesis	v	
Static timing analysis	v	
Design for test	v	
Automatic test pattern generation	v	

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Corporate Headquarters Mentor Graphics Corporation 8005 SW Boeckman Road Wilsonville, OR 97070-7777 Phone: 503.685.7000 Fax: 503.685.1204

Sales and Product Information Phone: 800.547.3000 sales_info@mentor.com Silicon Valley Mentor Graphics Corporation 46871 Bayside Parkway Fremont, CA 94538 USA Phone: 510.354.7400 Fax: 510.354.7467

North American Support Center Phone: 800.547.4303

Europe Mentor Graphics Deutschland GmbH Arnulfstrasse 201 80634 Munich Germany Phone: +49.89.57096.0 Fax: +49.89.57096.400 Pacific Rim Mentor Graphics (Taiwan) 11F, No. 120, Section 2, Gongdao 5th Road HsinChu City 300, Taiwan, ROC Phone: 886.3.513.1000 Fax: 886.3.573.4734 Japan Mentor Graphics Japan Co., Ltd. Gotenyama Garden 7-35, Kita-Shinagawa 4-chome Shinagawa-Ku, Tokyo 140-0001 Japan Phone: +81.3.5488.3033 Fax: +81.3.5488.3004



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