Questa 10.3 Series Product Comparison

Feature	Questa Core *Large Block/System Simulation and ABV*	Questa Prime *Advanced Verification, All Languages*	Questa Ultra *Advanced Verification, All Languages, Fastest Closure*
General			
Licensing - Floating License	■	■	■
Language Neutral License	Option (LNL)	■	■
ASIC Sign-Off		■	■
Platform-Independent Compiled Database	■	■	■
Native-Compiled Architecture	■	■	■
Incremental Compilation	■	■	■
32/64-Bit Cross-Compatability	■	■	■
Languages			
SystemVerilog IEEE1800 Design	■	■	■
SystemVerilog IEEE1800 Verification	Assertions Only	■	■
VHDL (including VHDL-2008)	VHDL, LNL or Mixed	■	■
Verilog	VLOG, LNL or Mixed	■	■
Mixed Language	Mixed	■	■
PSL (IEEE 1850)	■	■	■
Verilog PLI/VPI	■	■	■
SystemVerilog Direct Programming Interface	■	■	■
VHDL FLI	■	■	■
UPF 1.1 and 2.0 (IEEE 1801)	Option (PA Sim)	Option (PA Sim)	■
SystemC 2.2 (IEEE 1666/OSCI 2.2)	Option (SystemC)	■	■
Analog/Mixed Signal (Advance MS Product)	Questa ADMS	Questa ADMS	Questa ADMS
Advanced Verification			
Assertion-Based Verification	■	■	■
Questa Verification Library (Assertion Checker & Monitor Library)	OVL and QVLChecker Library Only	■	■
SystemVerilog Constrained-Random Test Generation		■	■
SystemVerilog Covergroups (and Coverpoints)		■	■
Open Verification Methodology (OVM)		■	■
Unified Verification Methodology (UVM)		■	■
Power Aware Simulation		Option(PA Sim)	■
inFact Testbench Automation		Add On Product	■
Codelink (Processor-Based Verification)		Add On Product	Add On Product
Questa Verification Components (Questa Verification IP Library)		Add On Product	Add On Product
Verification Management & Coverage			
Code Coverage (with Toggle Coverage)	■	■	■
Functional Coverage	PSL and SVA Cover directive	■	■
Unified Coverage DataBase (UCDB)	Code Coverage and PSL and SVA Assert and Cover	■	■
Coverage Viewer	Code Coverage and PSL and SVA Assert and Cover	■	■
Test Ranking	Code Coverage and PSL and SVA Assert and Cover	■	■
Test Plan Tracking with Excel/OpenOffice plugin	Option (VM)	■	■
Verification Results Analysis and database	Option (VM)	■	■
Verification Run Management (regressions)	Option (VM)	■	■
Design Entry, Debug, and Analysis			
HDL Editor	■	■	■
Integrated Project Manager	■	■	■
Source Code Templates and Wizards	■	■	■
Interactive & Post-Simulation Debug	■	■	■
Dataflow Graphical & Textual Causality Traceback	■	■	■
Schematic viewer	■	■	■
Advanced FSM Debug	■	■	■
Source Annotation	■	■	■
Hyperlinked Navigation	■	■	■
Class Browser	■	■	■
Dynamic Thread Debug & Control	■	■	■
OVM/UVM - Aware Debugging	■3	■	■
Assertion Thread Viewer		■	■
C Debugger	Option[1]	■	■
Memory Window	■	■	■
Multiple Waveform Windows	■	■	■
Extra Standalone Viewer	Option	Option	Option
Waveform Compare	■	■	■
Transaction Viewing and Analysis	Option[1]	■	■
Protocol Recognition with transactions		Option[2]	Option[2]
JobSpy	■	■	■
SignalSpy	■	■	■
User-Customizable GUI (via Tk)	■	■	■
Simulation			
Single-Kernel Simulation Engine	■	■	■
Verilog RTL & Gate Performance Optimizations	■	■	■
VHDL RTL & VITAL Performance Optimizations	■	■	■
Performance and Memory Profiler	■	■	■
Dynamic Object Capacity Profiler		■	■
Simulation & Compile Flow Optimizations	■	■	■
Waveform Management Tool Set	■	■	■
VCD and Extended VCD Support	■	■	■
VCD Re-Simulation	■	■	■
Batch Mode Simulation	■	■	■
Integrated Sim Farm Support (via JobSpy)	■	■	■
Interactive Simulation	■	■	■
Checkpoint & Restore	■	■	■
VHDL 2008 Encryption	■	■	■
Verilog 2005 Encryption	■	■	■
SecureIP	■	■	■
Platform Support			
32-Bit OS Support	Linux, Windows XP/Vista, Win7,8 [4]	Linux, Windows XP/Vista, Win7,8 [4]	Linux
64-Bit OS Support	Linux x86-64, Win7,8-64[5]	Linux x86-64, Win7,8-64[5]	Linux x86-64

1 - Included in SystemC Option
2 - Included with Questa Verification IP
3 - OVM and UVM Aware Debugger is present but things like randomize, and functional coverage for OVM/UVM are not available

4 - LINUX RHEL 4,5,6 SLES 10,11 Windows 32 XP, Vista, Windows 7
5 - LINUX RHEL 4,5,6 SLES 10,11 Windows 64 Windows 7

NOTE - not available on Windows: wlf threads, vopt threads, multi-core