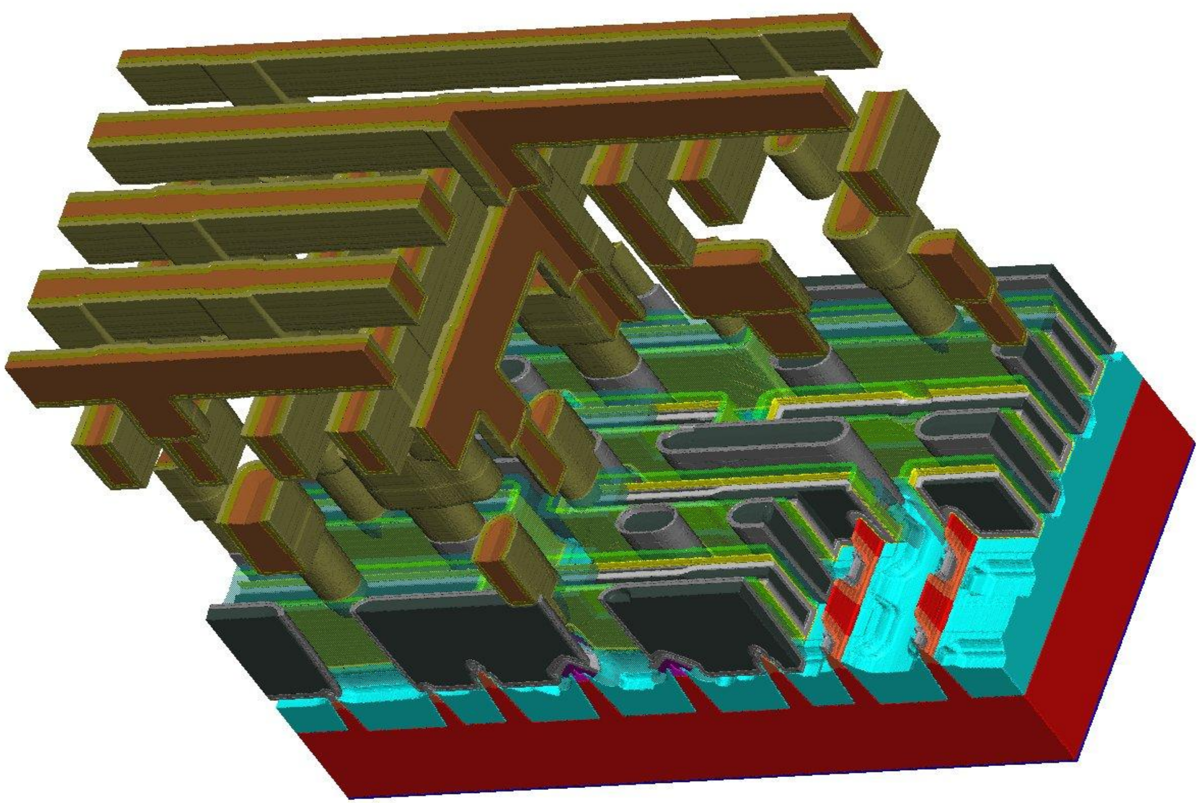
COVENTOR

SEMulator3D

Virtual Fabrication:

Integrated Process Modeling for Advanced Technology

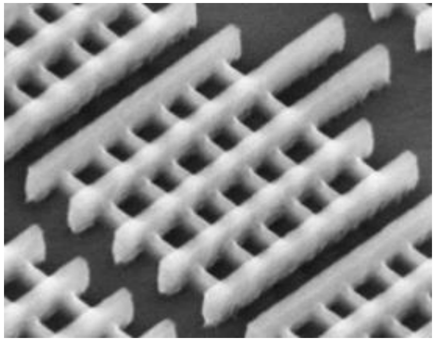


Outline

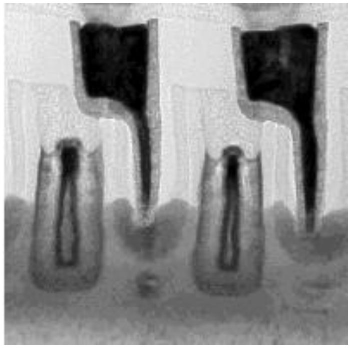
- SEMulator3D Product Overview
  - Virtual Fabrication
  - SEMulator3D Basic Platform
  - Advanced Modeling Module:
    - Selective Epitaxy, Advanced Etch, **Pattern Dependence, Visibility-Limited Deposition**
  - Automation Module:
    - Virtual Metrology, Expeditor, **Structure Search**
  - Meshing Module
- Example Use Cases
  - BEOL Development:
    - Cross-Wafer Optimization, Design Rule Development
  - FEOL Development:
    - Variation Analysis, Parasitic Extraction
  - Memory Development:
    - Micro- vs. Macro- Scale Modeling, Defect Evolution
- Conclusion
  - A Virtual Learning Cycle
- Backup Charts

New in 2014!!!

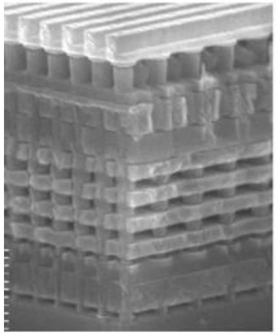
Complexity Drives Opportunity



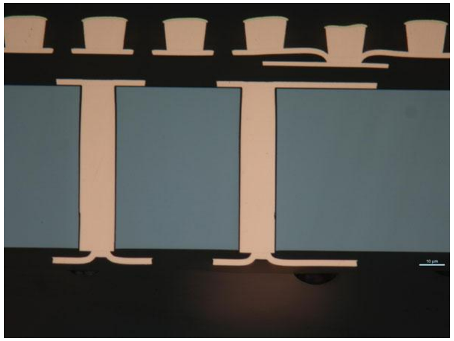
FinFET (Intel)



Self-Aligned Contact (Intel)



BiCS Flash (Toshiba)



3D TSV (Fraunhofer)

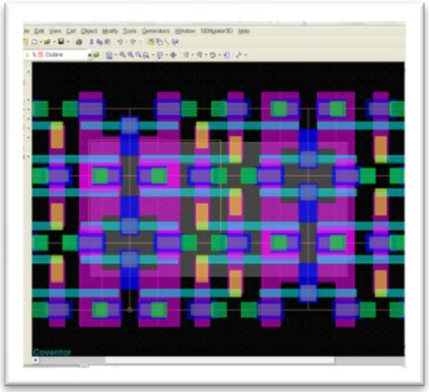
- ***Process Cost and Complexity Increasing at Alarming Pace***
  - *Innovation is in structural integration – The challenge is* ***PHYSICAL***

- ***New fab $5-10B, New process > $2B***
  - *This is all spent before a single revenue-generating wafer can be run*
  - *Much of process development cost is trial-and-error in-fab experimentation*
  - *A single cycle of experimental learning can cost $50M and take 3 months*

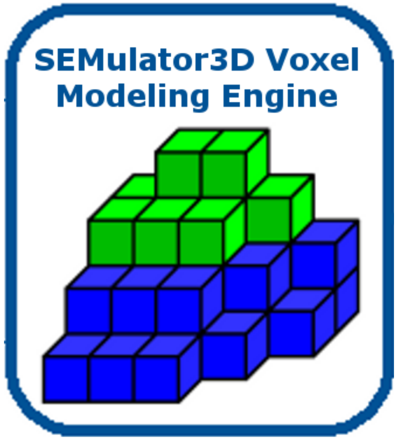
- ***Trial-and-Error Silicon Engineering is not acceptable!***
  - ***The time and cost of TRIAL is too great***
  - ***The penalty for ERROR is too extreme***

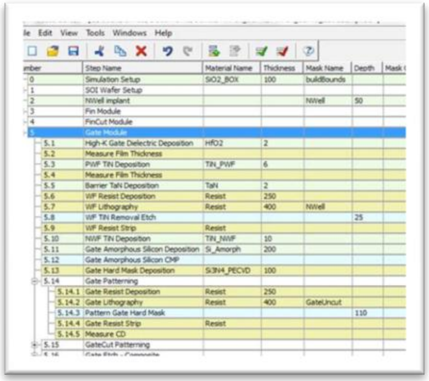
What is SEMulator3D?

A Powerful 3D Semiconductor Virtual Fabrication Platform



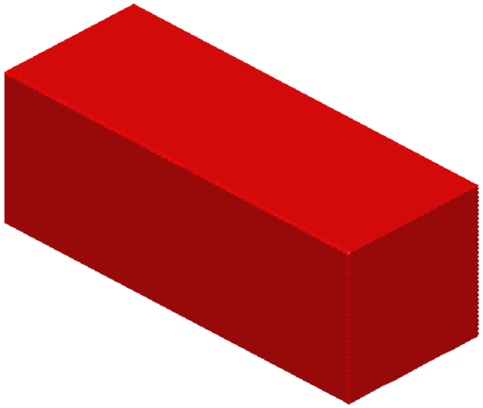
Layout Editor:
Design, OPC, PrintSim, etc.





Process Editor:
Step-by-Step Process
Behavioral Description

3D Viewer:
RMG FinFET Demo
Self-Aligned Contact
TFMHM BEOL w/ SAV



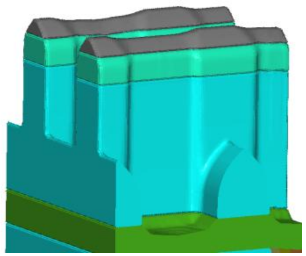
- Applicable to ANY process & ANY layout
- Replaces build & test with ***accurate*** 3D modeling of large areas & complex process sequences
- Provides validation and visualization of relationships between design and process
- Provides a ***predictive*** view of design-technology interactions

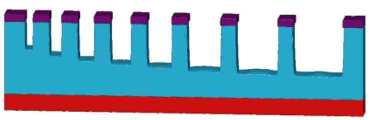
SEMulator3D 2014 Additional Packages

Three packages add additional model predictivity and usability:

Advanced Modeling

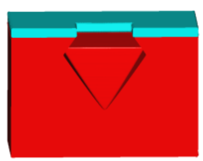
Multi Etch
Etch multi-material film stacks with sputtering, re-deposition, anisotropy

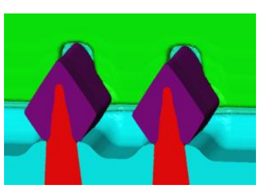




Pattern Dependence
Etch loading, ARDE, lag

Crystal Etch
Crystallographic etching of c-S

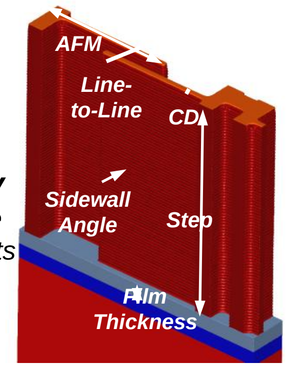


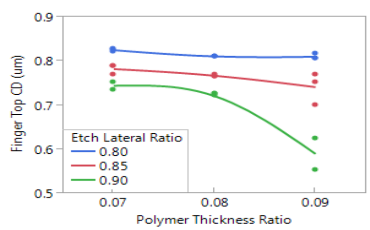


Selective Epitaxy
SiGe/SiP growth on c-Si

Automation

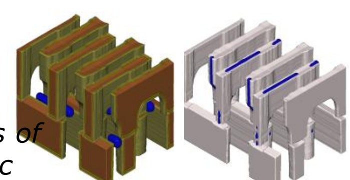
Virtual Metrology
Mimic in-line measurements





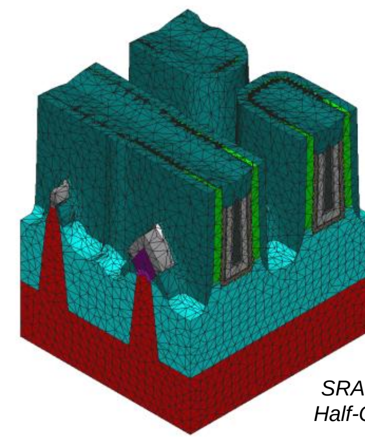
Expeditor
Batch mode for DOE or variation studies

Structure Search
Mark violations of 3D geometric criteria

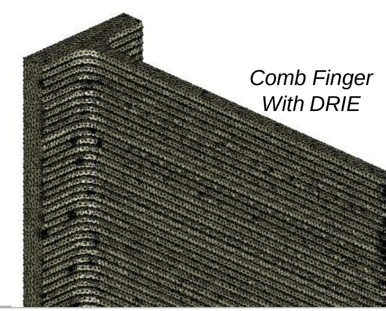


Meshing

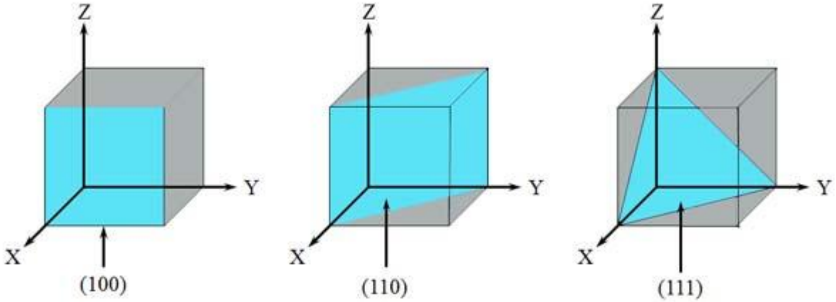
Export surface or volume meshes for interfacing with downstream tools



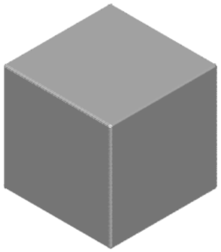
SRAM Half-Cell



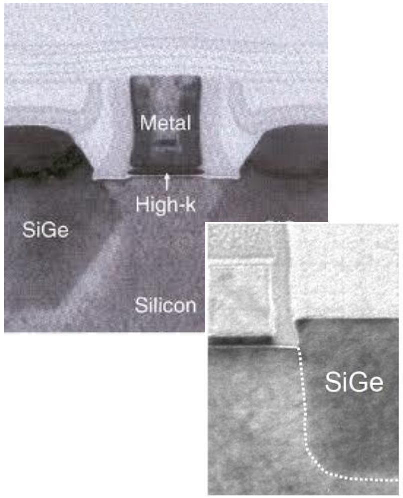
Advanced Epitaxy Modeling



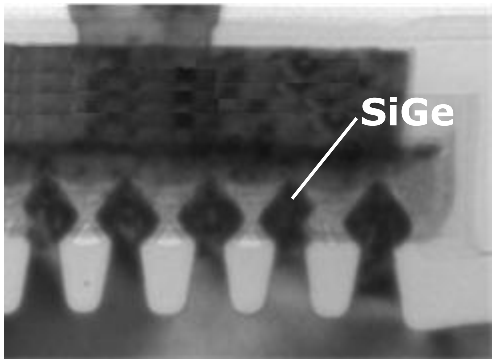
<111> facets form due to slow growth on the <111> planes



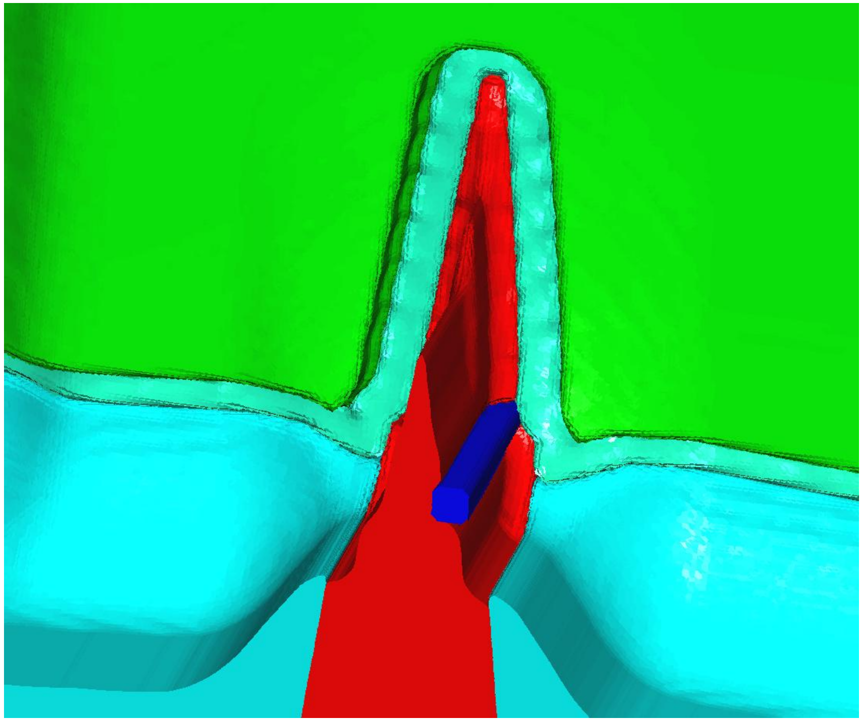
Epitaxial growth is sensitive to crystal planes <111> directions normally grow slowest and form limiting facets.



Embedded SiGe in planar technology (Intel, IBM)



22nm Tri-gate (Intel)



FinFET SiGe Epitaxy (with residual oxide)

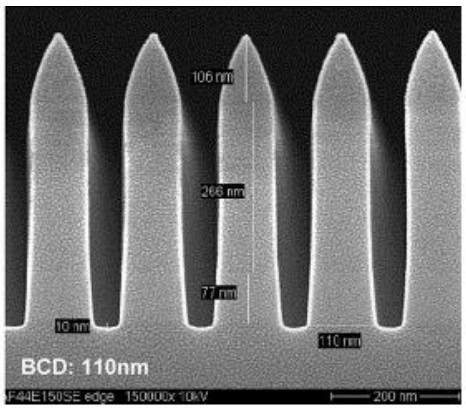
Advanced Etch Modeling

Physics-driven etch modeling of

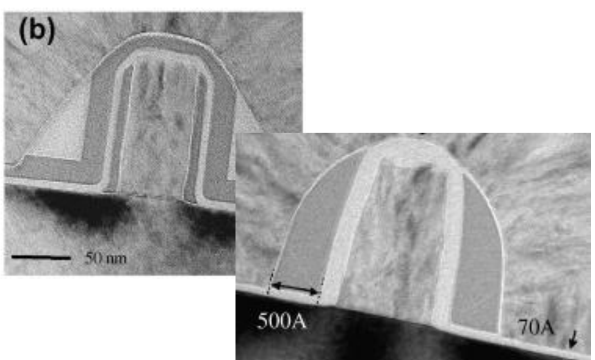
- Multi-material film stacks
- Multiple types of etch physics

Key Features

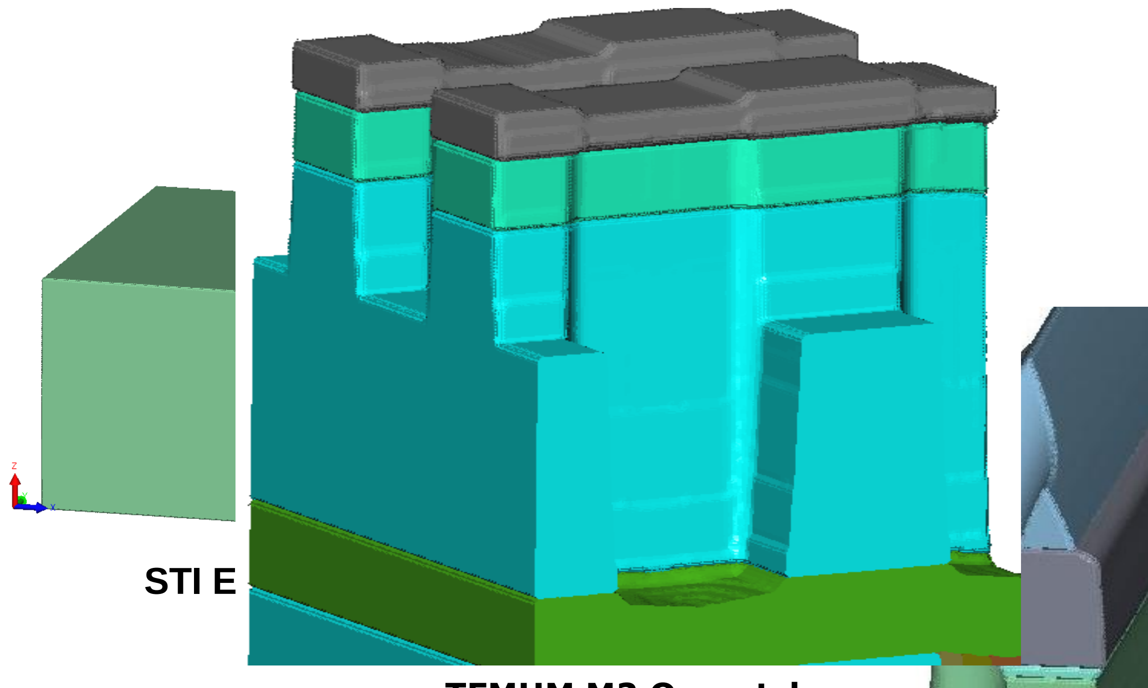
- Etch physics:
  - Redeposition (aka passivation)
  - Sputtering (physical etching)
  - Etch bias (lateral or chemical etching)



STI Etches



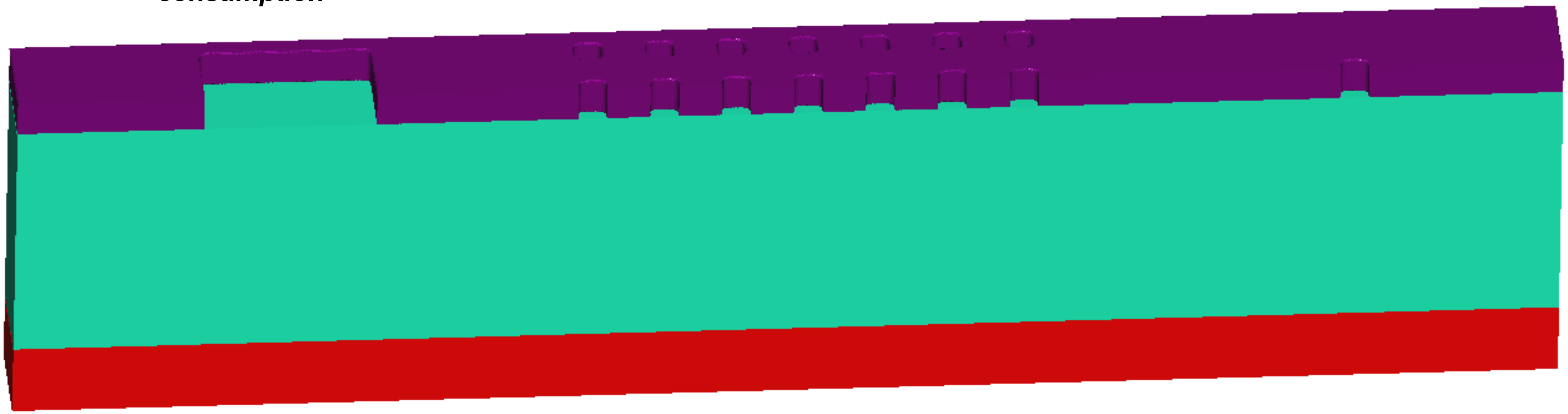
Spacer Etches



TFMHM M2 Overetch

Pattern Dependence

- Models account for multiple pattern-dependent effects:
  - Aspect Ratio Dependent Etching (ARDE), RIE Lag, etc.
  - Pattern Density effects: Isolated vs. Nested features
- Works with Basic Etch and MultiEtch process models
- Pattern Dependence feature enabled in Advanced Modeling Package
- Calibration "Wizard" included to make parameter input simple



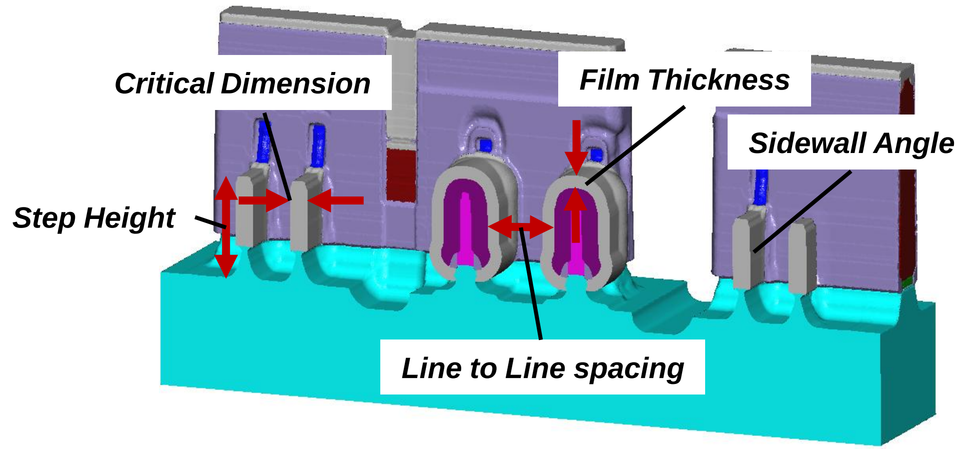
Automation

Virtual Metrology Operations

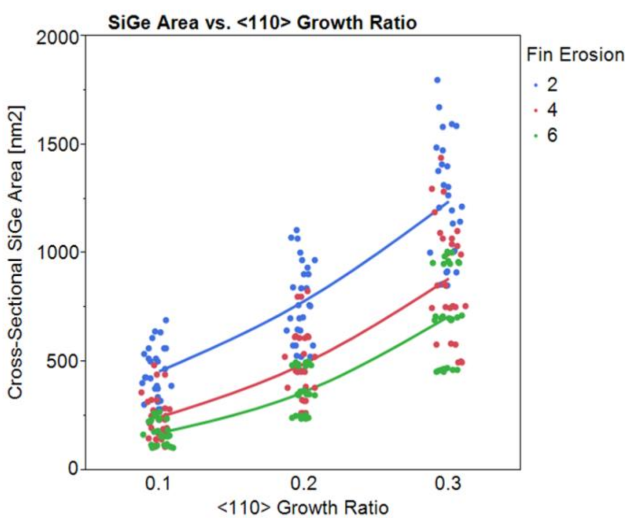
- Automate in-line, local measurements of critical technology parameters
- Mimic real in-fab metrology
- Replace slow out-of-fab destructive characterization

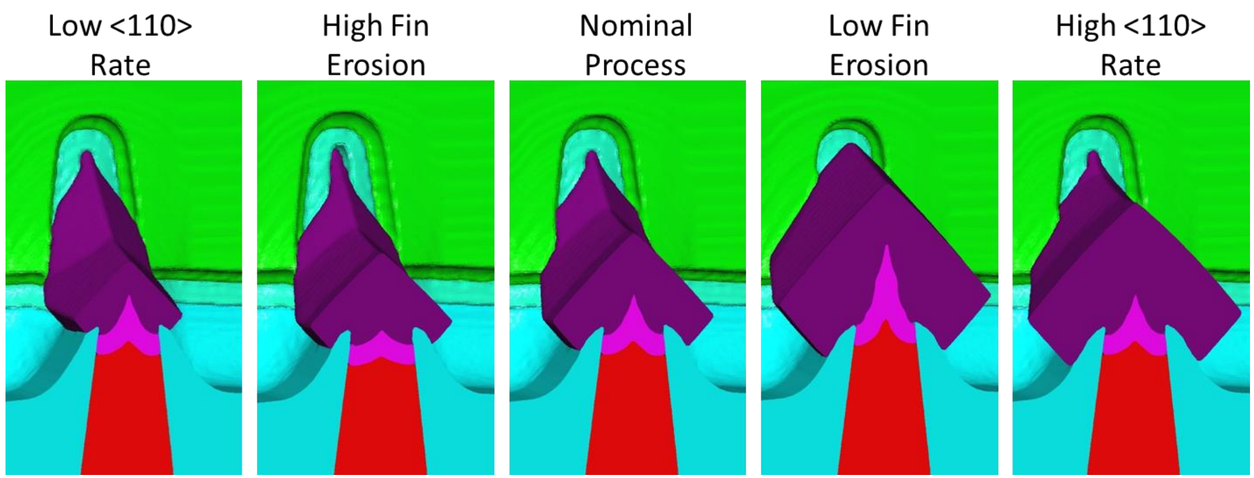
Expeditor batch processing tool

- Automated, spreadsheet-driven massively parallel parameter studies



Virtual Metrology measurement options





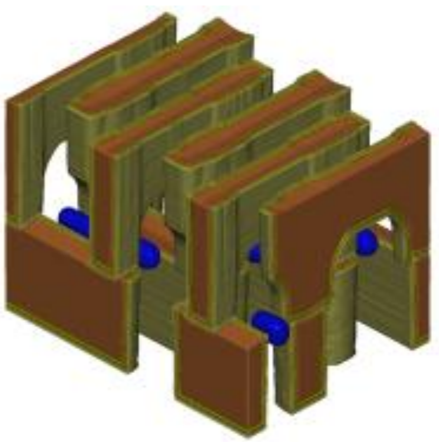
Example: DOE study on FinFET Epitaxy on <100> notched wafer: Dependence on pre-epitaxy fin erosion and epitaxial conditions

Structure Search

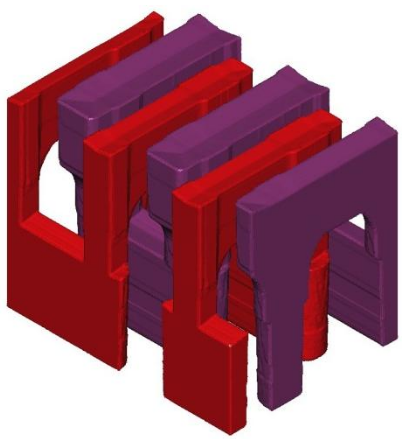
- Virtual Metrology makes a measurement at a specific location.
  - Virtual Metrology was released in SEMulator3D 2013

- Structure Search **FINDS** specific criteria, anywhere in the model:
  - Location of minimum spaces, line-widths, thicknesses
  - Number of electrical nets (opens/shorts)
  - Location of minimum material interfaces

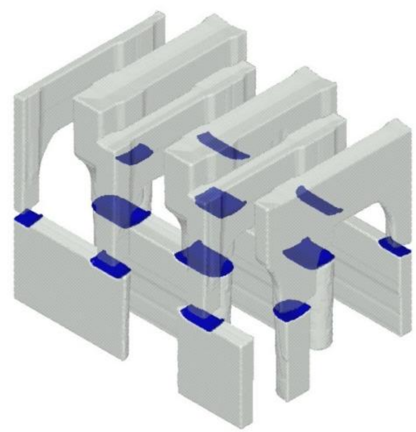
48nm Pitch Back End of Line (BEOL) Example



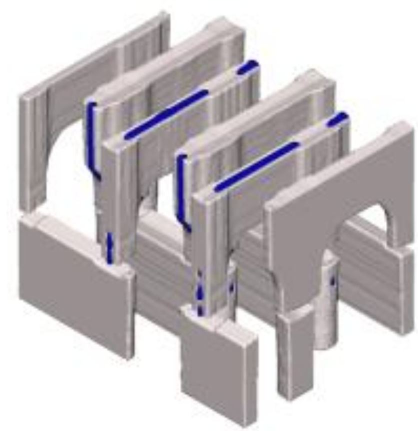
Minimum Insulator



Net ID and Count

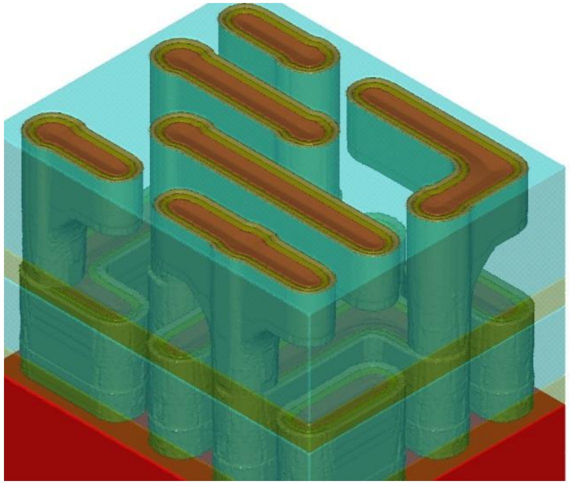


V1-M2 Contact

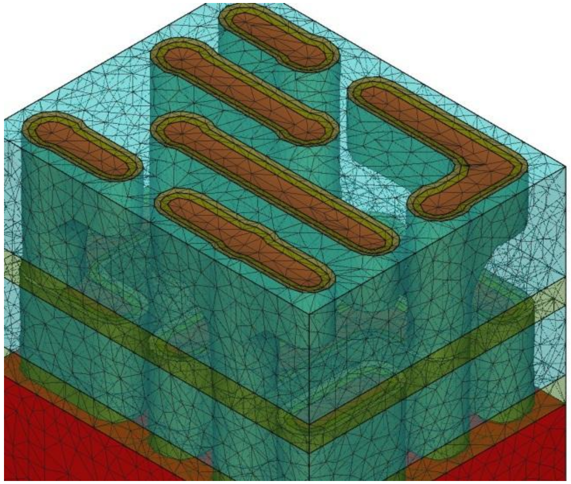


Minimum Cu Width

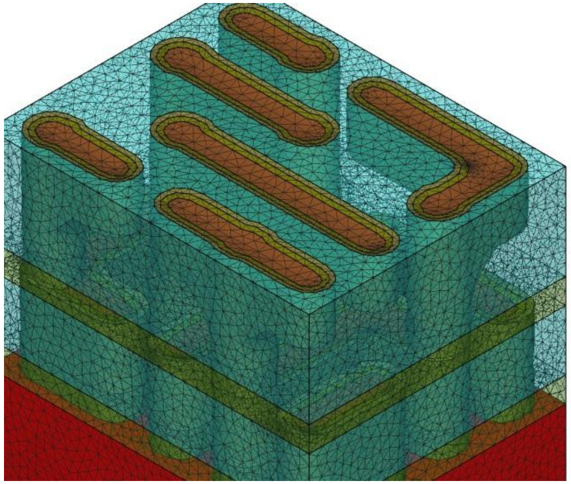
Meshing Module



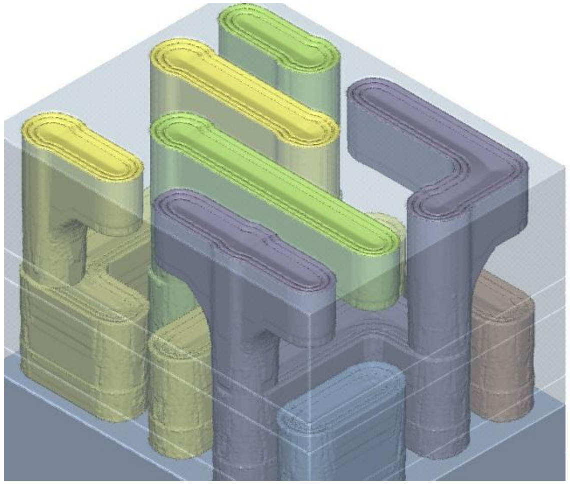
(1) SEMulator3D Material View of 64nm BEOL



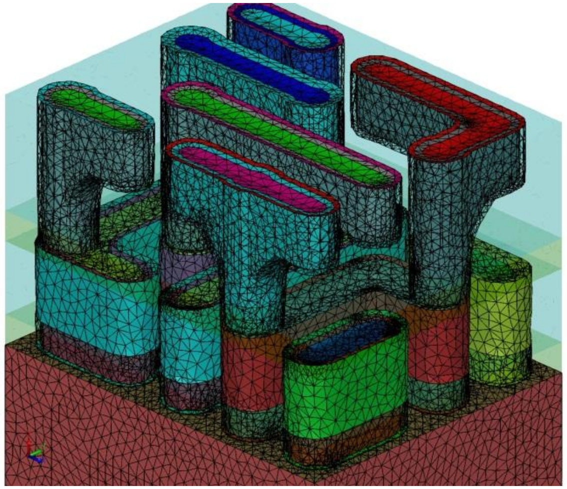
(2) SEMulator3D Initial Mesh



(3) SEMulator3D Refined Mesh



(4) SEMulator3D Electrical View of M1-V1-M2 Demo Build (5 nets)



(5) CoventorWare View of Imported Volume Mesh

Capacitance Matrix (pF)

	e0	e2	e1	e4	e3
e0	2.047833E-01	-1.269798E-01	-1.425979E-02	-5.969643E-02	-3.847307E-03
e2	-1.269798E-01	1.593481E-01	-2.344749E-03	-2.762691E-02	-2.396648E-03
e1	-1.425979E-02	-2.344749E-03	4.707713E-02	-2.908871E-02	-1.383876E-03
e4	-5.969643E-02	-2.762691E-02	-2.908871E-02	1.563615E-01	-3.994943E-02
e3	-3.847307E-03	-2.396648E-03	-1.383876E-03	-3.994943E-02	4.757723E-02

OK

(6) CoventorWare Capacitance Matrix Solution

Meshing allows use of realistic structures for electrical modeling

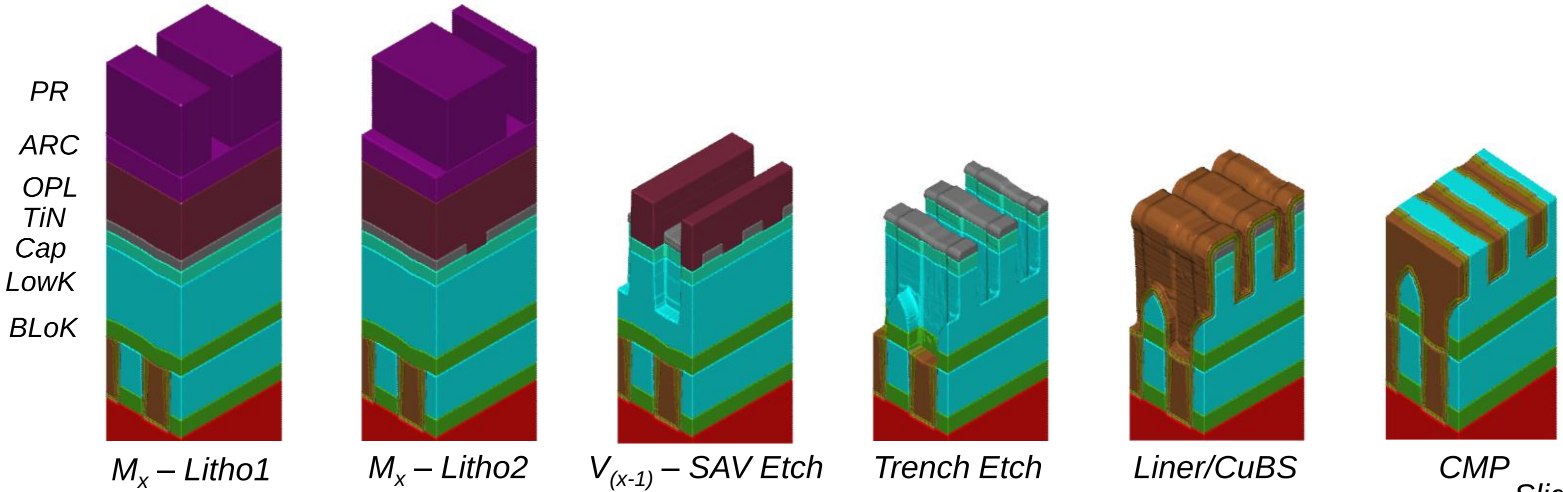
BEOL Development

Obvious: BEOL processes are pushed to the limit at 14nm

New patterning schemes to achieve density.
New metallization schemes for yield and reliability.

BUT…

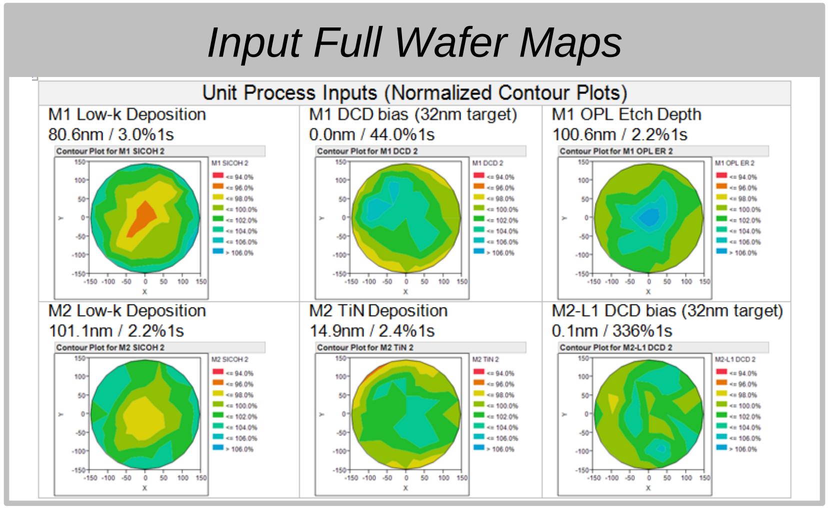
1. High aspect ratio integration challenges
2. Variability becoming larger portion of nominal dimensions
3. Parasitic R/C trade-offs driving hierarchical BEOL
4. Next-node BEOL scaling remains non-trivial

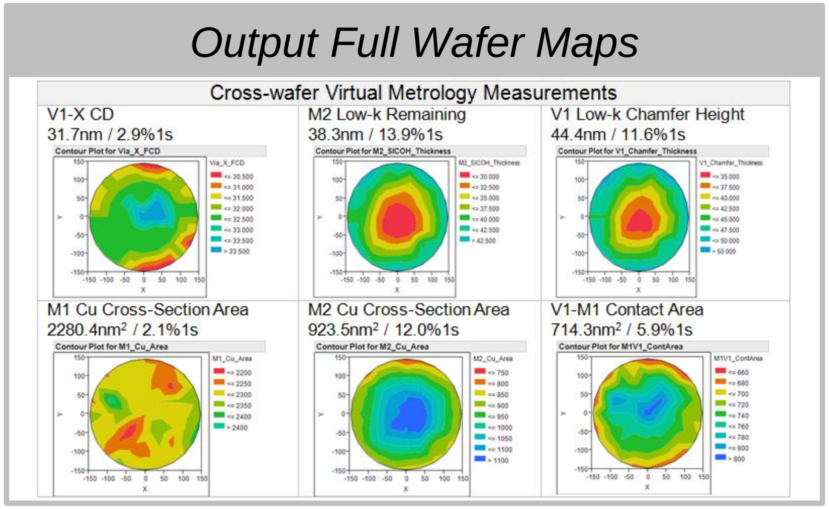


Cross-Wafer Uniformity

- Unit process cross-wafer behavior is easily validated from inline metrology
- The cross-wafer **requirement** is integrated and electrical
  - Costly & time-consuming to verify on HW
- Typical practice involves individual process optimization, driving toward a "flat" profile for all processes
- SEMulator3D provides a predictive methodology for evaluating integrated structural results (using virtual metrology) due to multiple forms of variation across the wafer (using Expeditor)
  - Process Co-optimization
  - Intelligent APC

At 450mm, the cross-wafer effects will dominate, and new methodology will prevail





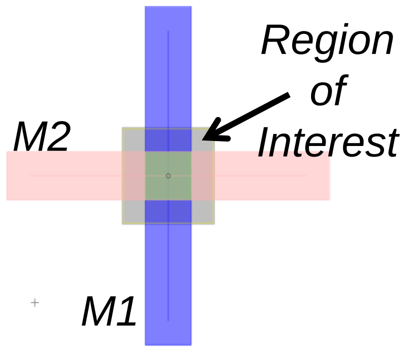
Design Awareness

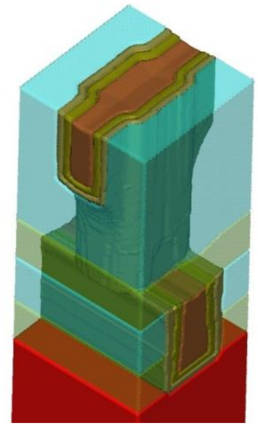
SEMulator3D models are the intersection of design and process

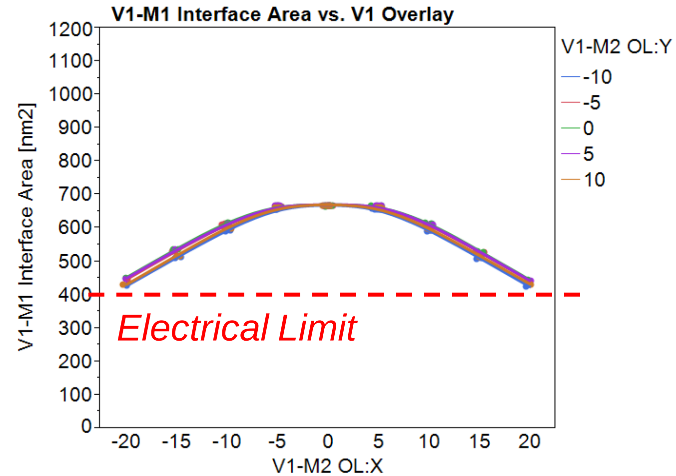
Integrated structural response to variations of multiple processes is now impossible to calculate with historical methods due to process complexity

Different designs respond to process variations differently

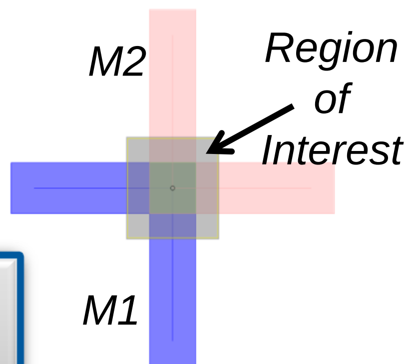
Virtual fabrication enables thorough investigation of design-process interaction

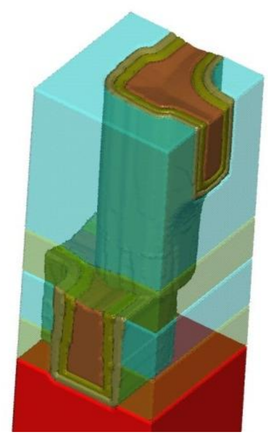


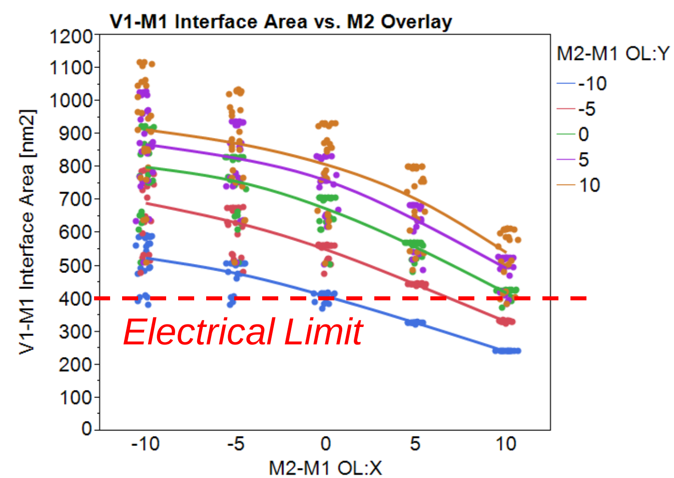




Design → Model → Data







Design → Model → Data

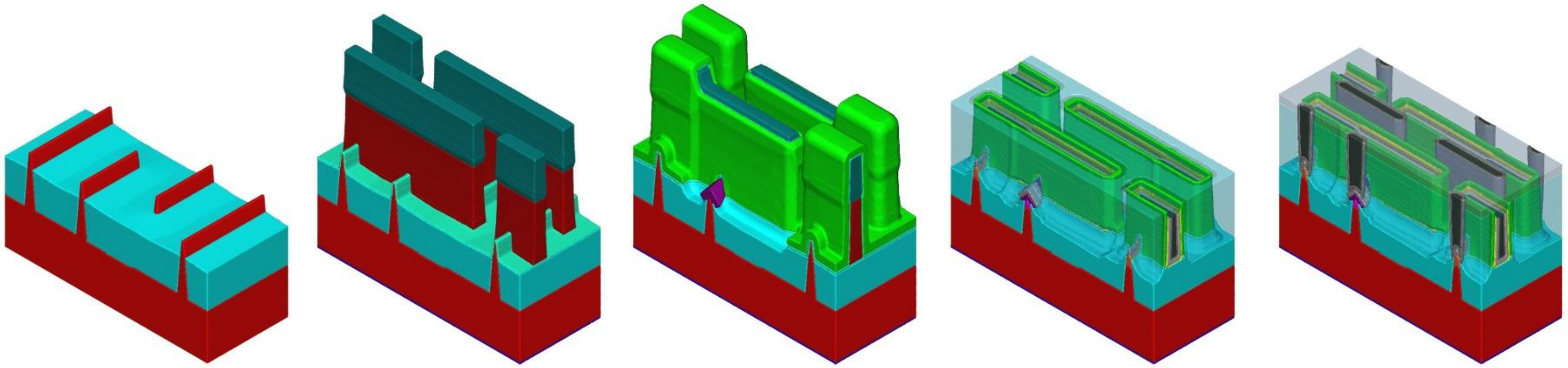
FinFET Development

Obvious: FinFET is the transistor architecture for the future of CMOS

Sub-threshold slope from double-gate structure improves power-performance

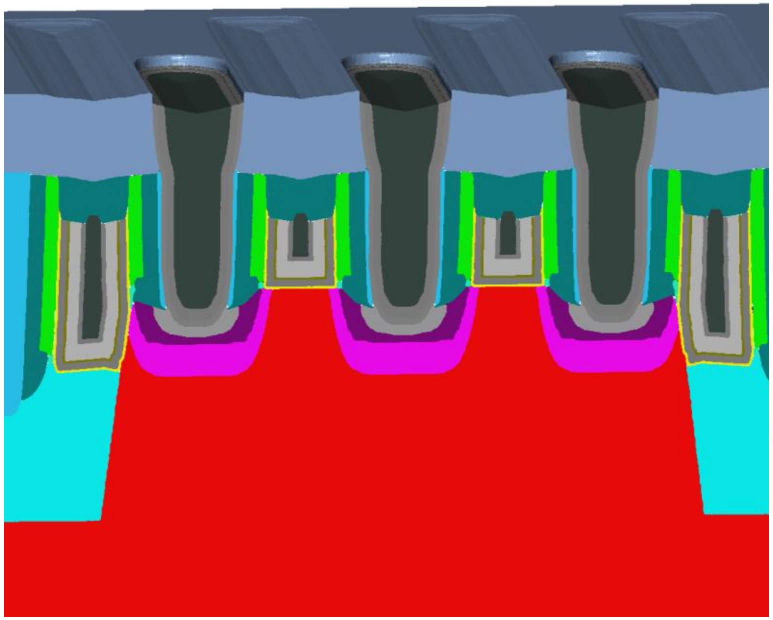
BUT…

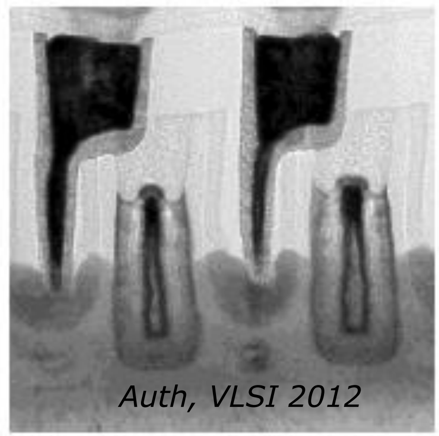
1. 3D structural integration challenges
2. New variability sources: Body thickness/shape, epi, MOL, etc.
3. New parasitic R/C trade-offs
4. Next-node FET scaling remains non-trivial



Fin/STI *Sacrificial Gate* *Spacers/Epi* *Metal Gate* *Middle of Line*

MOL Variation Analysis

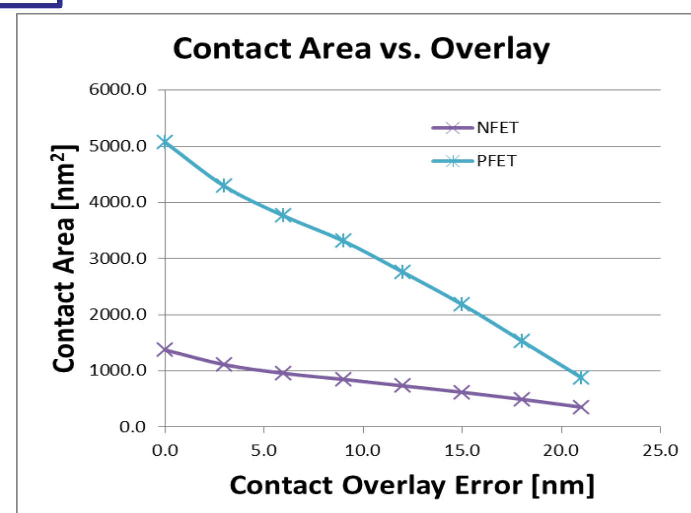




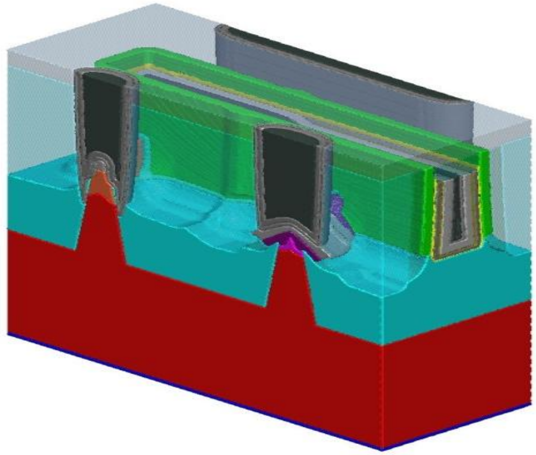
Example
Self-Aligned Contact
Overlay Variation

- *Predictive process deck built using public TEMs*
- *Variation analysis using Expeditor batch tool*

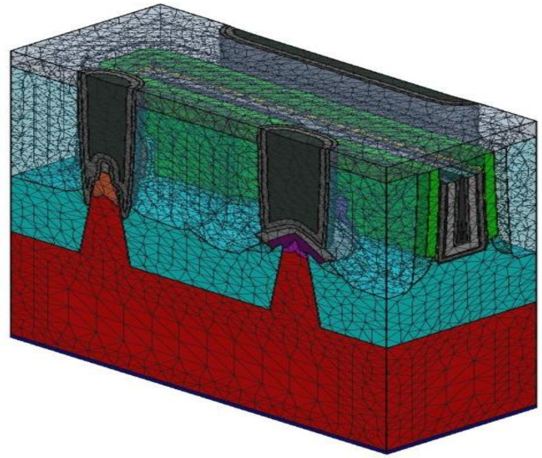
- *Virtual Metrology extracting 3D interface surface area – would require out-of-fab destructive characterization*
- *Physical parameter serves as electrical sensitivity for resistance or reliability criteria*



FEOL Parasitic Extraction



(1) SEMulator3D Material View of FinFET FEOL



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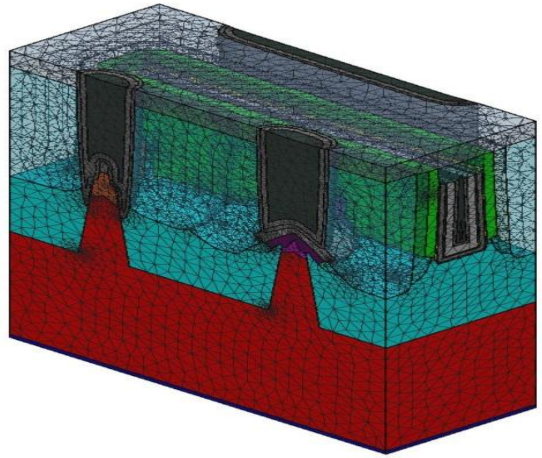
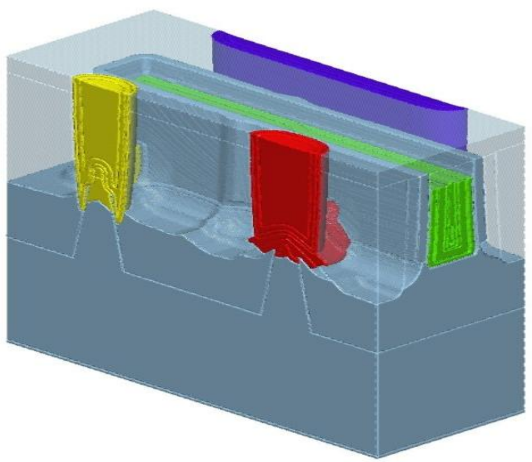
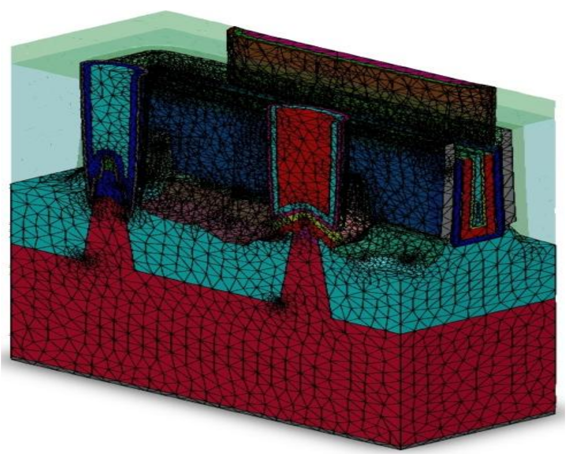


(3) SEMulator3D Refined Mesh



(4) SEMulator3D Electrical View of FinFET FEOL Demo Build (4 nets)



(5) CoventorWare View of Imported Volume Mesh

Capacitance Matrix (pF)

	Com	Gate	nSrc	pDrn
Com	8.910255E-02	-8.460155E-02	-2.303559E-03	-2.197076E-03
Gate	-8.460155E-02	1.549899E-01	-2.425009E-02	-4.613861E-02
nSrc	-2.303559E-03	-2.425009E-02	2.737773E-02	-8.242907E-04
pDrn	-2.197076E-03	-4.613861E-02	-8.242907E-04	4.916014E-02

OK

(6) CoventorWare Capacitance Matrix Solution

Meshing allows use of realistic structures for electrical modeling

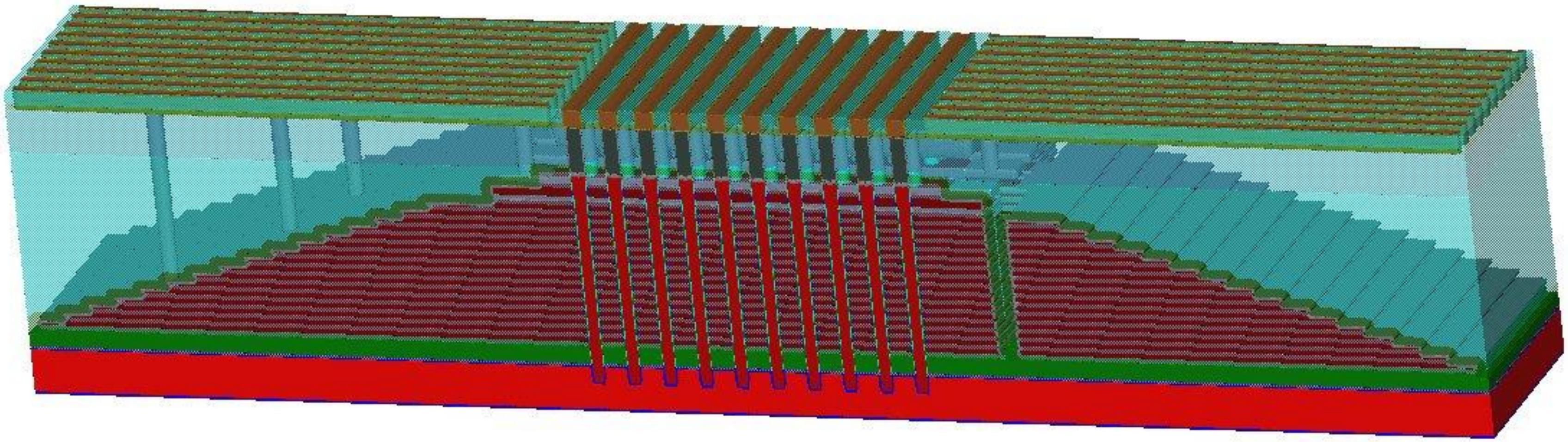
Memory Development

Obvious: Cost/bit NVRAM scaling has introduced *CRAZY* 3D structures

Vertical bit-line integration, multi-layer integration, etc.

BUT…

1. High aspect ratio integration challenges
2. Defects in multi-layer stack have wide-ranging implications
3. Further scaling drives more layers… really?!?!?!



Macro- vs. Micro-

Macro-scale – *Example: Overall Integration*

Large multi-regional structure
Complex multi-module integration

Modeling:

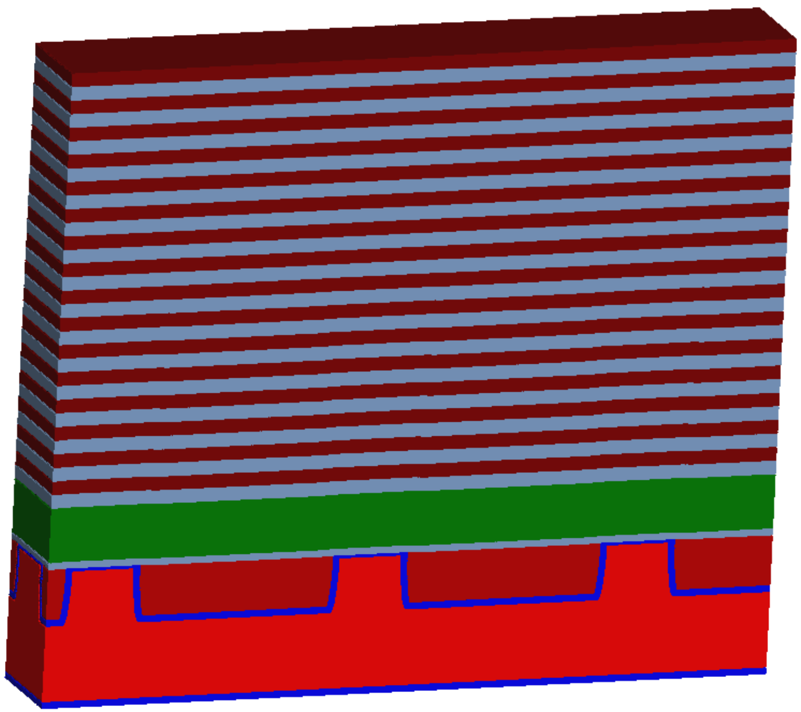
Large layout area selection
1.0 nm resolution
Basic Etch Model

Micro-scale – *Example: Plug Etch/Fill*

High aspect ratio etch
Multi-layer cyclic etch process
Profile details are critical

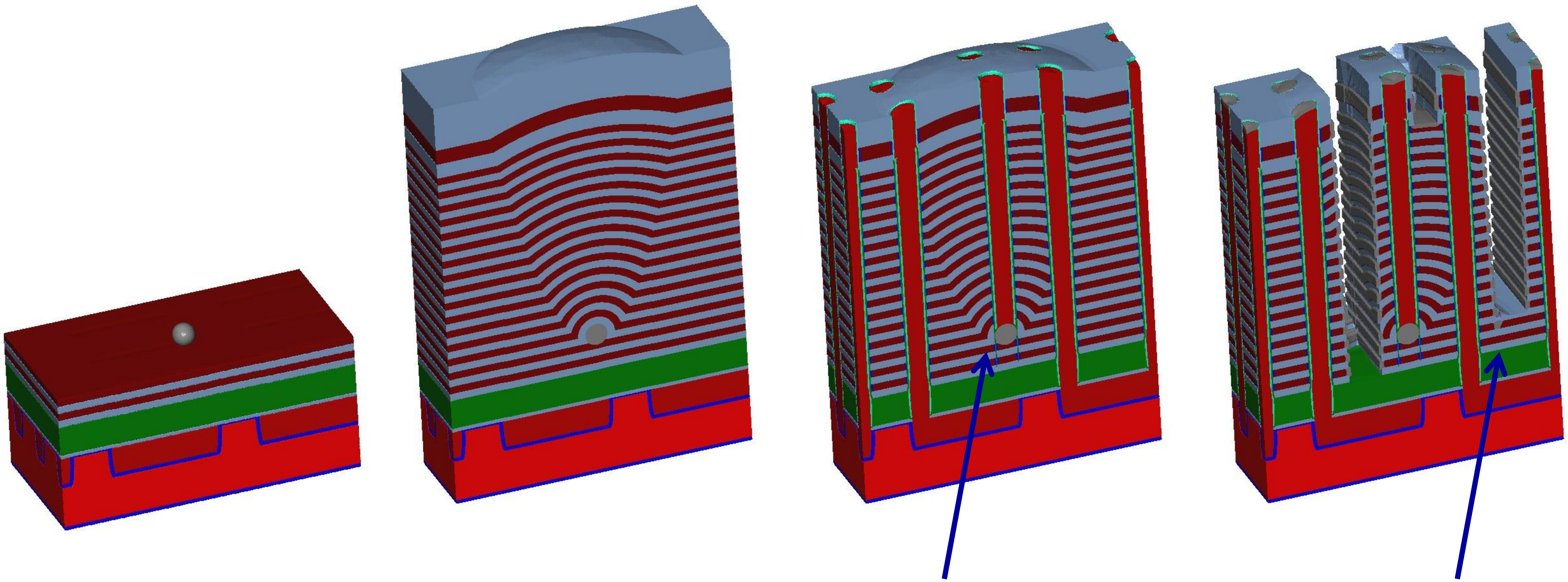
Modeling:

Layout area subset
0.5 nm resolution
Advanced Etch Model



SEMulator3D offers simple flexibility to explore different scales of physical challenges at high speed

Defect Evolution



60nm metal defect embedded during early phases of multi-layer stack deposition

Defect "magnification" through remainder of stack deposition

Defect blocks "plug etch", kills one bitline (expected). Plug module is robust enough for nearby bitlines to survive, despite non-planarity

Non-planarity affects "slit etch" later in flow. Results in underetch and shorted control gates. Kills entire sub-array block. ***NOT EXPECTED!!!***

SEMulator3D enables defect evolution understanding for yield ramp calculation and optimization

A Virtual Learning Cycle

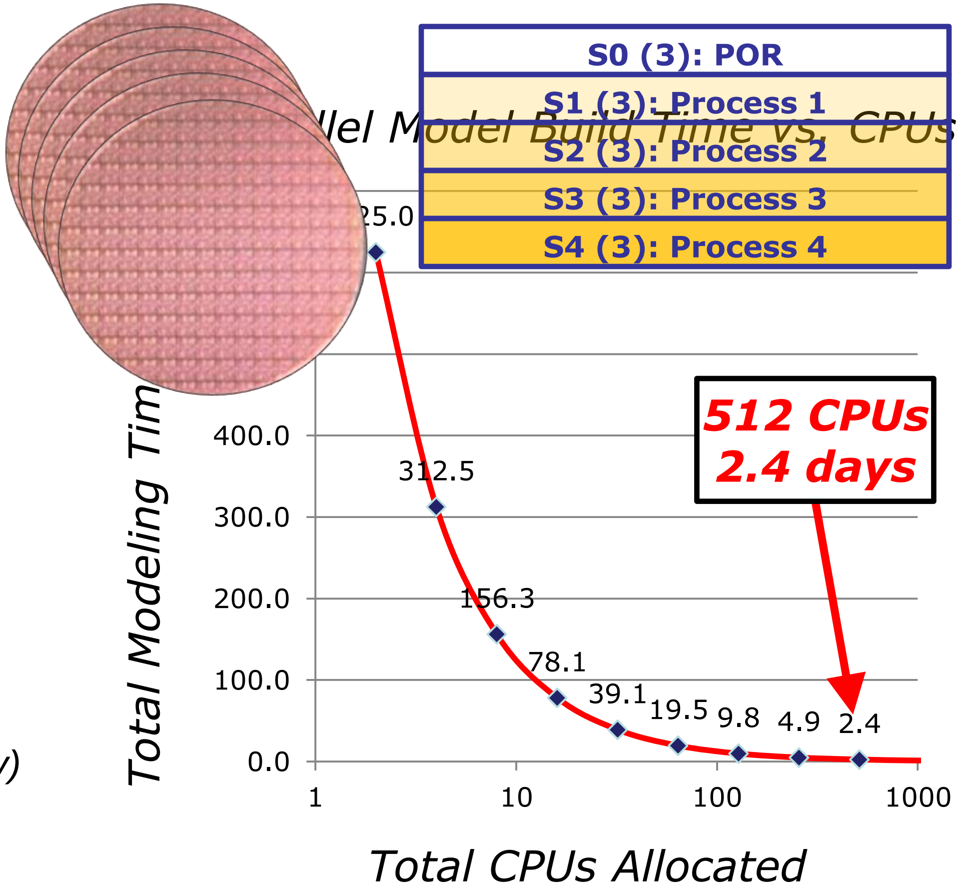
Utilize parallel computing infrastructure to dramatically accelerate development!

Silicon Cycle of Learning:

- *Wafers: 40 WSD * 3 months*
  - *150 5-way Experiments*
  - *All subject to variation*
  - *All captive to other processes*
- *Characterization: Additional Resource*
- *Analysis: Additional Resource*
- *Cost ~ $50M*

Virtual Cycle of Learning:

- *150 **Isolated** 5-way Experiments*
- *30 minute model build*
  - *High Resolution (~5A)*
- *20 designs: Key Library Elements*
- *Characterization: Built-in (Virtual Metrology)*
- *Analysis: Pre-processed (Expeditor)*
- *512 CPUs (4 CPUs/case): 2.4 days*



COVENTOR

Conclusion

- Advanced process technologies require Virtual Fabrication
  - Process complexity will impact Logic, SRAM, DRAM, Flash, etc.
- Process development in SEMulator3D saves time, money and development resources
- SEMulator3D Virtual Fabrication = **more than visualization**:
  - Cross-wafer process uniformity optimization and APC
  - Process centering conditions and sensitivity analyses
  - Meshing for electrical analysis such as Parasitic Extraction
  - Process corner analysis and design-process interaction sensitivities
  - Defect evolution exploration and yield-ramp optimization
- SEMulator3D capabilities benefit all semiconductor user groups:
  - Technology Developers: IDMs and Foundries
  - Fabless: Foundry Interface, IP Validation, DFM
  - Equipment/Process: Process co-optimization, APC, Integration context

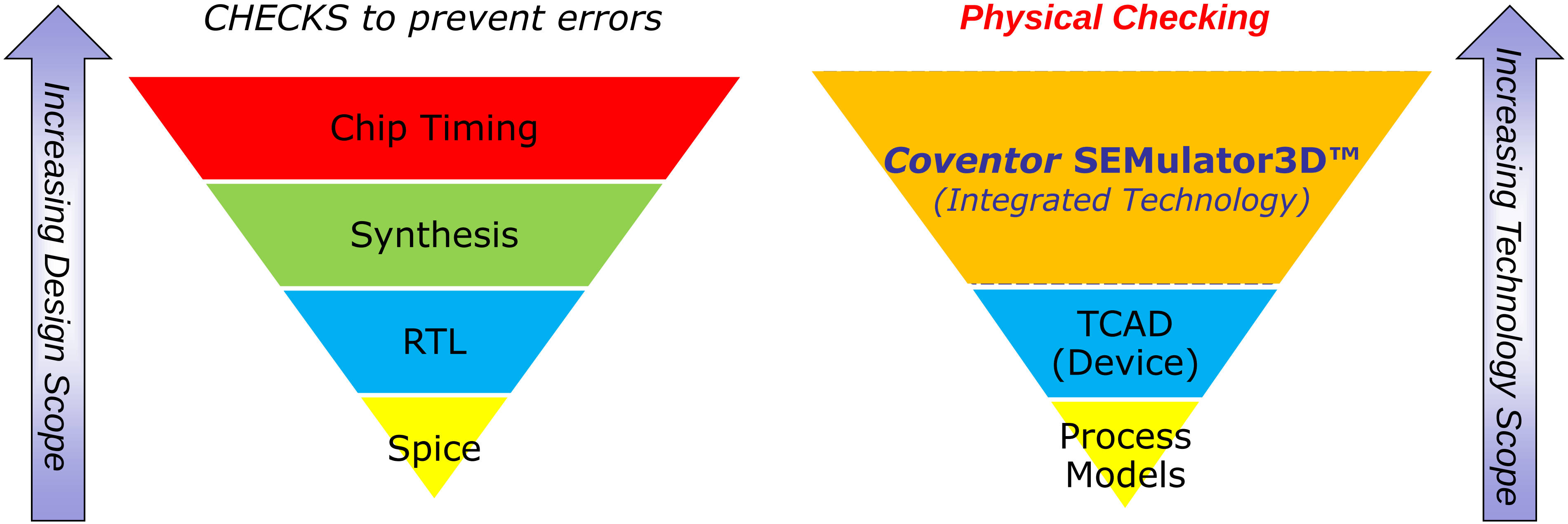
Thank you for your time

Backup Charts

The Analogy to EDA

Electronic Design Automation:
Hierarchical for all levels of design
Built for SPEED
CHECKS to prevent errors

Technology Development:
Hierarchical
Built for Speed
Physical Checking



Technology and Manufacturing dominates Design in the cost structure of semiconductor products, yet the Design community still leads in modeling infrastructure!

Abstraction

<u>Equipment Parameters:</u>
Process Gas Flows
RF Plasma Energy
Chamber Pressure
CMP Downforce
etc.

UNIT PROCESS MODELING

↓

UNIT PROCESS RESULT

*These results can not be combined to produce overall **integrated** result across designs in a timely manner*

<u>Behavioral Parameters:</u>

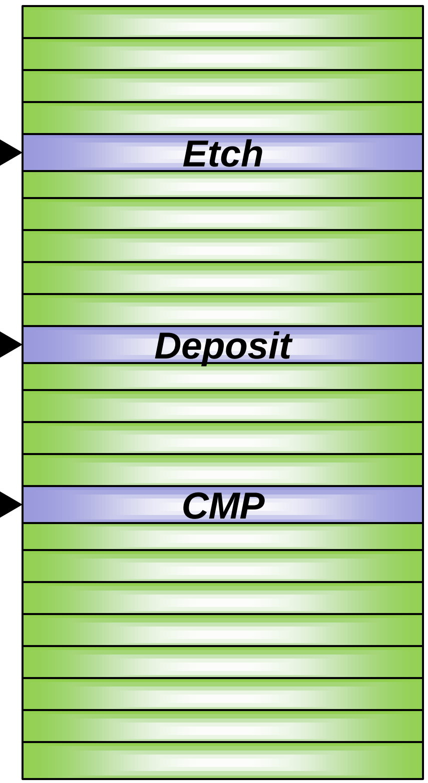
Etch:
Depth
Lateral Ratio
Selectivity
(Sputtering Ratio)
(Plane Dependence)
(Pattern Dependence)

Deposit:
Thickness
Conformality
(Visibility-Limited)

CMP:
Stopping
Overpolish
(Dishing Depth)
(Dishing Lateral Decay)

Many other processes

SEMulator3D



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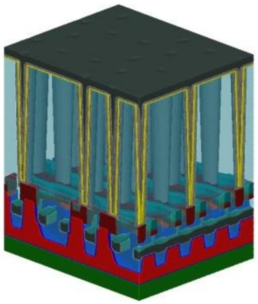
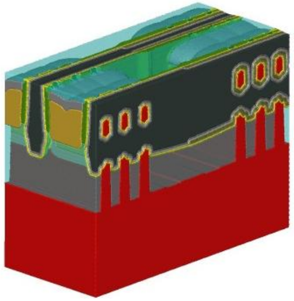
INTEGRATED RESULT

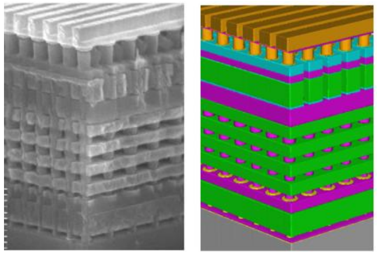
Continuum of Accuracy



$4F^2$ BWL DRAM



GAA Si Nanowire



3D NAND Flash

Accuracy & Detail – Development Timeframe

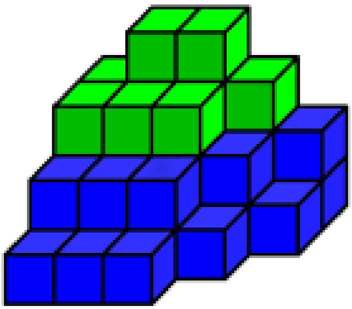
Proprietary Model: Iterative
Perfect for complex predictive problems

Calibrated Model: Based on existing HW data
Perfect for IP validation, parasitic extraction, flow optimization

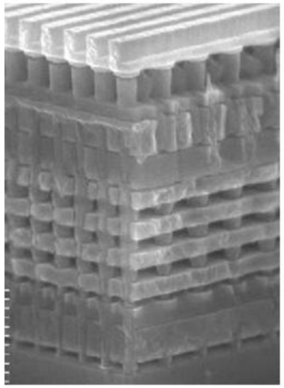
Realistic Model: Basic process knowledge, improved geometric accuracy
Perfect for design-technology co-optimization, flow development, testsite structure identification

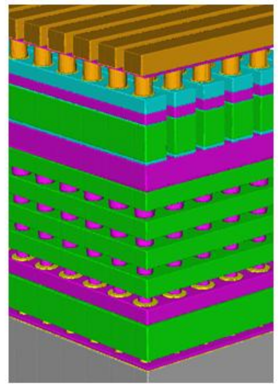
Basic Structural Model: Simplistic depositions and etches, no process details
Perfect for startup integration definition, process visualization, documentation, generated mask verification

Unique 3D Modeling Technology



Voxel Model



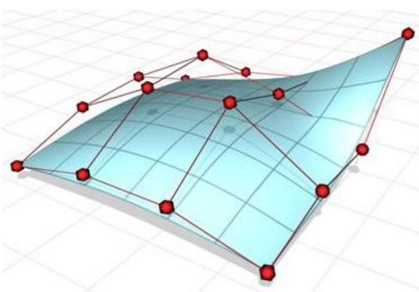


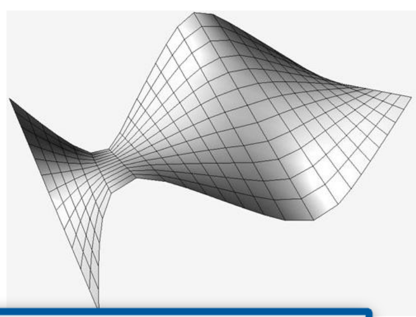
Other Process Modeling Tools

- Based on either BREP or moving mesh technology
- Surfaces are modeled with mathematical equations or discrete polygons
- Works for simple, well-defined models
- Fail or become unreliable for very complex topology common in Semiconductor devices

Voxel Modeling (SEMulator3D)

- Voxel = 3D Pixel
- Created for high performance
  - Medical Imaging, Semiconductor Modeling
- SEMulator3D modeling technology is proprietary, unique and patented
- Unlike other 3D modeling tools, SEMulator3D is very tolerant and *does not fail* due to small mask or model defects
- Ideal for arbitrarily complex 3D models





SEMulator3D is more reliable, accurate and faster than any other 3D process modeling tool

The Transformation is **NOW!**

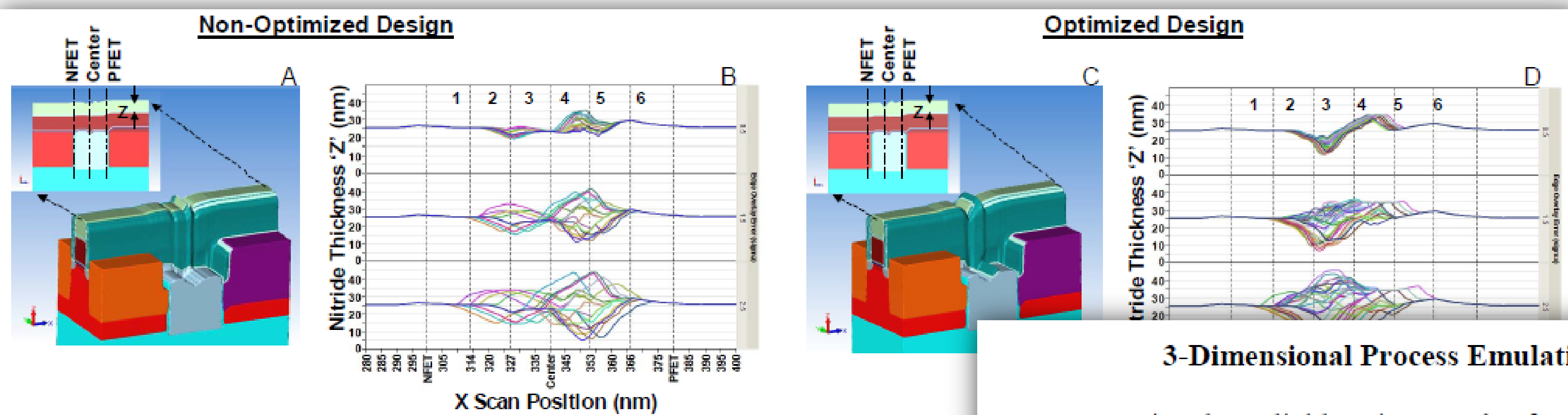


Fig 16. Coventor SEMulator3D Process Emulation Analysis showing (A) a 3D vie
Cap Evolution, (B) the variation analysis around this cap profile, (C) a 3D view of a
showing more controlled and centrally located residual cap. In Figures (B) and (D),
increasing total process tolerance.

3-Dimensional Process Emulation

Conventional salicide is used for gate/diffusion metallization. Prior to salicide, the gate cap film is removed using a simple RIE-based process, and does not require complex CMP. The gate cap is carefully engineered to maintain adequate coverage during S/D epitaxy without becoming elevated beyond the capability of the removal process. Coventor SEMulator3D™ process emulation software [13] was utilized to develop processes with manufacturing margin through the entire layout space. A variation analysis on two example integration schemes (Fig 16), presents an optimization of epitaxial protection versus cap removal simplicity.

(Narasimha, IEDM 2012)

IBM uses SEMulator3D to develop 22nm SOI Technology

Predictive Process Models

Virtual Metrology for Data Extraction

Batch Modeling for Variation Analysis

Parallelism for Cycle Time Reduction

The future of Computational Technology Development