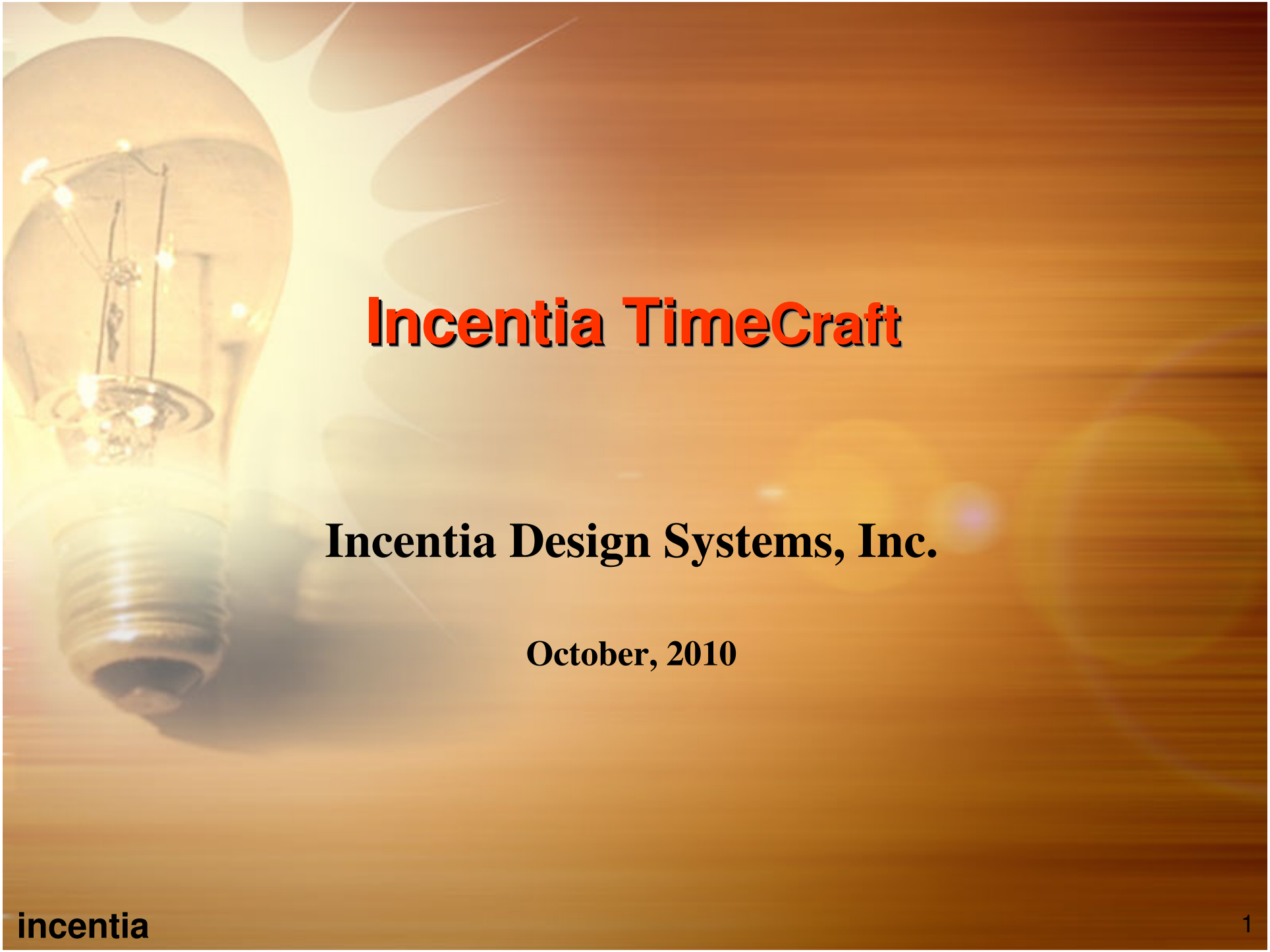


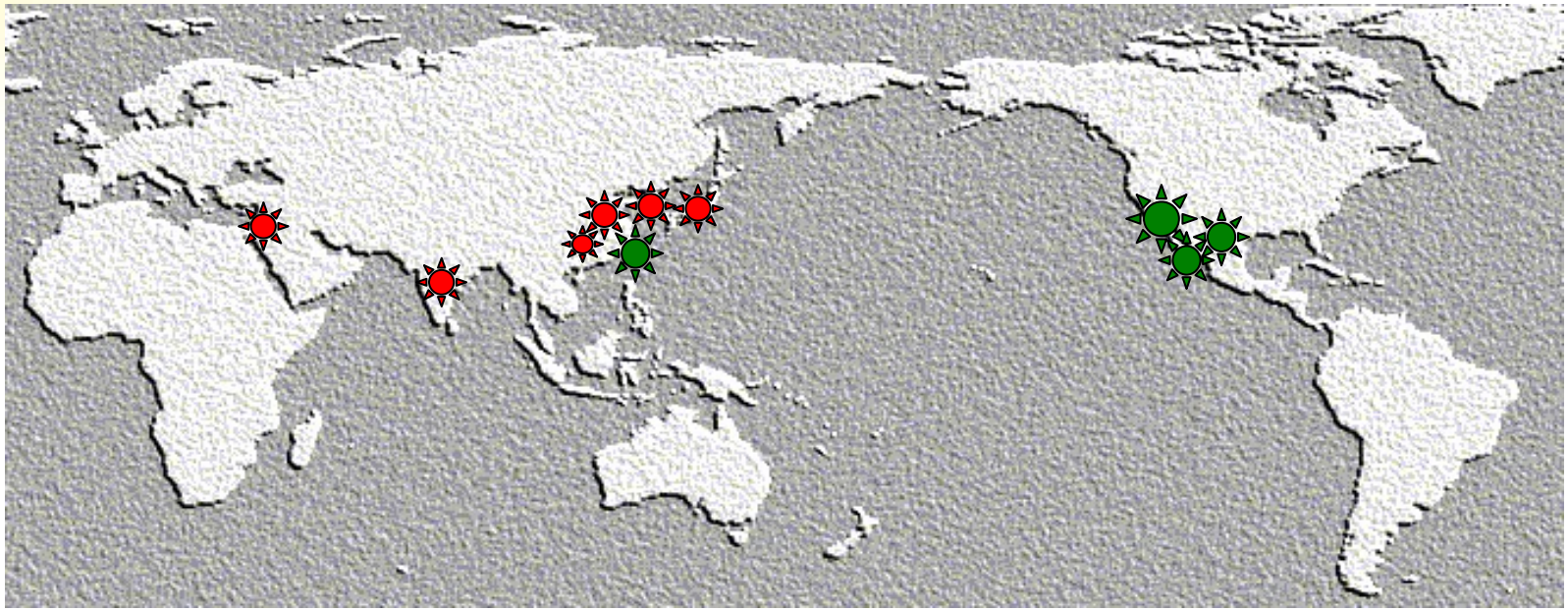
Incentia TimeCraft

Incentia Design Systems, Inc.

October, 2010

Company Introduction

- Mission: SoC nanometer timing and synthesis technology leader
- Channels



Direct Offices:
USA: Silicon Valley
Southern California
Taiwan: Hsinchu

Distributors:
Japan (Marubeni), India (ICON),
China (OnePass Solutions),
Korea (ED&C), Israel (AST)

Incentia Product Offering
"Fastest Timing Analysis & Design Closure"

- **Timing analysis solutions**
  - TimeCraft: High-speed, big capacity, signoff proven STA
  - TimeCraft-LOCV: Location Based OCV
  - TimeCraft-SI: Signal Integrity
  - TimeCraft-SSTA: Statistical STA
  - TimeCrfaft-PCA: Power Analysis
  - ConstraintCraft: Constraint Management
- **Design closure solutions**
  - ECOCraft-Power: Leakage Power ECO
  - ECOCraft-Timing: Hold-time and Setup-time ECO

Contents

- **Timing Analysis Solutions**
  - **TimeCraft**
    - TimeCraft-LOCV
    - TimeCraft-SI

TimeCraft Highlights

- Superior STA & SI performance
  - 2X – 3X faster than other tools
  - Less memory usage for big designs
- Proven signoff quality with hundreds of tape-outs
- Rich features
  - NLDM, CCS, ECSM
  - SDF & SPEF flows
  - IR-drop aware STA & SI
  - Voltage/temperature scaling
  - CPF/UPF support
  - LOCV
  - GRID/LSF based multi-task parallel MMMC
  - Multi-thread speedup
  - Variation tolerant clock: non-tree structure
  - Multi-voltage-frequency signoff
  - Advanced SI crosstalk pessimism reduction

TimeCraft Customer Examples

- Recent advanced customer tape-out cases
  - 2X to 3X faster than competitors' solutions

Designs	Complexity	Competitor	TimeCraft
Design 1 50+M logic gates (SDF, 65nm)	150+ clock domains 3000+ timing exceptions Very complex reporting	Runtime: 11.8 hrs (single-thread)	Runtime: 3.9 hrs 24% less memory (single-thread)
Design 2 30+M logic gates (SPEF+delta_SDF, 45nm)	170+ clock domains Multi-Vdd domains LOCV with dual clock/data derating	Runtime: 8.5 hrs (multi-thread)	Runtime: 3.1 hrs 11% less memory (multi-thread)
Design 3 30M gates (SPEF-SI, 40nm)	240+ clock domains Clock mesh, CCS library 100+ M coupling-cap	Runtime: 9.2 hrs (multi-thread)	Runtime: 3.7 hrs 16% less memory (multi-thread)

- Some on-going advanced big customer tape-outs
  - Around 100M gates

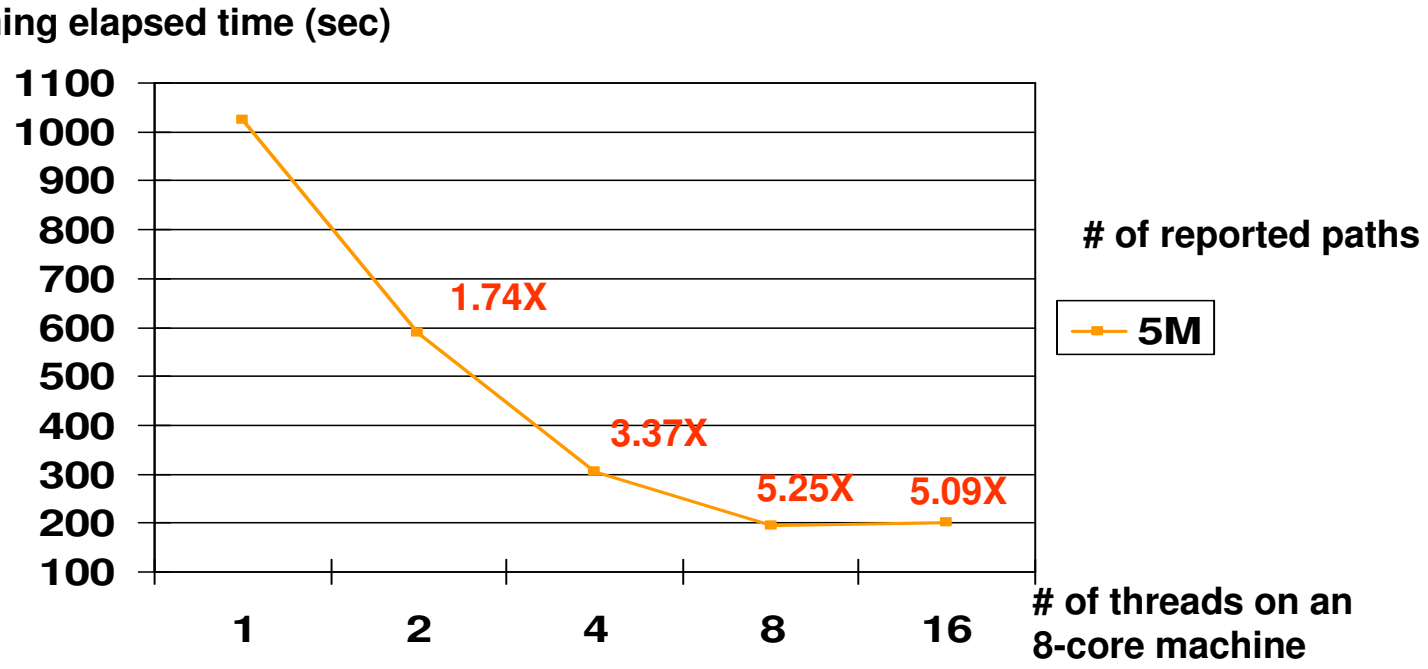
TimeCraft: Multi-thread Technologies

- Intra-command parallelism
  - Automatically performed
  - compile_spf, update_timing, check_timing, report_timing, get_timing_path, report_constraint, report_timing_coverage etc.
- Aggressive mode in big report generation
- Inter-command parallelism
  - Manually specify commands that can be performed in parallel
  - Command: *parallel*
- RESULT: Most aggressive multi-thread speedup
  - **2X to 5X over TC single-thread**

Multi-thread Aggressive Mode

- Aggressive mode for report printing
  - *report_timing –mt_aggressive_mode*
  - *report_constraint –mt_aggressive_mode*
    - Significant runtime improvement for large sized report file
    - Within 10% of memory increase

An example of a large report file containing 5M paths after report_timing



Inter-command Parallelism

- Command: *parallel*
- Parallel inputs
  - Multiple SDF imports
  - Multiple SPEF compilations

```
parallel {
read_timing –analysis_type on_chip_variation top.sdf
compile_spf –ocv_location only_pin –format spef top.spef
}
```

- Parallel outputs

```
parallel {
report_timing –nworst 100 –max_paths 1000
report_timing –begin_end_pair …
report_constraints …
}
```

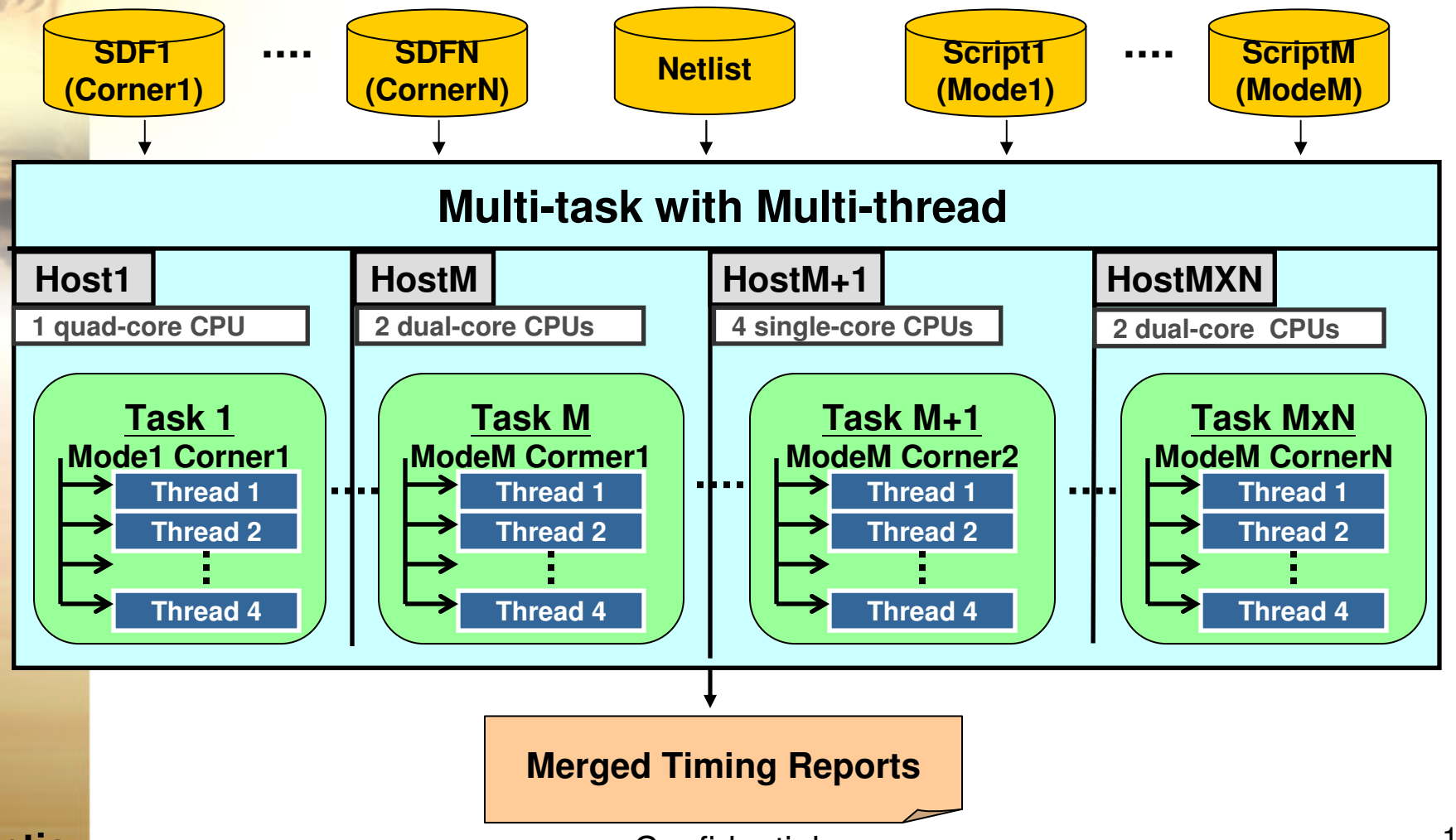
Multi-thread Speedup

- 2X to 5X speedup over single thread
- Example
  - Over 2.5X speedup using 4 cores and 3X speedup using 8 cores
  - Within 5% memory increase

	Single-core (Elapsed time)	4-cores (Elapsed time)	8-cores (Elapsed time)
Design & lib import	206s	209s	207s
SDC loading	40s	39s	40s
SDF + SPEF pin locations (1)	394s	216s	212s
14 misc. report commands (2)	1271s	394s	284s
LOCV setting	1s	1s	1s
6 report_timing commands (3)	836s	210s	163s
Total	2748s	1069s	906s
Speedup	1x	2. 57X	3.03X

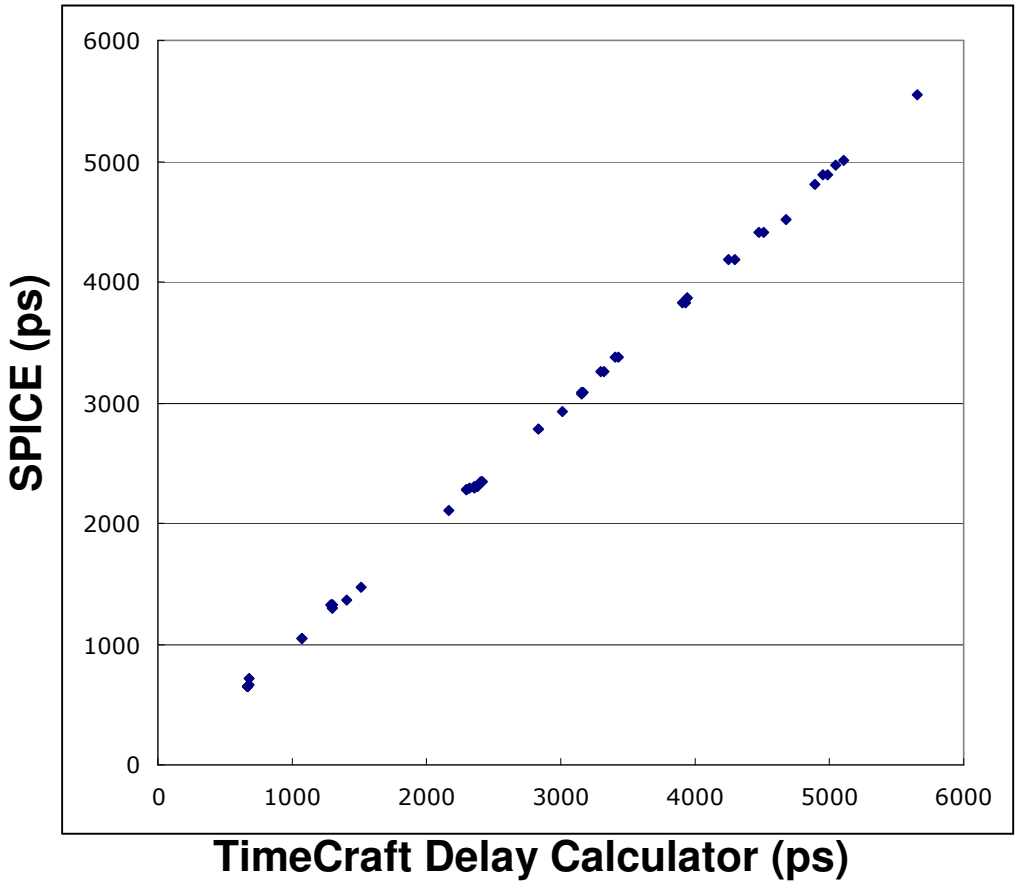
Multi-task with Multi-thread

- Multi-task: Submit MMMC jobs to network machines
- Multi-thread: Each multi-core machine runs TimeCraft-MT



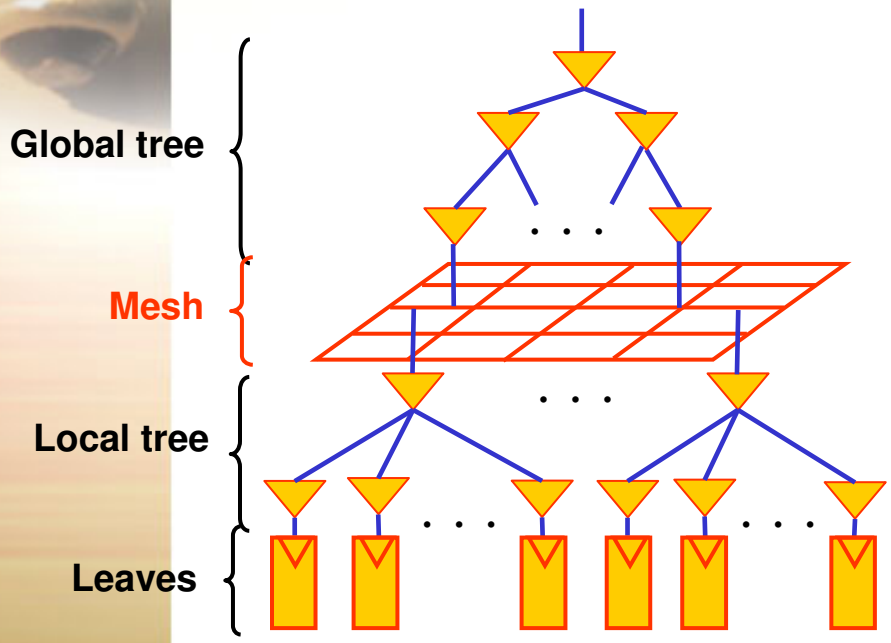
Incentia Delay Calculator Accuracy

- Path delay accuracy (45nm customer cases)
  - Plot TimeCraft path delays vs. SPICE results: within 2%



Variation Tolerant Clock
Non-tree Clock Structures

- Non-tree clock structures, e.g. clock mesh
  - Reduce skew at leaf instances
  - Thus reduce number of corner runs

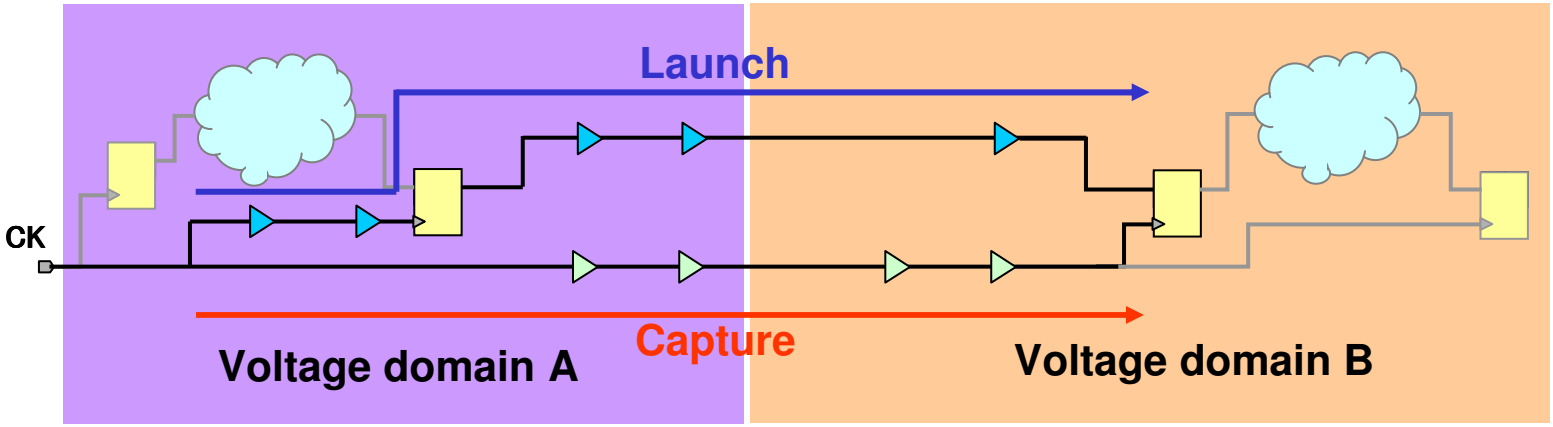


- Big customer clock mesh example
  - 1024 x 4096
  - Only solution satisfying desired accuracy & runtime
- Interface to output SDF/SDC
  - write_mesh_clock_interface

(Courtesy of Japan STARC)
Comparison to SPICE results
(1) Mesh in->out path delays: within 6%
(2) Clock skews are within 7 ps

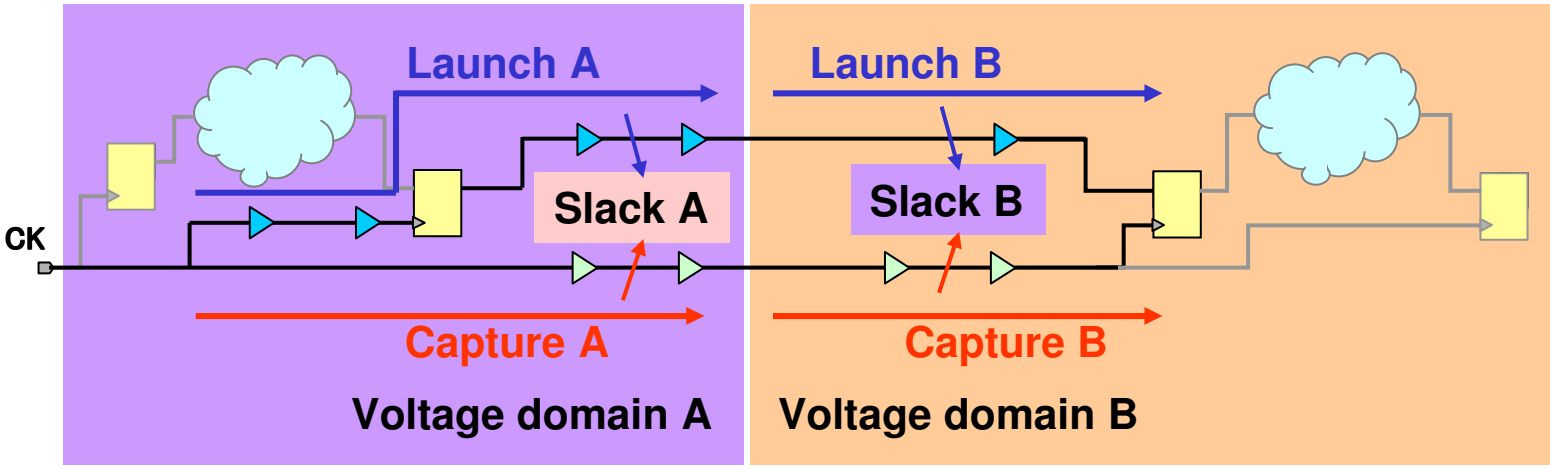
Multi-voltage-frequency STA
Inter Power Domain (IPD) Derating

- IPD timing analysis
  - Low power designs contain multiple voltage domains
  - Accurate STA needs to consider all voltage combinations
- Goal
  - Reduce multiple voltage-combination corner runs to 1
- Solution
  - IPD timing analysis & derating
  - Support both Graph based & Path based



IPD Timing Analysis: Path Based Example

- Analyze path segments based on voltage domains
  - In each voltage domain, if the slack is worse after applying the IPD derating factor
    => Apply the IPD derating factor
  - IPD derating table
    - Globa IPD derating factor
    - Cell-based IPD derating factors



Contents

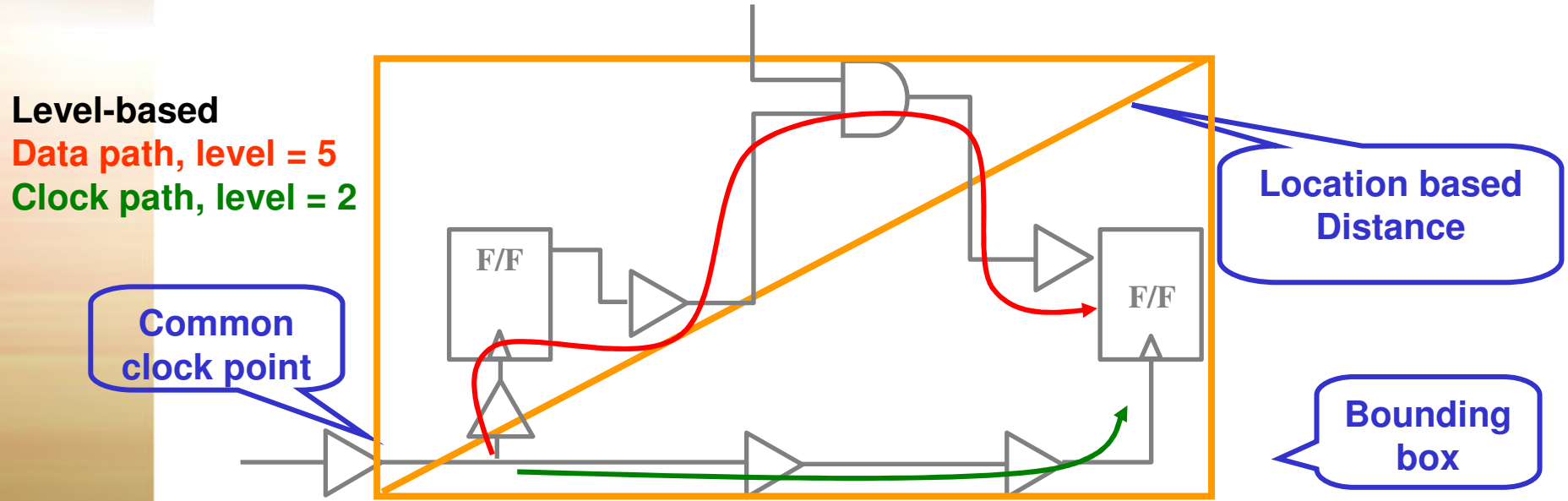
- **Timing Analysis Solutions**
  - TimeCraft
  - **TimeCraft-LOCV**
  - TimeCraft-SI

Advanced OCV (a.k.a. LOCV)

- Reduce over-pessimism timing analysis
- Consider variations using variable timing derating factors
  - Level (stage) based: random variations
  - Location (distance) based: systematic variations
- Rich features
  - Many fine-grain controls for further pessimism reduction
  - Native engine based: fastest runtime
- Many customer tape-outs in 90, 65, 55, 45, 40nm

Advanced OCV (a.k.a. LOCV) (Cont)

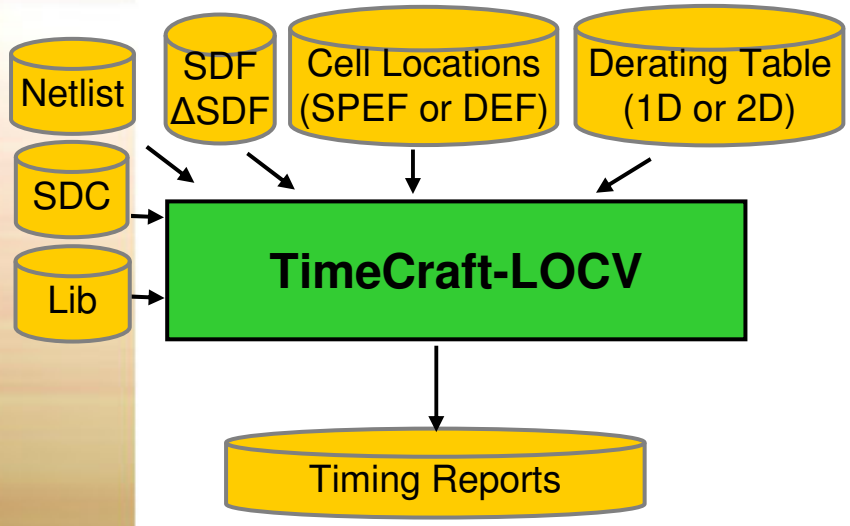
- Level (stage) based
  - Derating factor depends on path stages
- Location (distance) based
  - Derating factor depends on path locations: diagonal distance of bounding box



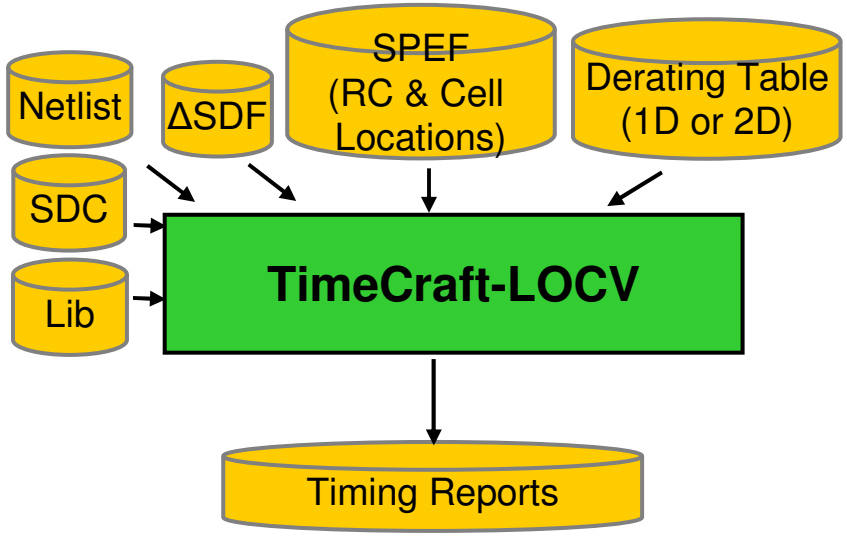
TimeCraft-LOCV Flow

- Usage
  - Level based (1D)
  - Level & Location based (2D)
    - Location information from SPEF or DEF

TimeCraft-LOCV SDF Flow



TimeCraft-LOCV SPEF Flow



TimeCraft-LOCV: Derating Table

- Level based: 1D table
- Level & Location based: 2D table
- Example: two-dimension table
  - X axis: Level (logic stage)
  - Y axis: Location (diagonal of bounding box)

MAX-Hold-Early

Distance	Stage 0	1	2	4	8	16	32
0	0.85	0.85	0.88	0.91	0.93	0.94	0.95
2000	0.85	0.86	0.88	0.90	0.93	0.94	0.95
8000	0.83	0.85	0.87	0.90	0.92	0.93	0.94
16000	0.82	0.84	0.85	0.89	0.91	0.92	0.93

MAX-Setup-Early

Distance	Stage 0	1	2	4	8	16	32
0	0.85	0.85	0.88	0.91	0.93	0.94	0.95
2000	0.84	0.84	0.87	0.90	0.91	0.93	0.95
8000	0.82	0.84	0.86	0.89	0.90	0.92	0.94
16000	0.81	0.83	0.85	0.88	0.89	0.91	0.93

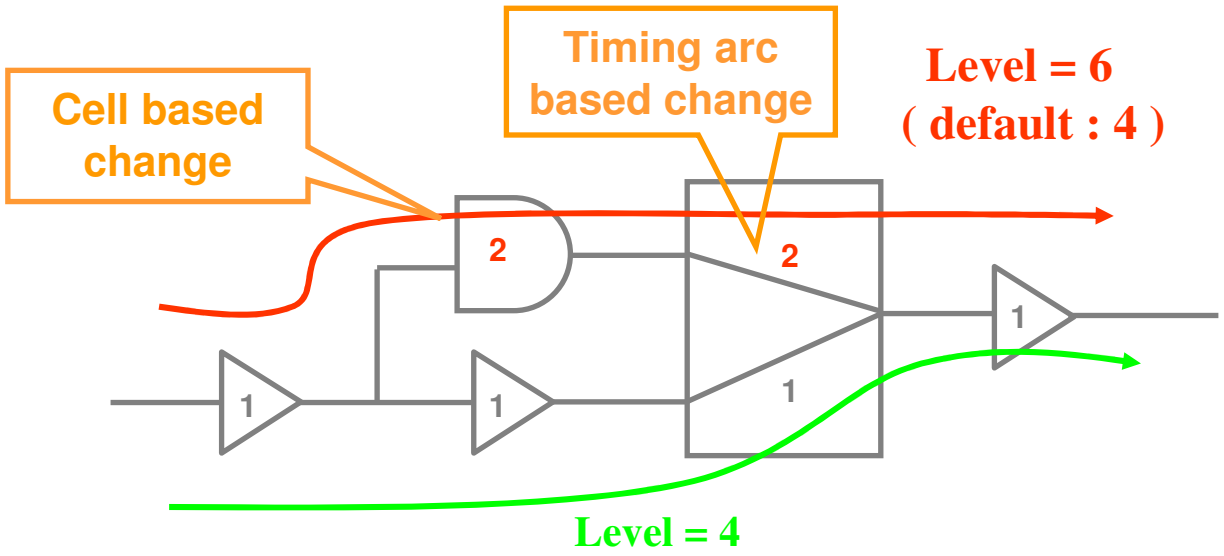
Max delays in SDF are too pessimistic; Compensate by factors less than 1

Longer distance means more systematic variations; Factors are farther away from 1

More logic levels means less random variations; Factors are closer to 1

Level-based OCV: Cell Level Control

- Fine-grain control on cell level counts
  - Default: 1 cell counted as 1 level
  - Cell based: larger count for more complicated cell
  - Timing arc based: larger count for longer cell timing path
  - Mode based: read/write mode in memory cell
  - Cell delay based: function of cell delay
- Mixture of variable and fixed deratings



TimeCraft-LOCV Benefits

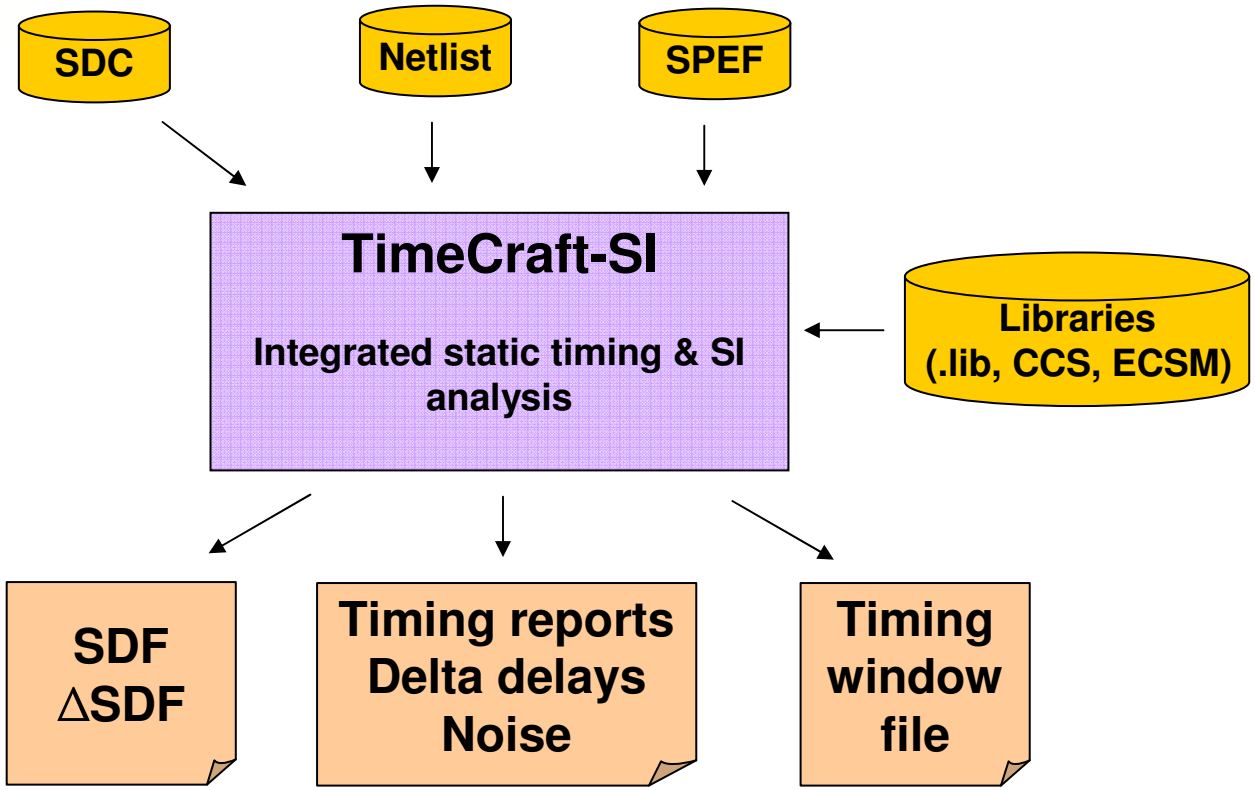
- Tape-outs prove advantages of TimeCraft-LOCV
  - Smaller WNS and fewer timing violations
  - Less conservative; easy to achieve timing closure
- Native-engine based
  - Very fast runtime speed!

Case Study (45nm)		Traditional OCV	Level-based OCV	Level & Location-based OCV
Setup	# Violations	582	318	83
	WNS	-0.675ns	-0.239ns	-0.01ns
	Runtime	1X	1.1X	1.3X
	Memory	1X	1.1X	1.2X
Hold	# Violations	3795	193	37
	WNS	-0.059ns	-0.023ns	-0.01ns
	Runtime	1X	1.2X	1.3X
	Memory	1X	1.1X	1.2X

Contents

- **Timing Analysis Solutions**
  - TimeCraft
  - TimeCraft-LOCV
  - **TimeCraft-SI**

TimeCraft-SI Flow



TimeCraft-SI Highlights

- Rich features
  - Support NLDM, CCS, and ECSM libraries
  - Cross talk delta delay analysis
  - Noise analysis
- Accurate analysis results: Within 5% of SPICE
- Very fast runtime, big capacity
  - 2X to 3X faster than other solutions
  - Multi-thread capability
- Advanced crosstalk pessimism reduction
  - Logical correlation in simple/complex gates
  - CRPR in cross talk
  - Discrete timing window

Cross-talk Analysis: Accuracy (Cont)

- CCS 45nm library
  - Mean value within 5% of SPICE
  - Standard deviation within 7%

Test case set 1 (900+ single-aggressor test cases)

	Typical	Slow	Fast
Mean	**1.0%**	**3.6%**	**-2.0%**
Std dev	**2.5%**	**5.8%**	**6.4%**

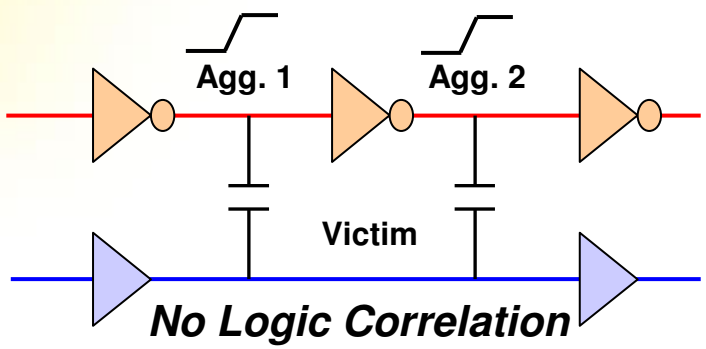
Test case set 2 (3000+ multi-aggressor test cases)

	Typical	Slow	Fast
Mean	**1.8%**	**3.3%**	**2.6%**
Std dev	**2.7%**	**5.2%**	**6.7%**

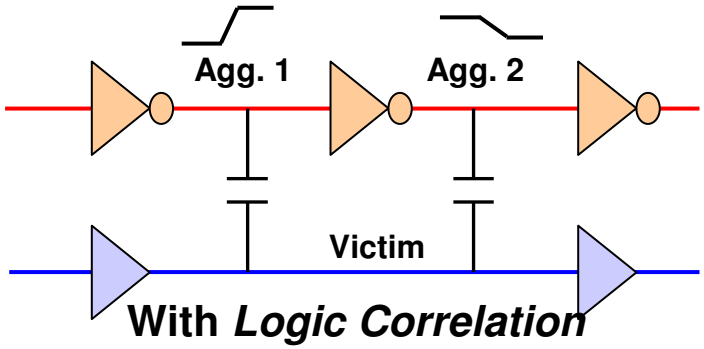
Courtesy of STARC for the data based upon TC 2009.12 version

SI Pessimism Reduction: Logical Correlation

- Too pessimistic assuming all aggressors switching at one direction
- Simple gate structure

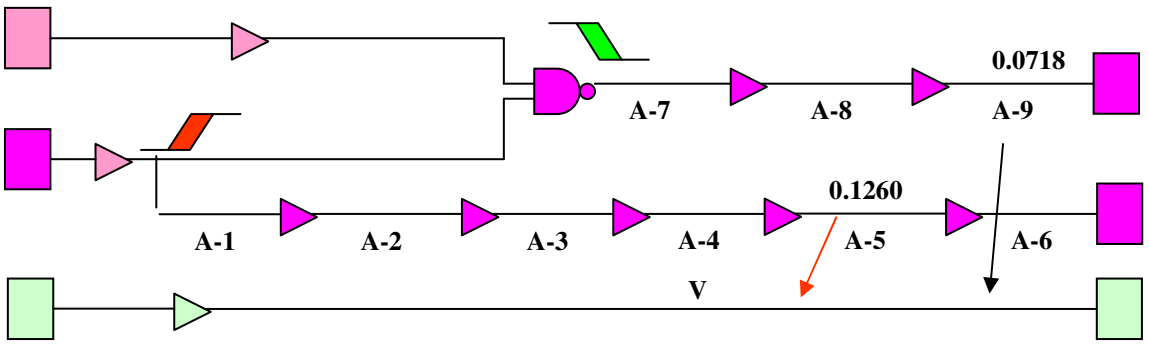


No Logic Correlation



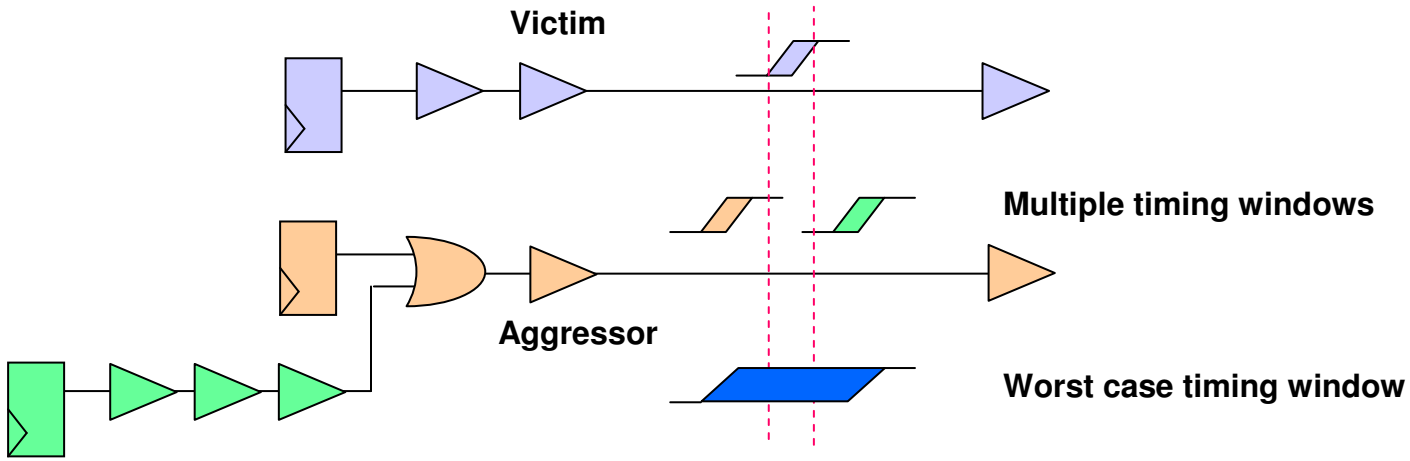
With *Logic Correlation*

- Complex gate structure
  - Aggressor vs. aggressors; aggressor vs. victim
  - Consider the different transitions between A-5 and A-9



SI Pessimism Reduction: Discrete Timing Window

- Consider multiple discrete timing windows instead of one worst case timing window
  - Remove unreal timing window overlaps and thus reduce pessimism



set xtalk_discrete_timing_window_check true

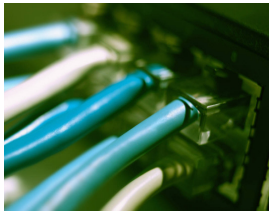
SI Pessimism Reductions: Customer Cases

- Noticeable amount of pessimism reductions
- Minimal runtime & memory overhead

	Advanced Xtalk pessimism reduction	Path slack improvement	report_timing runtime overhead	report_timing memory overhead
Design 1 (45nm, 7M instances)	Complex_gate	**28ps**	**1.16X**	**1.27X**
	Discrete_tw	**62ps**	**1.07X**	**1.01X**
	CRPR_tw	**80ps**	**1.08X**	**1.01X**
	all	**80ps**	**1.17X**	**1.27X**
Design 2 (45nm, 12M instances)	Complex_gate	**36ps**	**1.11X**	**1.25X**
	Discrete_tw	**170ps**	**1.05X**	**1.01X**
	CRPR_tw	**162ps**	**1.06X**	**1.01X**
	all	**170ps**	**1.13X**	**1.25X**

Incentia Customer Status

- **Over 50 customer sites worldwide**
  - Renesas, STARC, Ricoh, S***
  - World top design service companies
    - GUC (TSMC), Faraday (UMC), Wipro (India)
  - Many other fabless IC companies
    - Mediatek, Realtek, Via-Telecom, Ambarella, Sibeam, ITE, Via, Richtek, etc



- **Over 1200 copies installed at customer sites**
- **Numerous customer tape-outs**
  - Largest tape-out size: more than 100M gates
  - Many advanced tape-outs in 40nm
  - All kinds of design applications

TimeCraft Summary

- Superior STA & SI performance
  - Fastest-speed: 2X to 3X faster than others
  - Multi-thread: further 2X to 5X speedup over single-thread
  - Big capacity: 100M gate tape-outs
- Advanced features for 40nm & below
  - Variation tolerant clock: accurate & efficient analysis
  - Multi-voltage-frequency STA through IPD analysis
- Feature-rich Advanced OCV solution
  - Adopted in customer tape-outs since 2005
- Advanced SI pessimism reduction features

- Proven through numerous customer tape-outs
  - Very easy to adopt & migrate
  - Many in 90/65/45/40nm processes