Company Introduction

◆ Mission: SoC nanometer timing and synthesis technology leader
◆ Channels

Direct Offices:
USA: Silicon Valley
Southern California
Taiwan: Hsinchu

Distributors:
Japan (Marubeni), India (ICON),
China (OnePass Solutions),
Korea (ED&C), Israel (AST)
Incentia Product Offering
“Fastest Timing Analysis & Design Closure”

◆ Timing analysis solutions
  ■ TimeCraft: High-speed, big capacity, signoff proven STA
  ■ TimeCraft-LOCV: Location Based OCV
  ■ TimeCraft-SI: Signal Integrity
  ■ TimeCraft-SSTA: Statistical STA
  ■ TimeCraft-PCA: Power Analysis
  ■ ConstraintCraft: Constraint Management

◆ Design closure solutions
  ■ ECOCraft-Power: Leakage Power ECO
  ■ ECOCraft-Timing: Hold-time and Setup-time ECO
Contents

- Timing Analysis Solutions
  - TimeCraft
    - TimeCraft-LOCV
    - TimeCraft-SI
TimeCraft Highlights

◆ Superior STA & SI performance
  ■ 2X – 3X faster than other tools
  ■ Less memory usage for big designs
◆ Proven signoff quality with hundreds of tape-outs
◆ Rich features
  ■ NLDM, CCS, ECSM
  ■ SDF & SPEF flows
  ■ IR-drop aware STA & SI
  ■ Voltage/temperature scaling
  ■ CPF/UPF support
  ■ LOCV
  ■ GRID/LSF based multi-task parallel MMMC
  ■ Multi-thread speedup
  ■ Variation tolerant clock: non-tree structure
  ■ Multi-voltage-frequency signoff
  ■ Advanced SI crosstalk pessimism reduction
## TimeCraft Customer Examples

- **Recent advanced customer tape-out cases**
  - 2X to 3X faster than competitors’ solutions

<table>
<thead>
<tr>
<th>Designs</th>
<th>Complexity</th>
<th>Competitor</th>
<th>TimeCraft</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Design 1</strong></td>
<td>50+M logic gates (SDF, 65nm)</td>
<td>Runtime: 11.8 hrs (single-thread)</td>
<td>Runtime: 3.9 hrs 24% less memory (single-thread)</td>
</tr>
<tr>
<td></td>
<td>150+ clock domains</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3000+ timing exceptions</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Very complex reporting</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Design 2</strong></td>
<td>30+M logic gates (SPEF+delta_SDF, 45nm)</td>
<td>Runtime: 8.5 hrs (multi-thread)</td>
<td>Runtime: 3.1 hrs 11% less memory (multi-thread)</td>
</tr>
<tr>
<td></td>
<td>170+ clock domains</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Multi-Vdd domains</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>LOCV with dual clock/data derating</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Design 3</strong></td>
<td>30M gates (SPEF-SI, 40nm)</td>
<td>Runtime: 9.2 hrs (multi-thread)</td>
<td>Runtime: 3.7 hrs 16% less memory (multi-thread)</td>
</tr>
<tr>
<td></td>
<td>240+ clock domains</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Clock mesh, CCS library</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>100+ M coupling-cap</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Some on-going advanced big customer tape-outs**
  - Around 100M gates
TimeCraft: Multi-thread Technologies

◆ Intra-command parallelism
  ■ Automatically performed
  ■ compile_spf, update_timing, check_timing, report_timing,
    get_timing_path, report_constraint, report_timing_coverage etc.

◆ Aggressive mode in big report generation

◆ Inter-command parallelism
  ■ Manually specify commands that can be performed in parallel
  ■ Command: parallel

◆ RESULT: Most aggressive multi-thread speedup
  ■ 2X to 5X over TC single-thread
**Multi-thread Aggressive Mode**

- Aggressive mode for report printing
  
  \[
  \text{report\_timing} \text{ –mt\_aggressive\_mode} \\
  \text{report\_constraint \text{ –mt\_aggressive\_mode}}
  \]

  - Significant runtime improvement for large sized report file
  - Within 10% of memory increase

An example of a large report file containing 5M paths after report_timing

![Graph showing the effect of the multi-thread aggressive mode on runtime and the number of reported paths.](image-url)

- **Report Timing elapsed time (sec)**
  - # of reported paths
  - # of threads on an 8-core machine
  - 1.74X, 3.37X, 5.25X, 5.09X
Inter-command Parallelism

◆ Command: `parallel`

◆ Parallel inputs
- Multiple SDF imports
- Multiple SPEF compilations

```
parallel {
  read_timing –analysis_type on_chip_variation top.sdf
  compile_spf –ocv_location only_pin –format spef top.spef
}
```

◆ Parallel outputs

```
parallel {
  report_timing –nworst 100 –max_paths 1000
  report_timing –begin_end_pair ...
  report_constraints ...
}
```
Multi-thread Speedup

- 2X to 5X speedup over single thread
- Example
  - Over 2.5X speedup using 4 cores and 3X speedup using 8 cores
  - Within 5% memory increase

<table>
<thead>
<tr>
<th>Task</th>
<th>Single-core (Elapsed time)</th>
<th>4-cores (Elapsed time)</th>
<th>8-cores (Elapsed time)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design &amp; lib import</td>
<td>206s</td>
<td>209s</td>
<td>207s</td>
</tr>
<tr>
<td>SDC loading</td>
<td>40s</td>
<td>39s</td>
<td>40s</td>
</tr>
<tr>
<td>SDF + SPEF pin locations (1)</td>
<td>394s</td>
<td>216s</td>
<td>212s</td>
</tr>
<tr>
<td>14 misc. report commands (2)</td>
<td>1271s</td>
<td>394s</td>
<td>284s</td>
</tr>
<tr>
<td>LOCV setting</td>
<td>1s</td>
<td>1s</td>
<td>1s</td>
</tr>
<tr>
<td>6 report_timing commands (3)</td>
<td>836s</td>
<td>210s</td>
<td>163s</td>
</tr>
<tr>
<td>Total</td>
<td>2748s</td>
<td>1069s</td>
<td>906s</td>
</tr>
<tr>
<td>Speedup</td>
<td>1x</td>
<td>2.57X</td>
<td>3.03X</td>
</tr>
</tbody>
</table>
Multi-task with Multi-thread

- Multi-task: Submit MMMC jobs to network machines
- Multi-thread: Each multi-core machine runs TimeCraft-MT

- SDF1 (Corner1)
- SDFN (CornerN)
- Netlist
- Script1 (Mode1)
- ScriptM (ModeM)

- Host1
  - 1 quad-core CPU
  - Task 1
    - Mode1 Corner1
    - Thread 1
    - Thread 2
    - Thread 4

- HostM
  - 2 dual-core CPUs
  - Task M
    - ModeM Corner1
    - Thread 1
    - Thread 2
    - Thread 4

- HostM+1
  - 4 single-core CPUs
  - Task M+1
    - ModeM Corner2
    - Thread 1
    - Thread 2
    - Thread 4

- HostMXN
  - 2 dual-core CPUs
  - Task MxN
    - ModeM CornerN
    - Thread 1
    - Thread 2
    - Thread 4

Merged Timing Reports
Incentia Delay Calculator Accuracy

- Path delay accuracy (45nm customer cases)
  - Plot TimeCraft path delays vs. SPICE results: within 2%
Variation Tolerant Clock
Non-tree Clock Structures

◆ Non-tree clock structures, e.g. clock mesh
  ■ Reduce skew at leaf instances
  ■ Thus reduce number of corner runs

◆ Big customer clock mesh example
  ■ 1024 x 4096
  ■ Only solution satisfying desired accuracy & runtime
◆ Interface to output SDF/SDC
  ■ write_mesh_clock_interface

(Courtesy of Japan STARC)
Comparison to SPICE results
(1) Mesh in->out path delays: within 6%
(2) Clock skews are within 7 ps
Multi-voltage-frequency STA
Inter Power Domain (IPD) Derating

- IPD timing analysis
  - Low power designs contain multiple voltage domains
  - Accurate STA needs to consider all voltage combinations

- Goal
  - Reduce multiple voltage-combination corner runs to 1

- Solution
  - IPD timing analysis & derating
  - Support both Graph based & Path based
IPD Timing Analysis: Path Based Example

- Analyze path segments based on voltage domains
  - In each voltage domain, if the slack is worse after applying the IPD derating factor => Apply the IPD derating factor

- IPD derating table
  - Global IPD derating factor
  - Cell-based IPD derating factors
Contents

Timing Analysis Solutions
- TimeCraft
- TimeCraft-LOCV
- TimeCraft-SI
Advanced OCV (a.k.a. LOCV)

- Reduce over-pessimism timing analysis

- Consider variations using variable timing derating factors
  - Level (stage) based: random variations
  - Location (distance) based: systematic variations

- Rich features
  - Many fine-grain controls for further pessimism reduction
  - Native engine based: fastest runtime

- Many customer tape-outs in 90, 65, 55, 45, 40nm
Advanced OCV (a.k.a. LOCV) (Cont)

- Level (stage) based
  - Derating factor depends on path stages
- Location (distance) based
  - Derating factor depends on path locations: diagonal distance of bounding box

Level-based
Data path, level = 5
Clock path, level = 2

Common clock point

Location based Distance
Bounding box
TimeCraft-LOCV Flow

**Usage**
- Level based (1D)
- Level & Location based (2D)
  - Location information from SPEF or DEF

**TimeCraft-LOCV SDF Flow**
- Netlist
- SDC
- Lib
- SDF
- ΔSDF
- Cell Locations (SPEF or DEF)
- Derating Table (1D or 2D)

**TimeCraft-LOCV SPEF Flow**
- Netlist
- ΔSDF
- SDC
- Lib
- SPEF (RC & Cell Locations)
- Derating Table (1D or 2D)

Timing Reports
## TimeCraft-LOCV: Derating Table

- Level based: 1D table
- Level & Location based: 2D table
- Example: two-dimension table
  - X axis: Level (logic stage)
  - Y axis: Location (diagonal of bounding box)

### MAX-Hold-Early

<table>
<thead>
<tr>
<th>Distance</th>
<th>0</th>
<th>2000</th>
<th>8000</th>
<th>16000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stage</td>
<td>0</td>
<td>1 2 4</td>
<td>8 16 32</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.85</td>
<td>0.85</td>
<td>0.88</td>
<td>0.91</td>
</tr>
<tr>
<td></td>
<td>0.85</td>
<td>0.86</td>
<td>0.88</td>
<td>0.90</td>
</tr>
<tr>
<td></td>
<td>0.83</td>
<td>0.85</td>
<td>0.87</td>
<td>0.90</td>
</tr>
<tr>
<td></td>
<td>0.82</td>
<td>0.84</td>
<td>0.85</td>
<td>0.89</td>
</tr>
</tbody>
</table>

### MAX-Setup-Early

<table>
<thead>
<tr>
<th>Distance</th>
<th>0</th>
<th>2000</th>
<th>8000</th>
<th>16000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stage</td>
<td>0</td>
<td>1 2 4</td>
<td>8 16 32</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.85</td>
<td>0.85</td>
<td>0.88</td>
<td>0.91</td>
</tr>
<tr>
<td></td>
<td>0.84</td>
<td>0.84</td>
<td>0.87</td>
<td>0.90</td>
</tr>
<tr>
<td></td>
<td>0.82</td>
<td>0.84</td>
<td>0.86</td>
<td>0.89</td>
</tr>
<tr>
<td></td>
<td>0.81</td>
<td>0.83</td>
<td>0.85</td>
<td>0.88</td>
</tr>
</tbody>
</table>

- Max delays in SDF are too pessimistic; Compensate by factors less than 1
- Longer distance means more systematic variations; Factors are farther away from 1
- More logic levels means less random variations; Factors are closer to 1
Level-based OCV: Cell Level Control

◆ Fine-grain control on cell level counts
  ■ Default: 1 cell counted as 1 level
  ■ Cell based: larger count for more complicated cell
  ■ Timing arc based: larger count for longer cell timing path
  ■ Mode based: read/write mode in memory cell
  ■ Cell delay based: function of cell delay
◆ Mixture of variable and fixed deratings
## TimeCraft-LOCV Benefits

- **Tape-outs prove advantages of TimeCraft-LOCV**
  - Smaller WNS and fewer timing violations
  - Less conservative; easy to achieve timing closure

- **Native-engine based**
  - Very fast runtime speed!

### Case Study (45nm) Comparison

<table>
<thead>
<tr>
<th>Case Study (45nm)</th>
<th>Traditional OCV</th>
<th>Level-based OCV</th>
<th>Level &amp; Location-based OCV</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Setup</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td># Violations</td>
<td>582</td>
<td>318</td>
<td>83</td>
</tr>
<tr>
<td>WNS</td>
<td>-0.675ns</td>
<td>-0.239ns</td>
<td>-0.01ns</td>
</tr>
<tr>
<td>Runtime</td>
<td>1X</td>
<td>1.1X</td>
<td>1.3X</td>
</tr>
<tr>
<td>Memory</td>
<td>1X</td>
<td>1.1X</td>
<td>1.2X</td>
</tr>
<tr>
<td><strong>Hold</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td># Violations</td>
<td>3795</td>
<td>193</td>
<td>37</td>
</tr>
<tr>
<td>WNS</td>
<td>-0.059ns</td>
<td>-0.023ns</td>
<td>-0.01ns</td>
</tr>
<tr>
<td>Runtime</td>
<td>1X</td>
<td>1.2X</td>
<td>1.3X</td>
</tr>
<tr>
<td>Memory</td>
<td>1X</td>
<td>1.1X</td>
<td>1.2X</td>
</tr>
</tbody>
</table>
Contents

Timing Analysis Solutions

- TimeCraft
- TimeCraft-LOCV
- TimeCraft-SI
TimeCraft-SI Flow

SDC → Netlist → SPEF → TimeCraft-SI
Integrated static timing & SI analysis

Libraries (.lib, CCS, ECSM)

SDF
△SDF

Timing reports
Delta delays
Noise

Timing window file
TimeCraft-SI Highlights

◆ Rich features
  - Support NLDM, CCS, and ECSM libraries
  - Cross talk delta delay analysis
  - Noise analysis
◆ Accurate analysis results: Within 5% of SPICE
◆ Very fast runtime, big capacity
  - 2X to 3X faster than other solutions
  - Multi-thread capability
◆ Advanced crosstalk pessimism reduction
  - Logical correlation in simple/complex gates
  - CRPR in cross talk
  - Discrete timing window
Cross-talk Analysis: Accuracy (Cont)

◆ CCS 45nm library
  - Mean value within 5% of SPICE
  - Standard deviation within 7%

<table>
<thead>
<tr>
<th></th>
<th>Typical</th>
<th>Slow</th>
<th>Fast</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test case set 1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mean</td>
<td>1.0%</td>
<td>3.6%</td>
<td>-2.0%</td>
</tr>
<tr>
<td>Std dev</td>
<td>2.5%</td>
<td>5.8%</td>
<td>6.4%</td>
</tr>
<tr>
<td>Test case set 2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mean</td>
<td>1.8%</td>
<td>3.3%</td>
<td>2.6%</td>
</tr>
<tr>
<td>Std dev</td>
<td>2.7%</td>
<td>5.2%</td>
<td>6.7%</td>
</tr>
</tbody>
</table>

Courtesy of STARC for the data based upon TC 2009.12 version
SI Pessimism Reduction: Logical Correlation

- Too pessimistic assuming all aggressors switching at one direction
- Simple gate structure

- Complex gate structure
  - Aggressor vs. aggressors; aggressor vs. victim
  - Consider the different transitions between A-5 and A-9
SI Pessimism Reduction: Discrete Timing Window

- Consider multiple discrete timing windows instead of one worst case timing window
  - Remove unreal timing window overlaps and thus reduce pessimism

```
set xtalk_discrete_timing_window_check true
```
SI Pessimism Reductions: Customer Cases

- Noticeable amount of pessimism reductions
- Minimal runtime & memory overhead

<table>
<thead>
<tr>
<th>Advanced Xtalk pessimism reduction</th>
<th>Path slack improvement</th>
<th>report_timing runtime overhead</th>
<th>report_timing memory overhead</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design 1 (45nm, 7M instances)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Complex_gate</td>
<td>28ps</td>
<td>1.16X</td>
<td>1.27X</td>
</tr>
<tr>
<td>Discrete_tw</td>
<td>62ps</td>
<td>1.07X</td>
<td>1.01X</td>
</tr>
<tr>
<td>CRPR_tw</td>
<td>80ps</td>
<td>1.08X</td>
<td>1.01X</td>
</tr>
<tr>
<td>all</td>
<td>80ps</td>
<td>1.17X</td>
<td>1.27X</td>
</tr>
<tr>
<td>Design 2 (45nm, 12M instances)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Complex_gate</td>
<td>36ps</td>
<td>1.11X</td>
<td>1.25X</td>
</tr>
<tr>
<td>Discrete_tw</td>
<td>170ps</td>
<td>1.05X</td>
<td>1.01X</td>
</tr>
<tr>
<td>CRPR_tw</td>
<td>162ps</td>
<td>1.06X</td>
<td>1.01X</td>
</tr>
<tr>
<td>all</td>
<td>170ps</td>
<td>1.13X</td>
<td>1.25X</td>
</tr>
</tbody>
</table>
Incentia Customer Status

♦ Over 50 customer sites worldwide
  ■ Renesas, STARC, Ricoh, S***
  ■ World top design service companies
    ● GUC (TSMC), Faraday (UMC), Wipro (India)
  ■ Many other fabless IC companies
    ● Mediatek, Realtek, Via-Telecom, Ambarella, Sibeam, ITE, Via, Richtek, etc

♦ Over 1200 copies installed at customer sites
♦ Numerous customer tape-outs
  ■ Largest tape-out size: more than 100M gates
  ■ Many advanced tape-outs in 40nm
  ■ All kinds of design applications
TimeCraft Summary

- Superior STA & SI performance
  - Fastest-speed: 2X to 3X faster than others
  - Multi-thread: further 2X to 5X speedup over single-thread
  - Big capacity: 100M gate tape-outs
- Advanced features for 40nm & below
  - Variation tolerant clock: accurate & efficient analysis
  - Multi-voltage-frequency STA through IPD analysis
- Feature-rich Advanced OCV solution
  - Adopted in customer tape-outs since 2005
- Advanced SI pessimism reduction features
- Proven through numerous customer tape-outs
  - Very easy to adopt & migrate
  - Many in 90/65/45/40nm processes