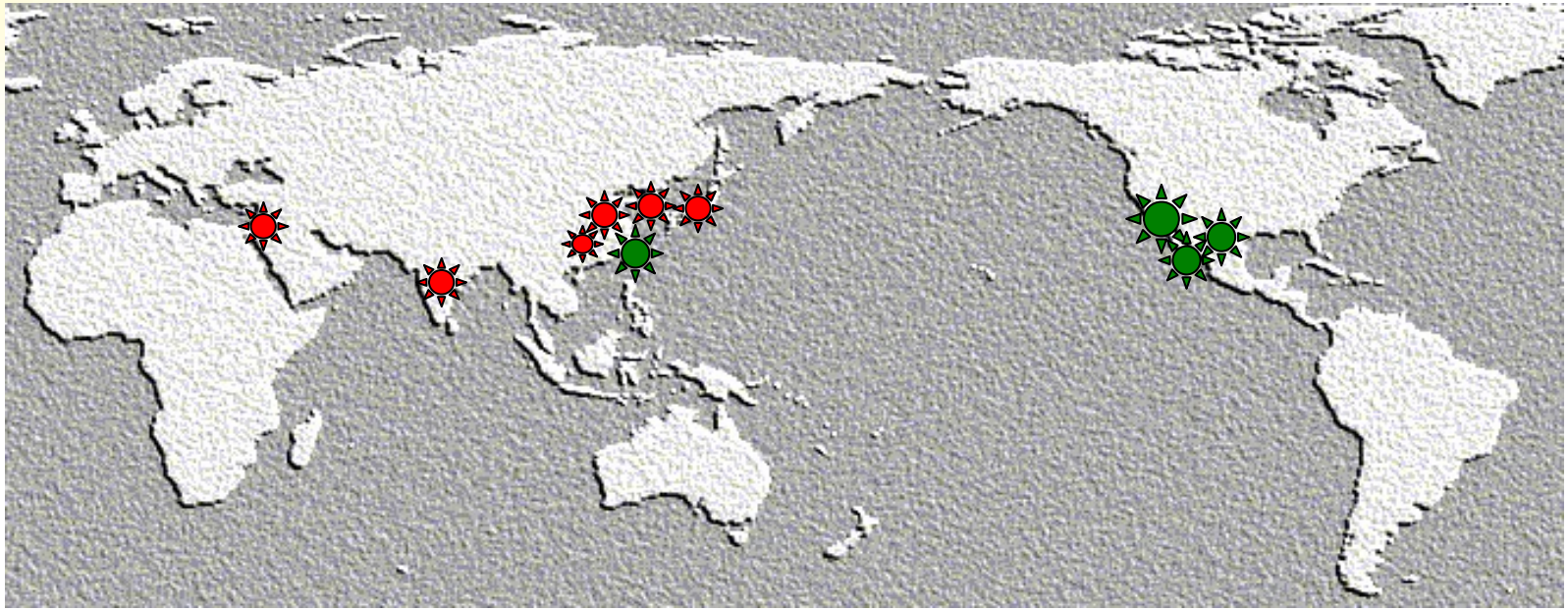
Incentia Test Synthesis Solution TestCraft

Incentia Design Systems, Inc.

October, 2010

Company Introduction

- Mission: SoC nanometer timing and synthesis technology leader
- Channels



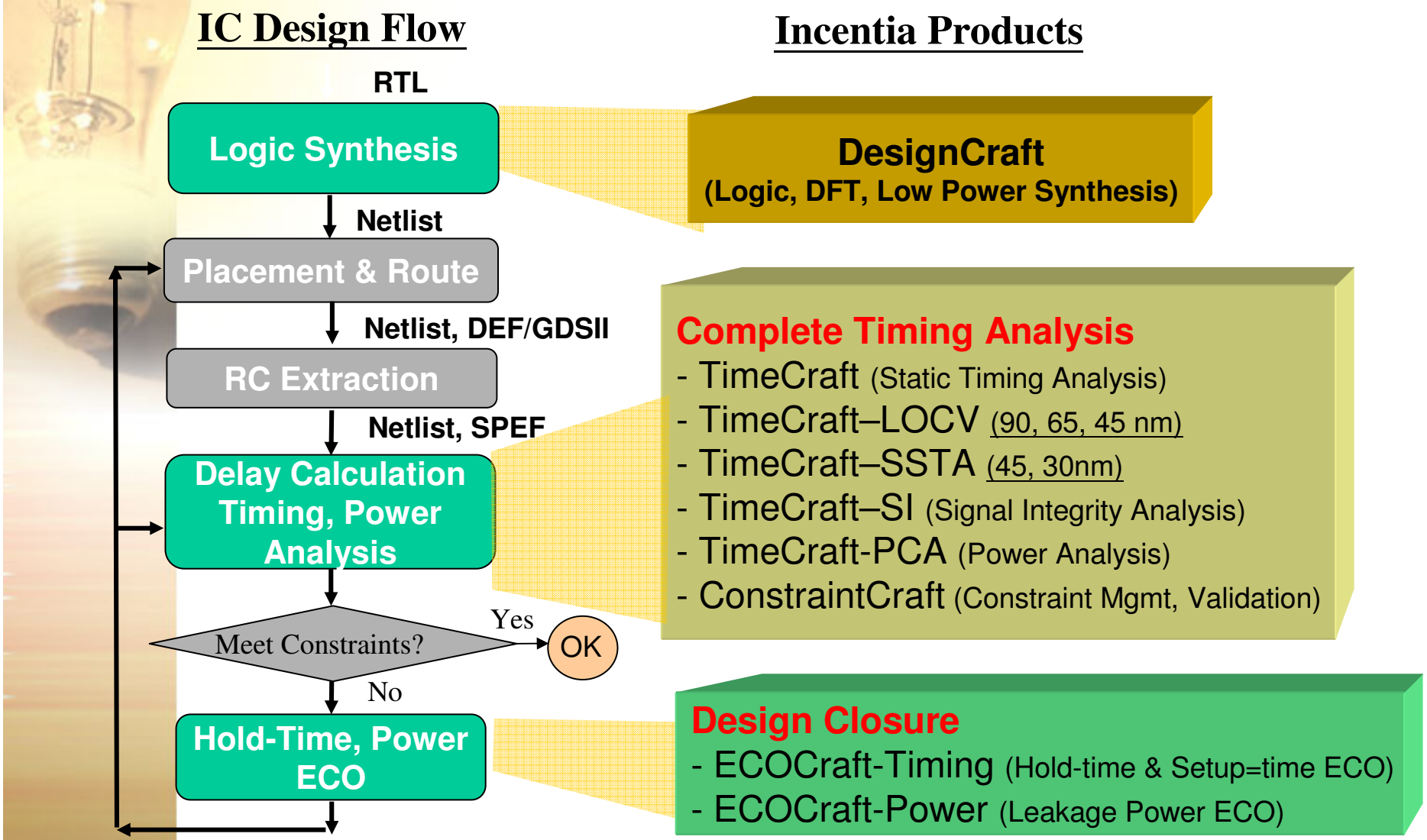
Direct Offices:
USA: Silicon Valley
Southern California
Taiwan: Hsinchu

Distributors:
Japan (Marubeni), India (ICON),
China (OnePass Solutions),
Korea (ED&C), Israel (AST)

Incentia Product Offering

- **Logic, Low Power, DFT Synthesis solution**
  - **DesignCraft, PowerCraft, TestCraft**
- **Timing analysis solution**
  - TimeCraft: World fastest Static Timing Analyzer (STA)
  - TimeCraft-LOCV: Location Based OCV
  - TimeCraft-SSTA: Statistical STA
  - TimeCraft-SI: Signal Integrity
  - TimeCrfaft-PCA: Power Analysis
  - ConstraintCraft: Constraint Management
- **Design closure solution**
  - ECOCraft-Timing: Hold-time & Setup-time ECO
  - ECOCraft-Power: Leakage power ECO

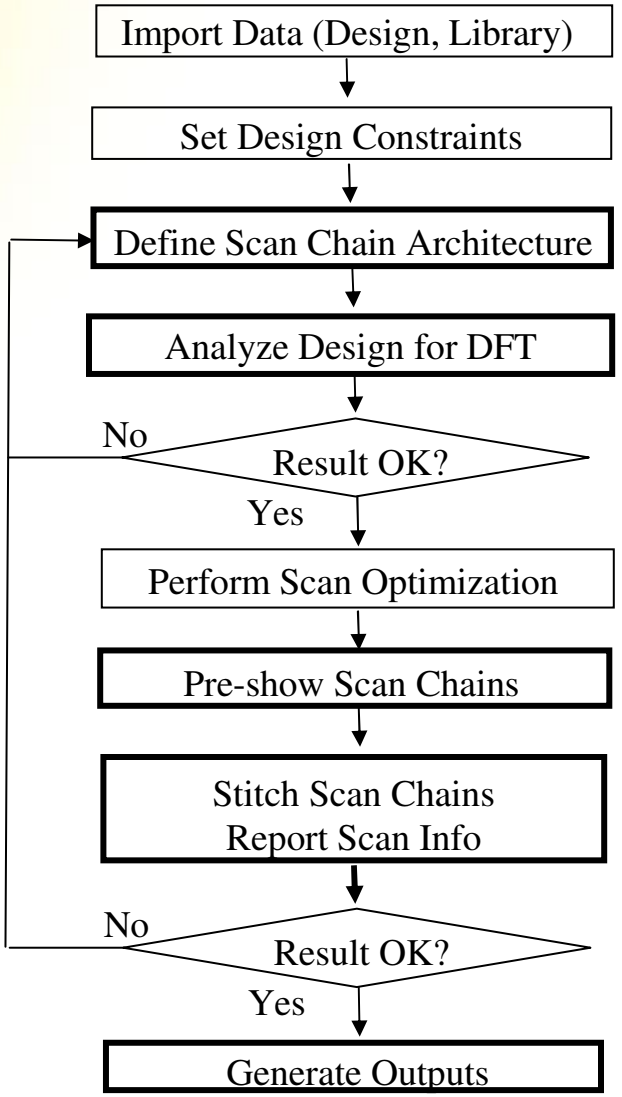
How Incentia Products Fit into Design Flow



TestCraft Key Features

- One pass logic and DFT synthesis
- Top-down or bottom-up design methodology
- Scan cell replacement
- DFT rule checking
- Automatic fixing of DFT rule violations
- Scan chain ordering, stitching, balancing
- Smooth integration to Incentia low power solution
- Smooth interface to 3rd-party ATPG tools: STIL format
  - Mentor (FastScan), Synopsys (TetraMax), SynTest (TurboScan)
- Shorter downstream ATPG runtime
  - More DFT violations can be fixed during DFT synthesis

Typical DFT Flow (RTL or Netlist Input)




```
compile_lib, read_design, link_design
make_unique, set target_lib
```

```
Load SDC constraints
```

```
set_scan_implementation
set_dft_rule_option
set_scan_port, set_scan_route
set_scan_cell_connect_style
```

```
check_design
check_dft_rule
```

```
optimize -scan (for RTL input)
```

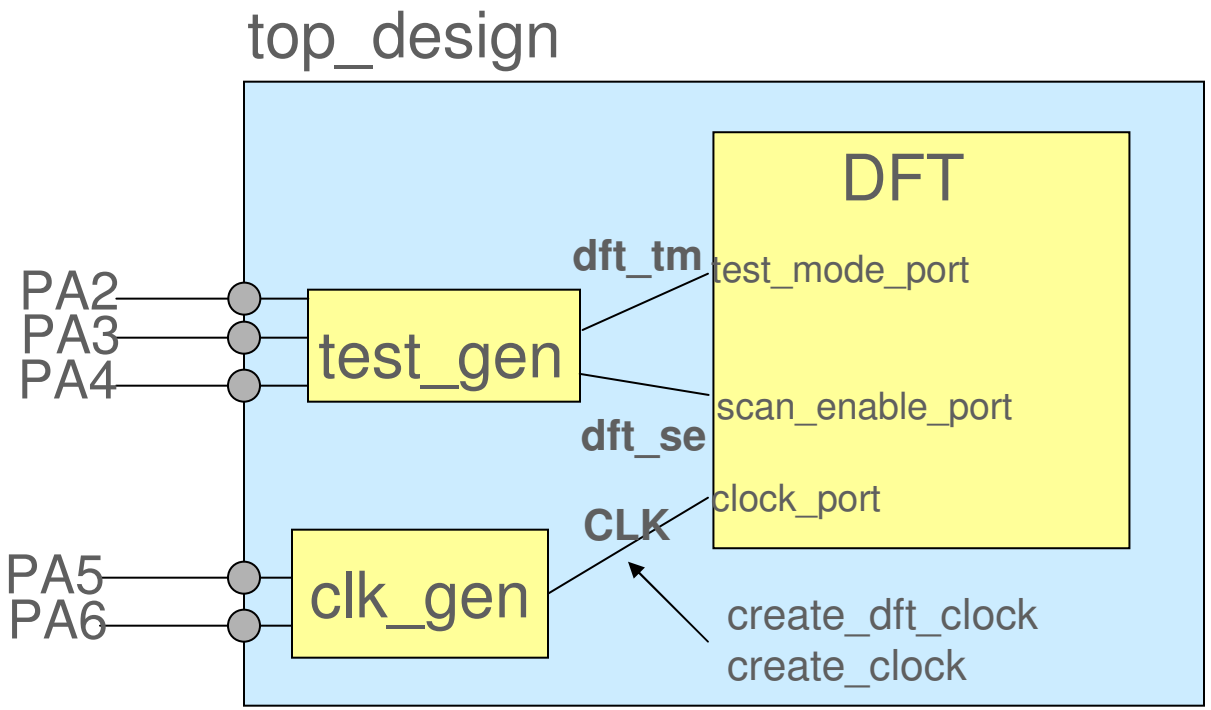
```
set_scan_implementation -stitch false
implement_scan
pre_show_dft
```

```
set_scan_implementation -stitch true
implement_scan
report_dft
```

```
write_design
write_dft_interface
```

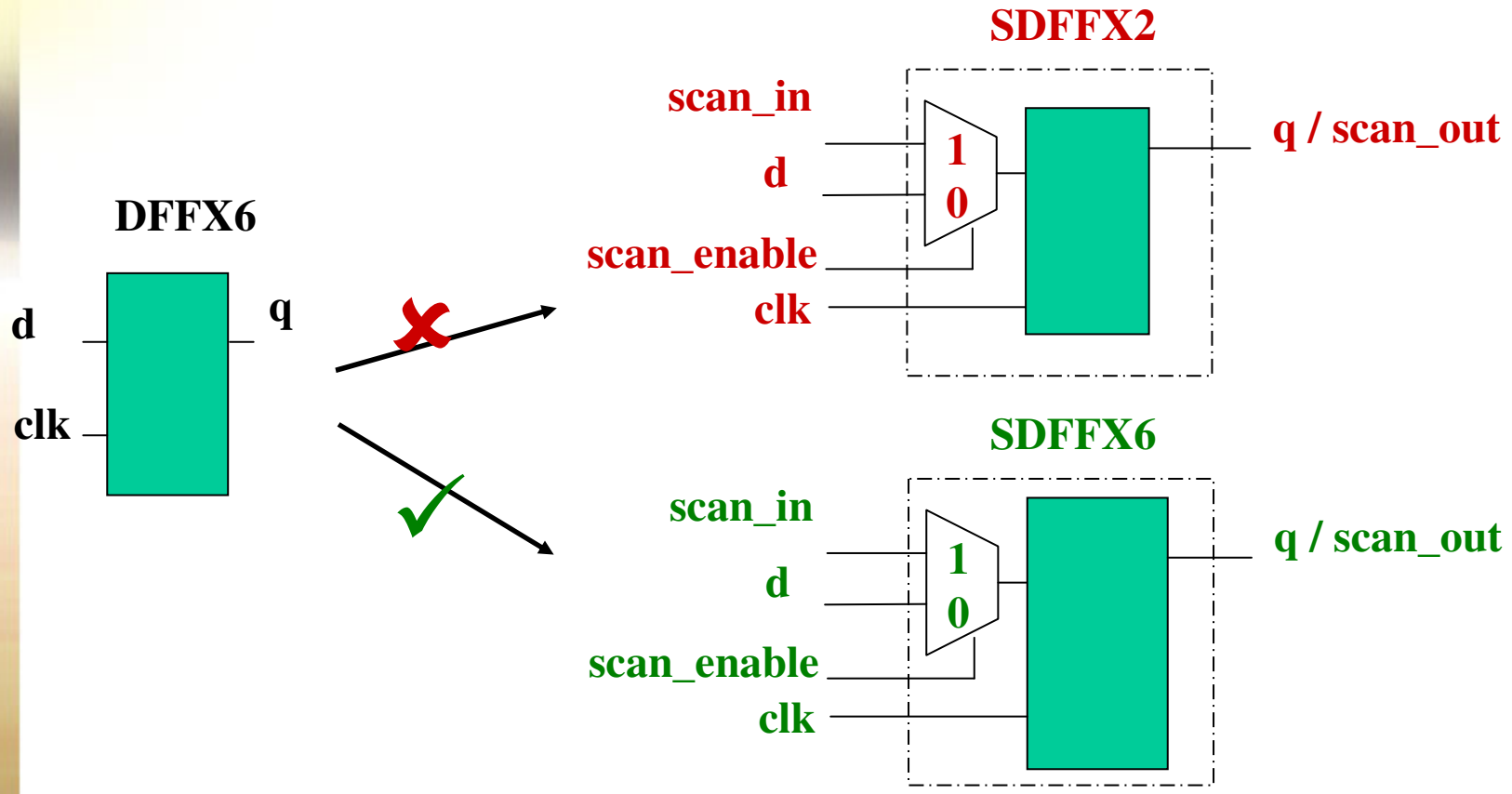
Fastest Runtime: STA-based Technology

- Fastest run time: up to 10X faster than any other solutions!
  - Key technology: STA based static analysis
    (vs. event driven approach used in other tools)
  - Bigger designs show bigger speedup



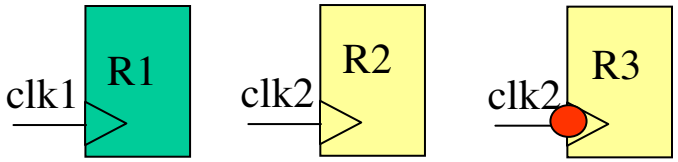
Efficient Scan Cell Replacement

- Scan cell replacement
  - Preserve timing quality of pre-DFT design



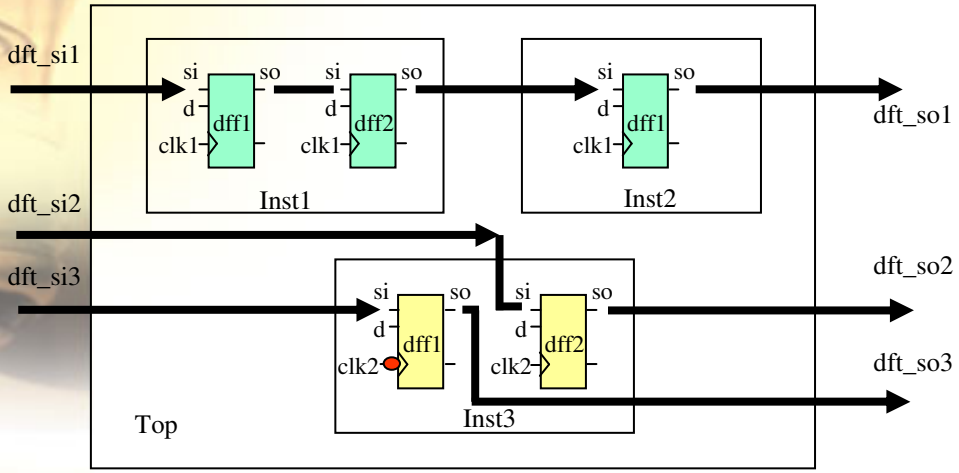
Scan Chain Planning

- Rich controls in scan chain ordering & stitching
  - Number of scan chains
  - Chain length
  - Balanced chaining
  - Chaining styles
    - Chain with distinctive clock domain: (R1), (R2), (R3)
    - Chain with merged clocks: (R1, R2, R3)
    - Chain with merged edges: (R1), (R2, R3)
    - Chain with merged clocks but not edges: (R1, R2), (R3)

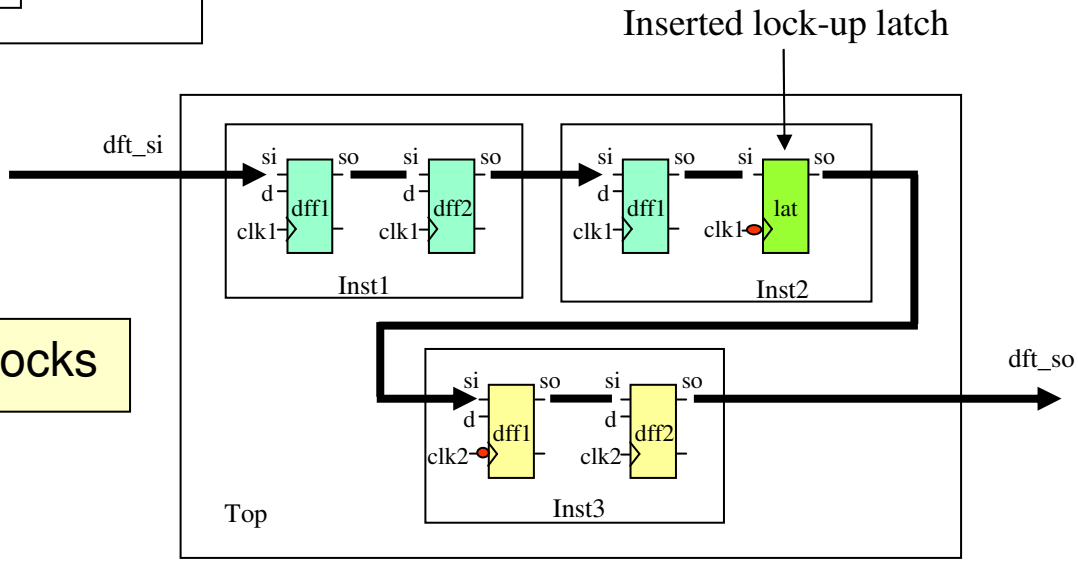


  - Lock-up latch insertion to avoid timing issues
    - Automatic & user-control

Scan Chaining: Example



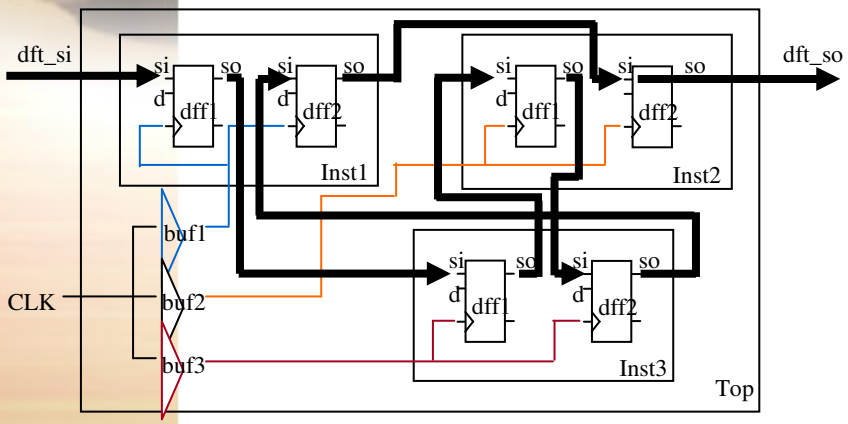
- Chain by distinctive clock domain



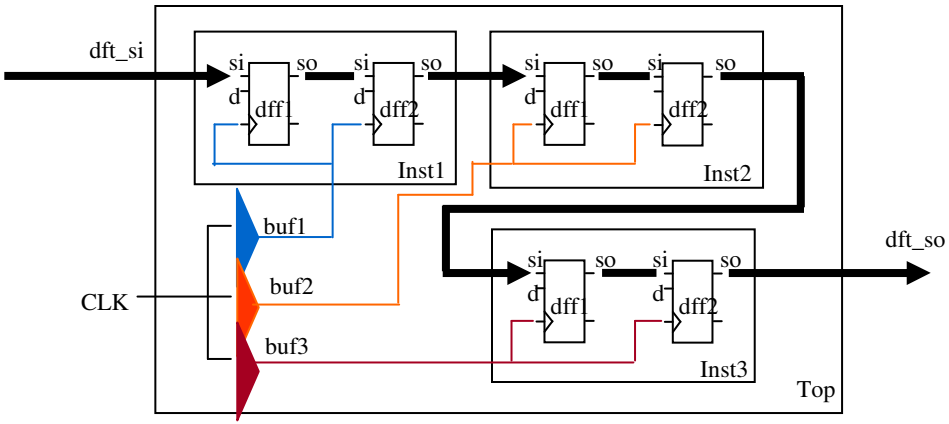
- Chain by merged clocks

Clock Tree Based Scan Chaining

- Clock tree based scan ordering and chaining
  - Clock tree grouping and ordering
  - Example: buf1 group first, following by buf2, and buf3 groups



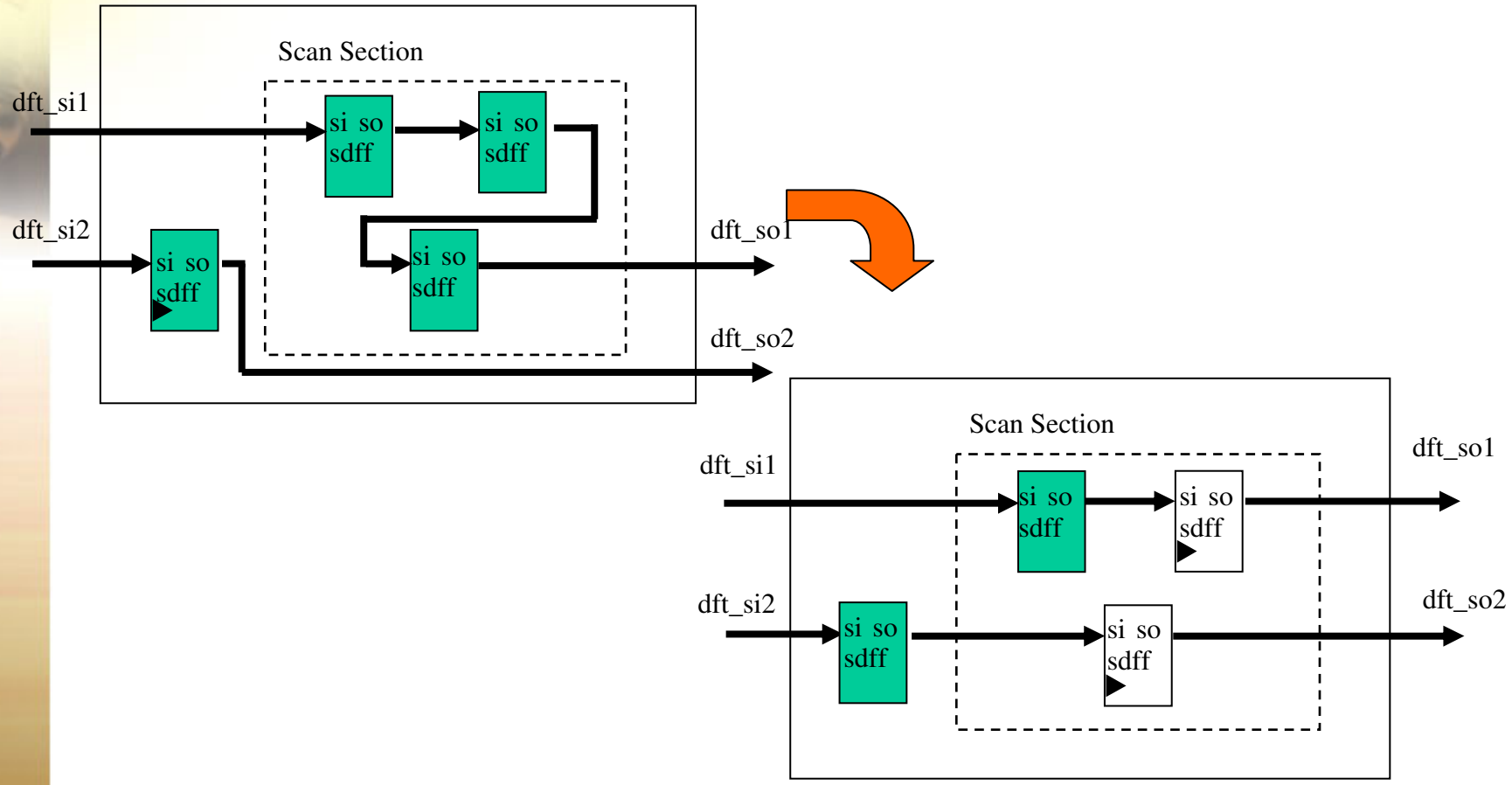
One possible result if clock tree information is not considered



Clock tree information is given { buf1/o, buf2/o, buf3/o} to guide scan chaining

Scan Chain Re-chaining

- Scan chain re-chained
  - Re-balance scan chains on existing scan chains

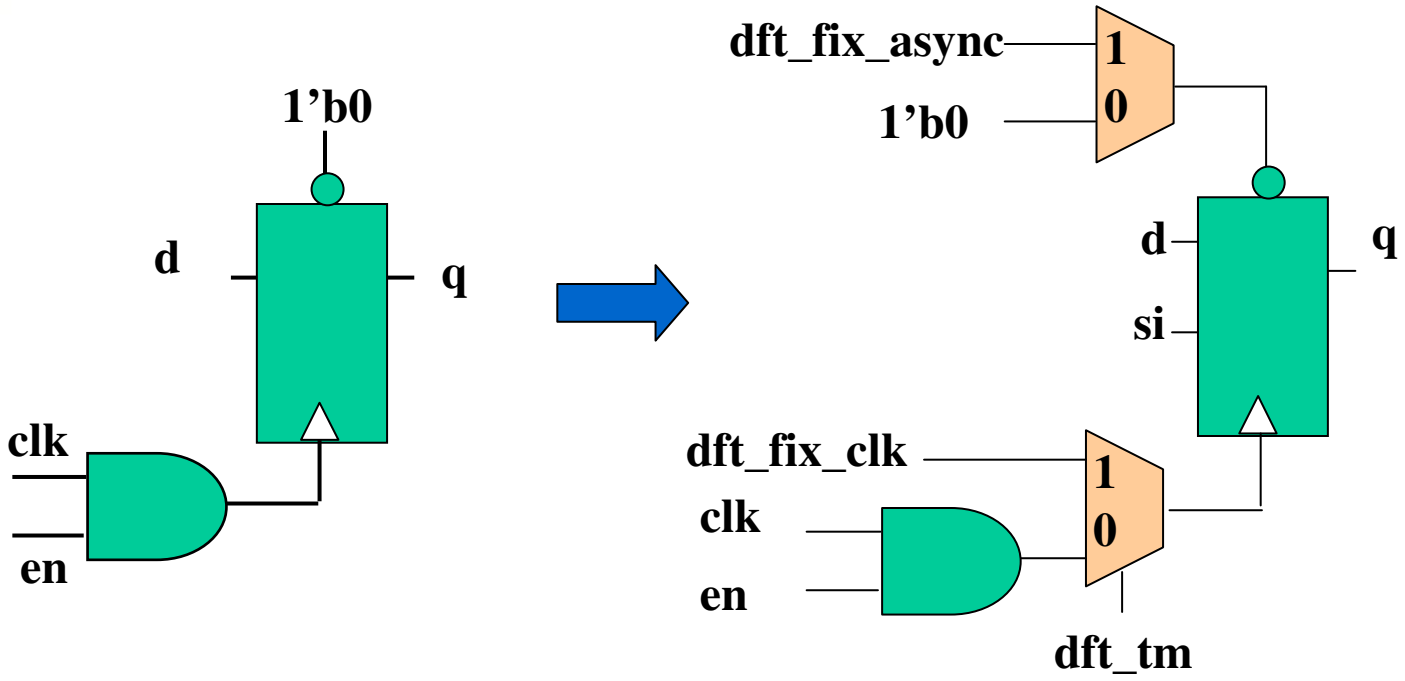


DFT Rule Checking & Fixing

- DFT rule violations will cause
  - Shorter or incorrect scan chains
  - Lower fault coverage or failure in later ATPG
- Checking of over 25 rule violations
  - Clock, latch, asynchronous signals, gated clock, tri-state bus, bi-direction port, etc.
- Automatic fixing of over 15 rule violations
  - MUX-style, disable-style
- Fastest runtime for checking & fixing
  - Unique patented STA-bases approach

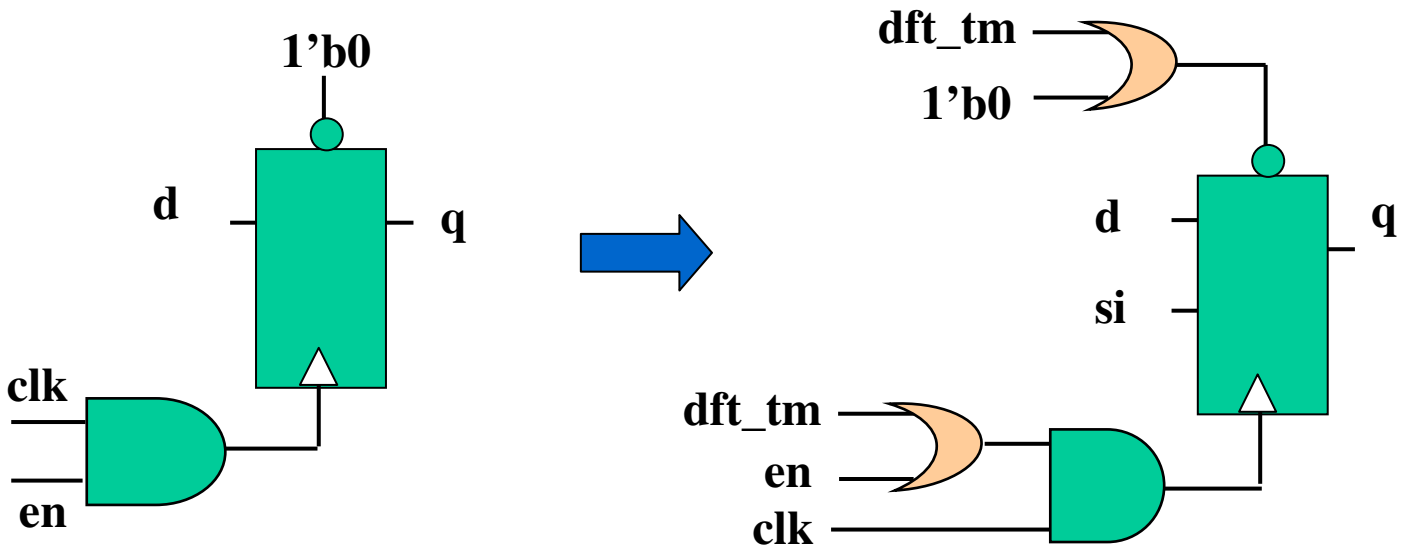
Automatic Fixing of DFT Rule Violations

- DFT Violation Fixing (MUX-Style)
  - Uncontrollable, Gated, Generated Clock Violation Fixing
  - Uncontrollable Asynchronous Set/Reset Violation Fixing



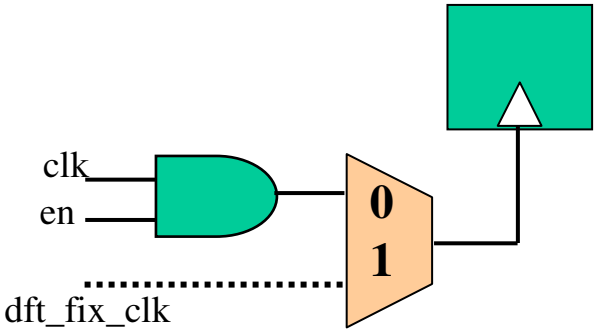
Automatic Fixing of DFT Rule Violations (Cont)

- DFT Violation Fixing (Disable-Style)
  - Uncontrollable, Gated, Generated Clock Violation Fixing
  - Uncontrollable Asynchronous Set/Reset Violation Fixing

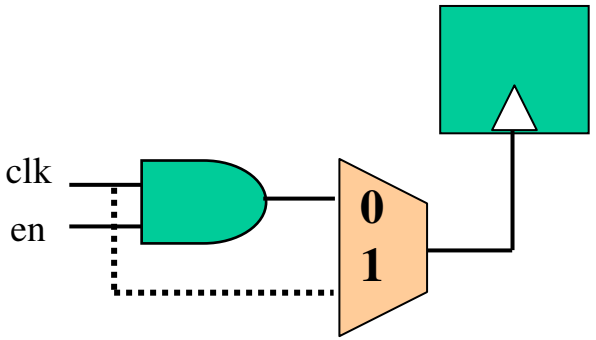


Automatic Fixing of DFT Rule Violations (Cont)

- Same Clock Source Fixing
  - This fixing can help to reduce buffer insertion by clock tree synthesis.



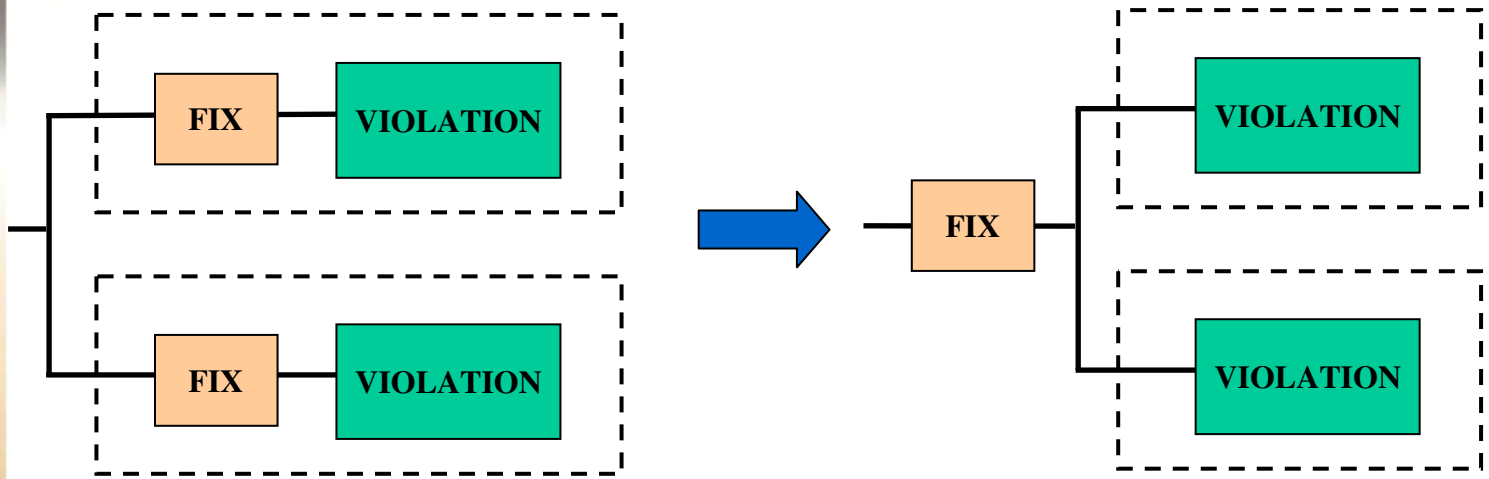
Default Fixing



CTS Specific Fixing

Automatic Fixing of DFT Rule Violations (Cont)

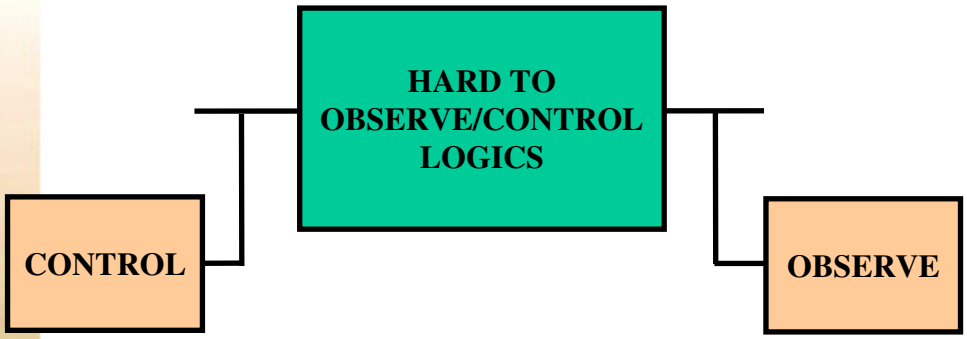
- Cross Hierarchy Fixing
  - Reduce the logic count, thus reduce area



Testability Estimation

- Testability estimator before ATPG
- Test Point Insertion & Testability Report
  - Insert test point to hard observe or control point
  - Report hard to observe or control point

CONTROLLABILITY		
Level of Logics	Net	Terminal Pin (Starting pt)
5	N340	reg2/SO
4	N23	reg1/SO
2	N3	Top_in1

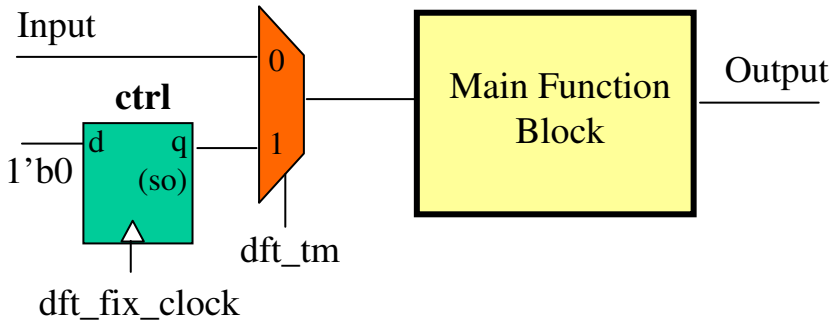


OBSERVABILITY		
Level of Logics	Net	Terminal Pin (Ending pt)
7	N55	reg7/D
4	N402	reg6/CK
1	N2	Top_out6

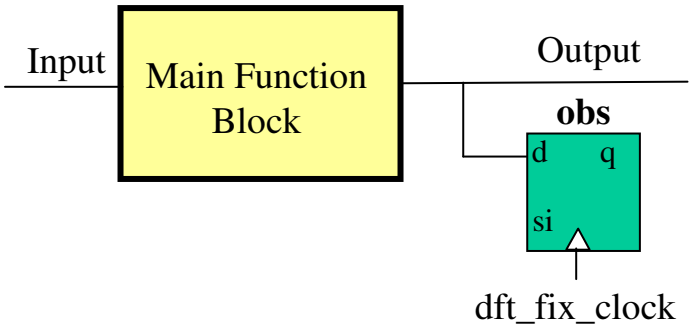
Test Point Insertion

- Insert test points at hard to control or observe locations

Inserting control test point
=> A Reg & a MUX are added

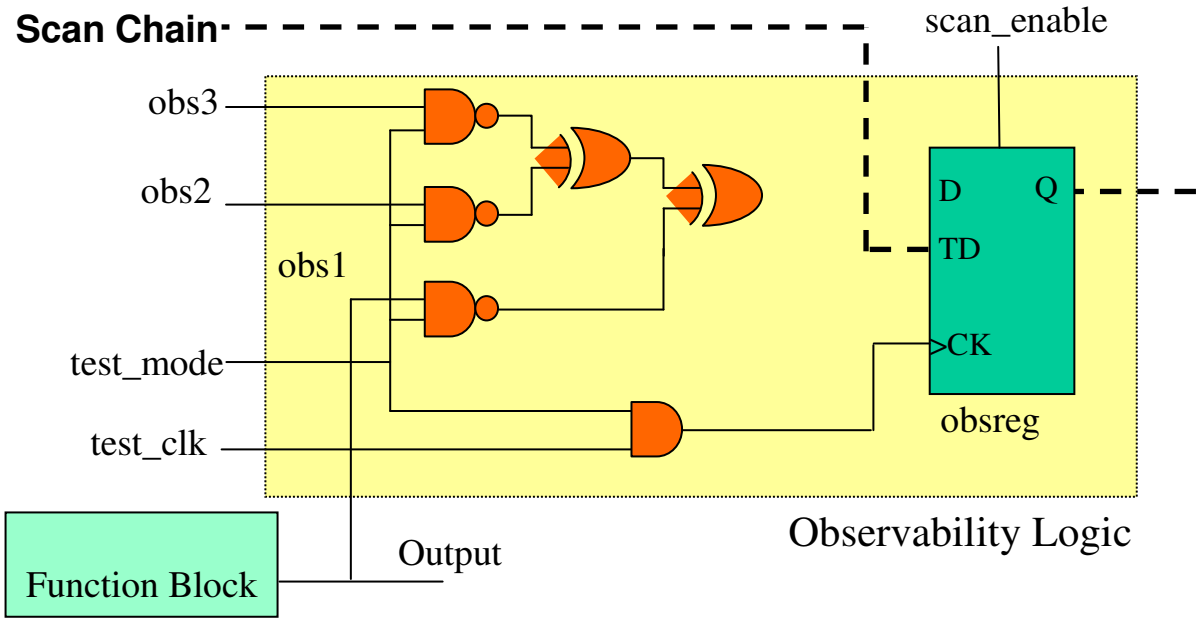


Inserting observe test point
=> A MUX is added



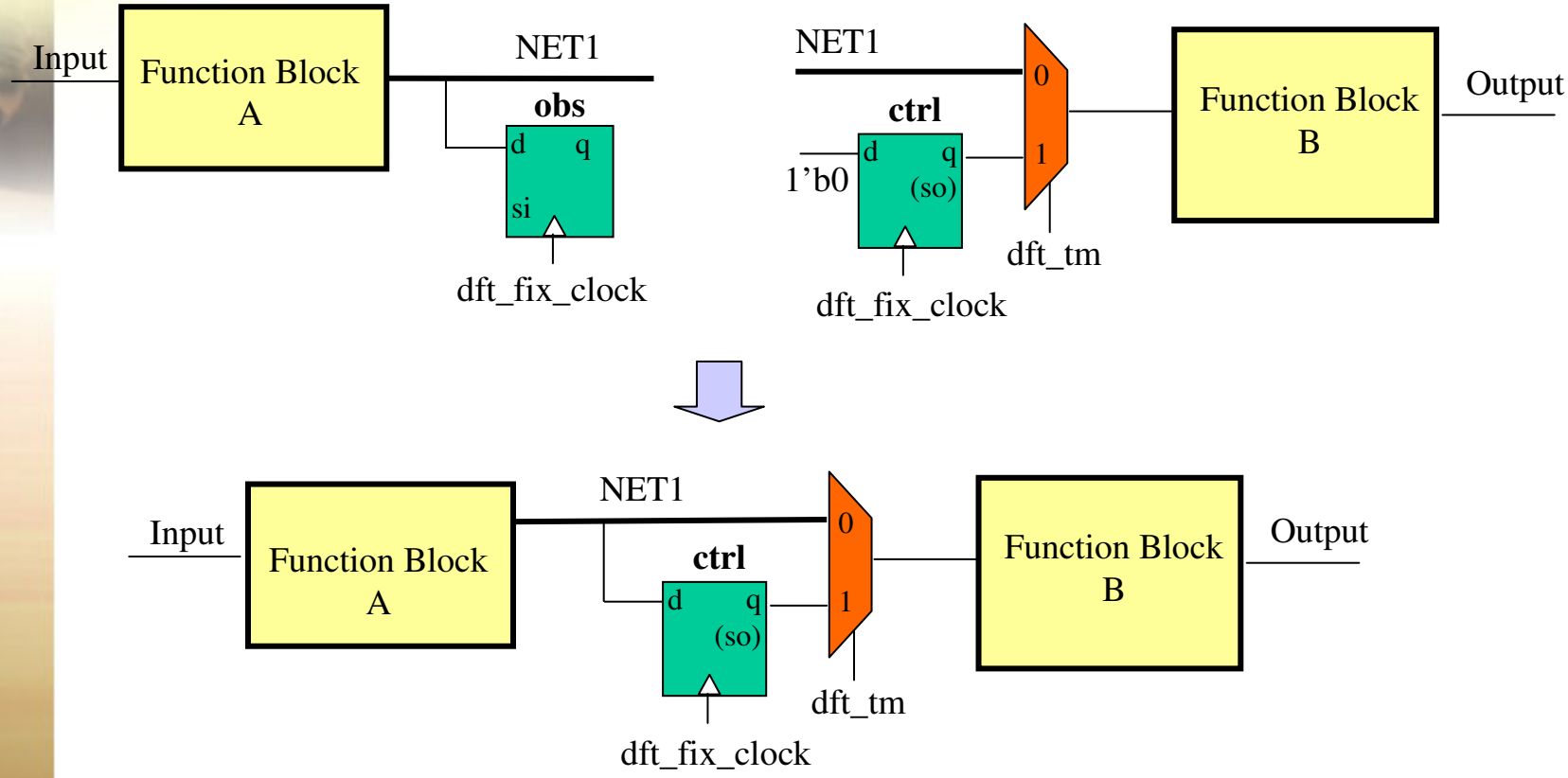
Observation Test Point Compression

- Compress multiple observation test points into one test point logic to reduce the logic
  - Can control # of compressed points
  - Example: compress obs1, obs2, obs3 into 1 test point logic



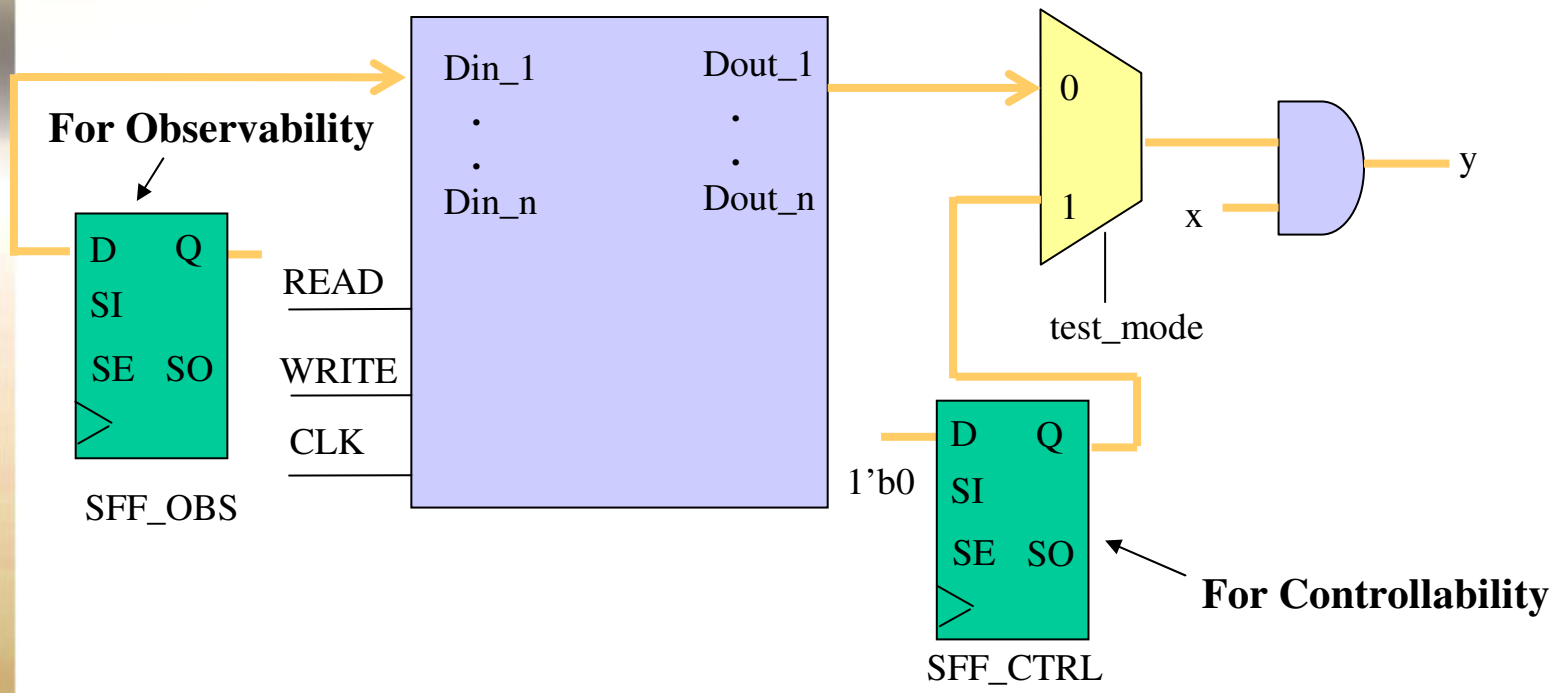
Sharing Control & Observe Test Point

- Control & observe logic at the same point can be shared
- Example: NET1 is hard to control & observe



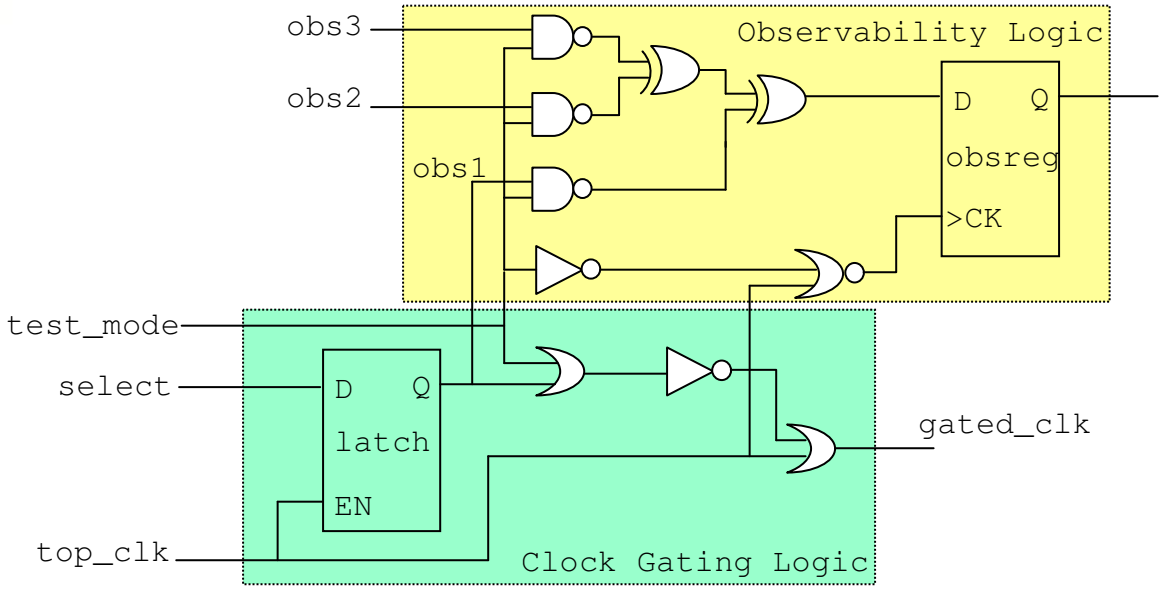
Bypass Logic

- Adding bypass logic for memory blocks or black boxes
  - Insert observable and/or controllable logics to increase testability



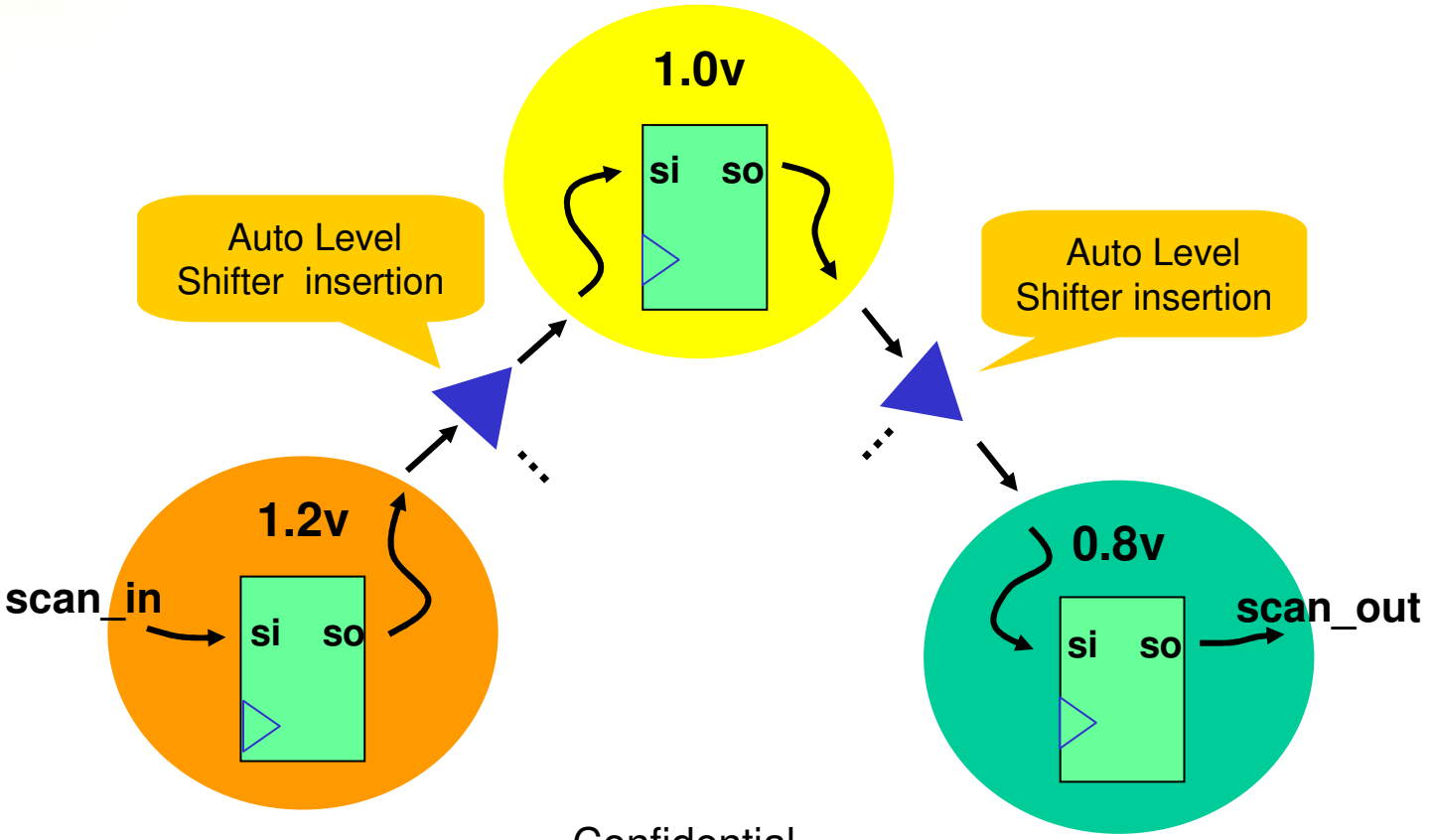
Seamless DFT and Low Power Integration

- Smooth DFT & low power integration
  - Automatic DFT insertion for clock gating in Incentia environment



Multiple Supply Voltages

- DFT for multiple supply voltages
  - Automatic level shifter insertion when chaining registers from different voltage domains
  - Scan chain order by voltages



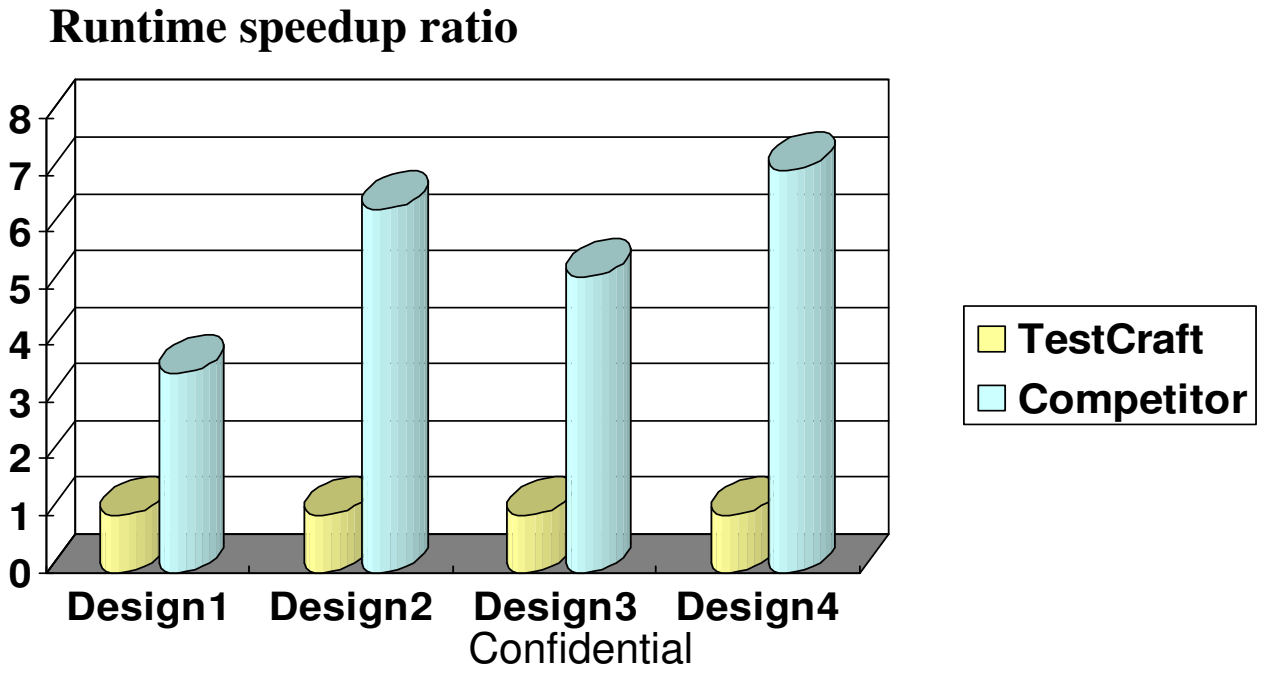
Enhancement for Low Power

- CPF interface support
- Auto library reading and target library link when sourcing CPF script
- Control of scan-chain crossing voltage domain
- Level-shifter Insertion control of scan-chain crossing voltage domain.
- Level shifter covering IO port and special voltage domain through IO of certain IP
- Support multi-bit scan cell to further reduce area/power

TestCraft Runtime Data

- Perform DFT rule checking, fixing, chaining, and reporting
- Runs 2x to 8x faster than others

Design1	1.4M logic instances, 90nm
Design2	2.8M logic instances; 90nm
Design3	5.4M logic instances; 65nm
Design4	6.2M logic instances; 65nm



Summary

- Complete integrated synthesis solution
  - Logic, Low Power, DFT
- Very fast runtime with big capacity
  - 2X to 5X faster than other solutions!
- Most aggressive reduction in chip area and power consumption
  - Up to 30% less synthesized gate counts
  - Up to 20% less power
- Many customer tape-outs in different applications
  - Communication, networking, wireless, consumer electronics, multi-media, graphics
  - Easy to adopt