

DIALITE™ PLATFORM

YOUR VERIFICATION RUNS ON-CHIP AND AT SPEED

→ BENEFITS

- **The widest choice of instruments** (15 instruments among 6 families of IP)
- **A unique productivity and flexibility** when combining the instruments, associating signal instruments and code fault finder or even embedding assertions
- **The true flow independency** as DiaLite exports RTL instrumented designs, while tighter integrations with pre-defined flow (Synthesis, Partitioning) can be achieved with TCL scripts
- **A complete & true collection of solutions for debug & verification:** 3 Editions that take into account the next generation of Debug tools: IP Reuse, System verification, Micro-testers (Protocol checkers, Bus navigators...)
- **Open and gifted for communication** based on standards (VHDL, System Verilog, TCL, C/C++, DCOM)
- **Assertions running On-Chip and at speed:** PSL and SVA are supported in DiaLite, being a major step in design verification. The DiaLite Assertions translator is a mature engine
- **Off-Chip instrumentation:** TemStorage allows to store high amount of test data traces outside the FPGA target
- **Incremental flow* compatibility** allowing to only compile your instrumentation partition
- **Easier to identify the signals that are traced** as DiaLite works at pre-synthesis level with source code reference, while keeping fast debugging

* Date of availability will be announced during 2007

OVERVIEW

DiaLite™ Platform is the most complete and powerful tool available on the market to verify and debug your SoC or FPGA:

- Trigger on design signal values and sample them at Design Speed
- Run RTL Code Debugger interface to your FPGA Design
- Re-use your Assertion Language Code from Simulation directly in your FPGA to spot system bugs
- Trace and check AMBA Bus Transaction On-Chip

VERIFICATION RUNNING ON CHIP AT DESIGN SPEED

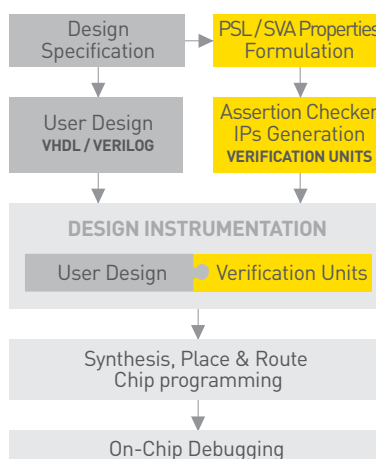
The Platform Edition includes all features of the Power Edge Edition plus the Assertion Checker (AC) module. This IP allows designers to embed their system assertion conditions along with their system specifications before synthesis and then check them at speed. While the system design is running, the assertion checker verifies the properties in real-time. A property failure will trigger the AC and open the corresponding debug interface with all the details for the verification of properties.

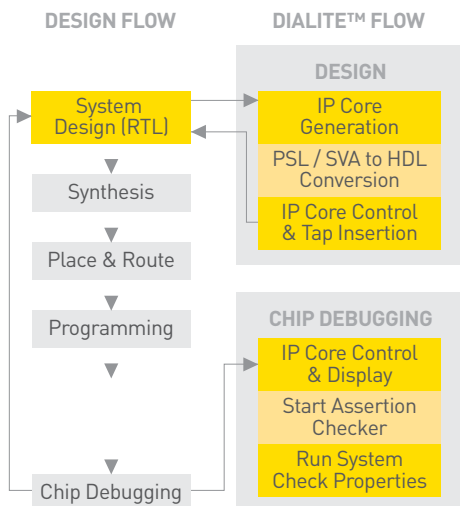
SMART & PRECISE TEMPORAL SEQUENCE ORIENTED VERIFICATION

This IP is built on the PSL and SVA standard, which makes all your formal verification tests and system properties reusable. Properties are derived from a temporal layer involving expressions or sequences. They allow verifying synchronous signals timings through easy, elegant and powerful semantics.

Unlike conventional formal verification, the "On-Chip Assertions" approach allows you to skip extensive processing run time and so cover possible behavior deviations at the system level.

This tool is thus well adapted to complex test scenarios involving race hazards and asynchronous events. While your design is running at full speed, the On-Chip Verification Process monitors and checks that your properties are not infringed. The cover directive even gives you metrication for your verification process.





INDEPENDENT FROM THE DESIGN FLOW

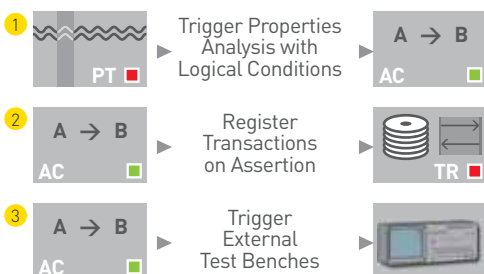
Designed to fit into any design flow that uses a VHDL or Verilog synthesis tool, DiaLite™ Platform Edition has been thought out to be seamlessly integrated.

During the design phase of your hardware, the DiaLite™ Core library allows you to choose and insert the Assertion Checker IP like any other IP. This AC core is simply generated from a PSL / SVA file. The connection and insertion into the VHDL or Verilog design are automatically performed by DiaLite™. After synthesis, you place and route using your usual design flow and finally the bitstreams are downloaded into the FPGA or SoC target. During the Chip debugging phase, the On-Chip AC is constantly watching the property status. A failure will instantly issue this information to your remote DiaLite™ environment and trigger a debugging window.

MUCH MORE THAN A STANDALONE IP!

The Assertion Checker IP is a powerful tool in itself but its capabilities are greatly amplified by the DiaLite™ Platform Edition environment. As part of a collection of IPs, the AC IP can be connected to a large set of instruments and allows the designer the ability to build an unlimited debugging project which can be finely controlled.

For example, you may have the Assertion Checker enabled by another IP. Let's imagine your system has a boot sequence that you don't want to be analyzed by the AC. In that case you can insert a trigger composed of the signals condition enabling the end of boot that will drive the AC IP ①. Of course, the AC IP can also drive other IPs like, for example, a History Register or a Transaction Register, if you want to capture events or track communications in a time window triggered by the AC ②. In fact you aren't limited to just IP communication. By using I/O device pins you can connect the AC output to external test benches: logic analyzers, bus protocol analyzers, etc ③. This way your instruments only record the transactions in which you are interested when a specific property condition is met.



→ ASSERTION CHECKER HIGHLIGHTS & BENEFITS

- PSL / SVA standards, On-Chip Real-Time and Real-Speed verification
- Reuse of your formal verification coming from "Assertion Based" CAD tools: Solidify™ (Averant), Safelogic Monitor® (Jasper Design Automation), ModelSim® SE (Mentor Graphics)...
- Timing oriented verification (Ex: Protocol State Machine)
- VHDL / Verilog generation, automatic IP connection & insertion
- In-depth observation without numerous synthesis loops
- Ensure test coverage of corner cases or bugs that would have remained undetected
- Measure functional coverage & get statistics on the verification process (cover directive)
- Find bugs earlier in the design cycle
- Facilitate debug in race hazards environments
- Fully integrated into DiaLite™ environment: AC can be interfaced with IPs or other external test benches

REUSE & BROWSE YOUR PROPERTIES

The Platform Edition provides a new way to verify your design. Verification using PSL properties or System Verilog assertions is now performed on-chip. By skipping simulation processing time, you are really going to verify faster. Even the GUI is designed to meet this objective: a property browser allows you to navigate through the PSL / SVA file and provides many facilities, such as the search with "regular expressions".

By giving you the opportunity to reuse your assertions coming from CAD "assertion based" simulation tools, DiaLite™ Platform allows the designer to directly take them to silicon level. Whatever the situation, implementing DiaLite™ Assertion Checker as part of the design process will considerably improve the quality of the design. It will also speed up time-to-market by skipping the processing time barrier required by formal verification.

DIALITE™ PLATFORM

ONLY SYNTHESIZE WHAT CHANGES!

The AC of the DiaLite™ Platform Edition brings you detailed diagnosis about a property in failure. For example, if you get a faulty property, you will know which part of it is causing the error. On-Chip debugging and verification is most commonly a step-by-step process where getting to the fault origin is synonymous with extra synthesis loops. The AC IP will get you to the fault faster! Each variable of a given property can be dynamically masked "on-chip". This way, designers can progress along the verification process by ignoring errors that have already been detected. By progressively masking the successive variables at fault, they can avoid going back to the synthesis step.

DiaLite™ also takes advantage of the incremental flow* compatibility. If your design is structured in different partitions, it will be easy to put the instrumentation into a dedicated partition. Changing instrumentation (IP and/or instrumented signals) will only have an impact on this block. Recompiling the instrumentation partition, and not the complete design, allows saving time and working with efficient iterative debugging.

AMBA BUS ON-CHIP VERIFICATION

It is a fact that most designs implant processor cores and thus embed buses. While many cores and IPs can communicate through these buses, signals tracing can greatly help designers to debug a HW/SW embedded system. DiaLite™ now introduces the first of a new generation of IPs: Bus Trace Analyzer (BTA) and Bus Protocol Checker (BPC*).

AMBA BUS TRACE ANALYZER

This IP is connected to the AMBA system bus and provides signal monitoring and bus tracing. Real-time tracing is achieved with a specific trace compression module, allowing different AMBA bus protocol abstraction level representations. Finally the trace data can be stored in on-chip memory or output to an off-chip memory device like TemStorage. The tracer can be set up through a JTAG port interface.

AMBA BUS PROTOCOL CHECKER*

This IP is also connected to the AMBA system bus. It is dedicated to check bus transactions and is composed of dedicated modules responsible for verifying different rules related to bus entities behaviors (master, slave, decoder, arbiter, signals...). The IP is thus able to check in real-time any default occurring in a bus transaction and to report it for further analysis and debugging.

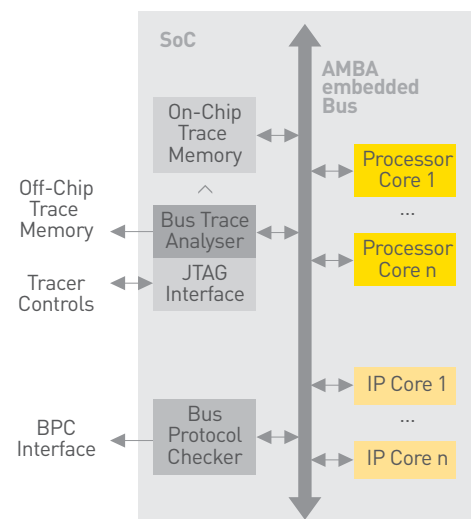
ALL SEGMENTS, FROM FPGA TO SOC

The DiaLite™ Platform Edition is the most complete environment among all DiaLite™ Editions. Now each DiaLite™ Edition provides the specific debugging and verification tools you need. They range from the basic logical instruments and waveform view to Assertion Checker, HDL Fault Finder and code view. All editions can be extended and complemented according to the verification level you expect and your device target, from small FPGA to SoC.

* Date of availability will be announced during 2007

→ PLATFORM HIGHLIGHTS

- Bus Tracer & Checker for AMBA AHB/APB
- Incremental flow compatibility for Altera & Xilinx targets
- Linux support
- Partitioning management on Multi-FPGAs platforms
- State Machine Viewer
- TemStorage integration: the 1GBytes / 128 Channels external memory solution for storing large amount of data coming from register-based IPs like HR or TR
- Support of Xilinx® Native TAP (Spartan™, Virtex™) and Altera® Native TAP (Stratix®, Cyclone™)
- Project Import/Export support to: Mentor Graphics® Precision™, Quartus® II, Synplify Pro®, Libero™, ISE™



→ DIALITE™ EDITIONS

	Leading Edge	Power Edge	Platform
RTL INSTRUMENTATION	•	•	•
DEBUG MANAGER	•	•	•
HDL FAULT FINDER	-	•	•
PSL / SVA ASSERTION CHECKER	-	-	•
AMBA BPA / BPC	op.	op.	op.

"•": included, "-": non included, "op.": optional

→ DIALITE™ IP CORES INSTRUMENTATION LIST

IP FAMILY	IP NAME	USE AND BENEFITS
Property Verification	Assertion Checker(AC)	Allows the verification of system properties written in PSL / SVA. Automatic insertion of the VHDL or Verilog Verification Unit corresponding to PSL or SV assertions into the design. At-speed and interactive debugging allows knowing the exact part of the property in failure and proceeding by forcing its state without re-synthesis. Metrication on property cover is also offered.
RTL Logic Debug	HDL Fault Finder (FF)	Allows accurate monitoring and display of logic events contained in your HDL code that can be traced by inserting Watchpoints and Breakpoints into the source (Option).
RTL Logic Debug	Switches / Leds	Allows interactively observing internal signal values and/or driving them to the desired value.
RTL Logic Debug	User Logical Module (ULM)	Allows users to insert or to define their own triggering functions from VHDL or Verilog descriptions. This customized instrumentation can be used either to combine DiaLite™ standard triggers or to detect specific events (State Machine sequences, assertions...).
Logic Analyzer/ Trigger	Glitch Detector (GD)	Allows glitch tracking on sets of signals and generates synchronization for other instruments (internal or external) on the first or more occurrence of a glitch, using pulse or flag mode.
Logic Analyzer/ Multi Conditional Trigger (MCT)	Logic Equation Module (LEM)	Basic qualifier generator, using a real-time adjustable logic equation between a set of two signals or trigger outputs to generate a complex measurement window. Can be chained using multiple LEM and ULM to create a multiple signal logic combination and MCT.
Logic Analyzer/ Trigger	Parallel Trigger (PT)	Allows pattern recognition on a parallel bank of signals and generates synchronization for other instruments (internal or external) on the first or more occurrence of the expected pattern, using pulse or flag mode.
Logic Analyzer/ Trigger	Serial Trigger (ST)	Allows the serial pattern recognition on a signal chosen from a bank of signals and generates synchronization for other instruments (internal or external) on the first or more occurrence of the expected pattern, using pulse or flag mode.
Logic Analyzer/ Memory Register	History Register (HR)	Basic recording capability, based on RAM or registers (according to FPGA resources available) allows building a sophisticated logic analyzer with preceding triggers (in flag mode) and logic equations modules. HR can be associated with Glitch Monitoring capabilities.
Logic Analyzer/ Transaction Register	Transaction Register (TR)	Advanced recording capability based on FPGA RAM blocks allowing the recording of a transaction whatever its duration. Defined by Triggers and Logic Equation Modules, TR can track and capture transactions for long periods of time while saving internal memory resources.
Counter	Counter (CTR)	Allows to trigger on an event after a fixed duration or after a fixed occurrence of an event. It is also possible to trigger if a signal pulse is too short.
Bus Monitoring	Bus Range Checker (BRC)	Allows capturing any value included inside or outside a given range defined by two values or a value higher or lower than a user-defined constant.
Bus Monitoring	Bus Trace Analyzer (BTA)	Allows monitoring and dumping bus trace after resolution encoding and data compression computing. Data trace is stored On or Off Chip for further analysis.
Bus Monitoring	Bus Protocol Checker (BPC)*	Allows checking bus transactions according to a set of defined rules related to bus entities behaviors (master, slave, arbiter...).
Bus Monitoring	Traffic Analyzer (TA)	Analyzes bus traffic on-chip. Monitors DMA cycles (read, write, or all cycles), measures traffic intensity or bus occupancy. Tracks any faulty bus (stuck, one sense only or saturated). Provides statistics over a long observation period.
Design Robustness	PseudoRandom Generator (PRG)	Allows the generation of pseudo random patterns on one or more signals to stimulate designs randomly and to check their robustness.

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www.temento.com

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