Turbo-MSIM™

High Speed and High Capacity Circuit Simulator

Legend's Products

- IP Library Characterization Products
  - Charflo-Cell!™ : *Automatic Cell/IO Library Characterization*
  - Charflo-Memory!™: *Automatic Memory Characterization*
- IP Library Model Quality Assurance Products
  - Model Diagnoser™

    Cell/IO Library .Lib Quality Assurance and Defect Repair
- Circuit Simulation Products
  - MSIM®: Accurate-Spice Simulator
  - Turbo-MSIM™: Fast-Spice Simulator

MSIM® Certifications

- MSIM certified by TSMC's Spice Tool Qualification Program

  http://www.legenddesign.com/BW/021009.shtml
- MSIM certified by TSMC's TMI (TSMC Model Interface) Qualification Program

Turbo-MSIM™ Introduction

Turbo-MSIM is a leading-edge Fast Spice circuit simulator with

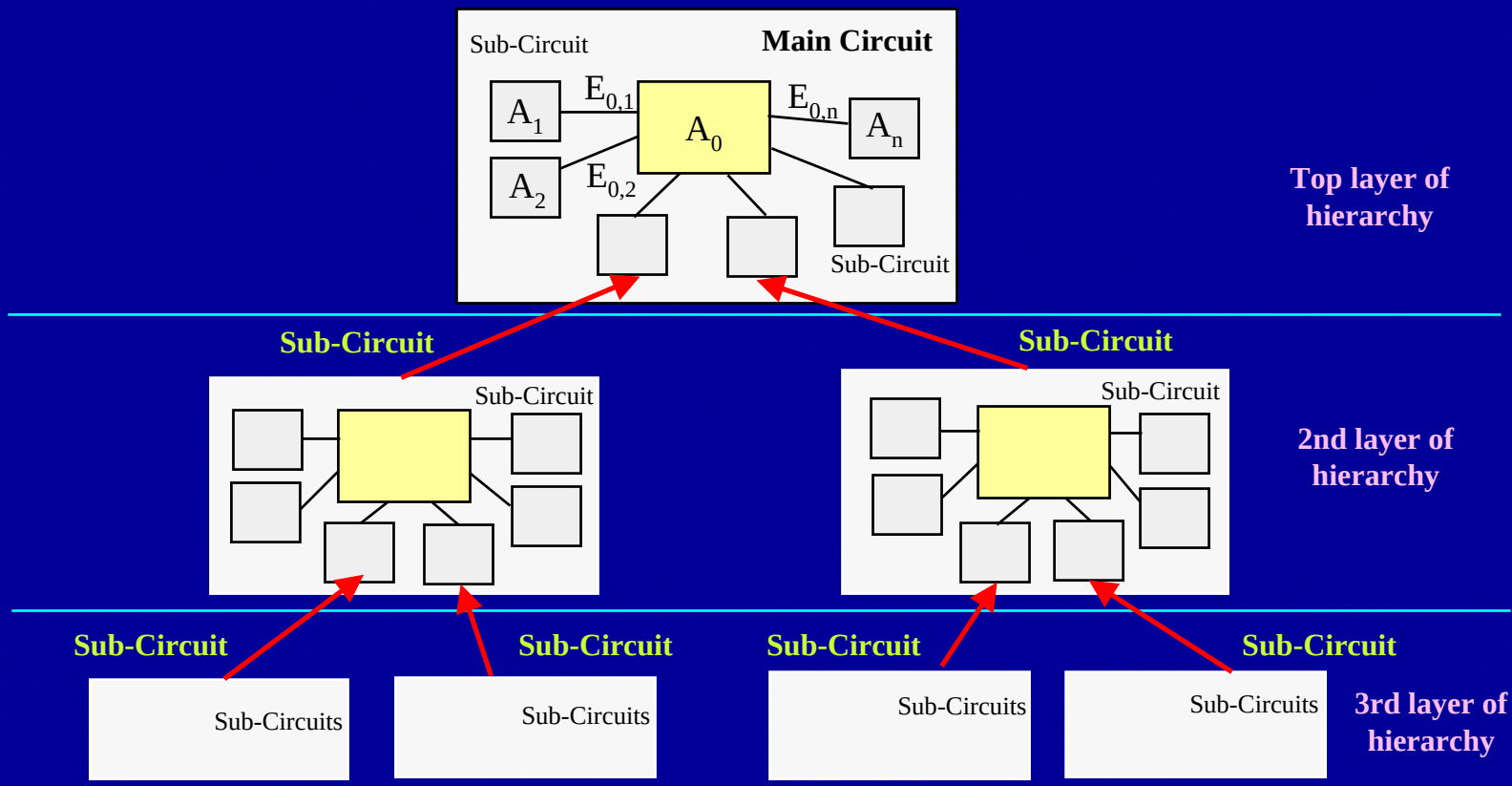
- Super high speed
- Extremely large capacity
- Exceptional accuracy
- Extensive model support
- Multi-threaded applications on multi-core computer
- Automatic matrix solver selector for throughputs
- Full-scope applications including digital/ analog/ mixed-signal designs, and hierarchical/flatten netlists

Turbo-MSIM™ Technology

- Mixed use of tabular and equation device models
- Hierarchical structures for running large circuits
- Circuit partition for tightly-grouped sub-matrices
- Multi-rate for simulating sub-matrices efficiently
- Event-driven (latency) for running active circuits only
- Isomorphism recognition and simulation results re-use
- Analog-nature subcircuits recognition and re-grouping
- Advanced RC reduction
- Innovative algorithms and structures for optimizing performance and minimizing memory usage

Hierarchical Structure

Enable Huge Circuit Simulation

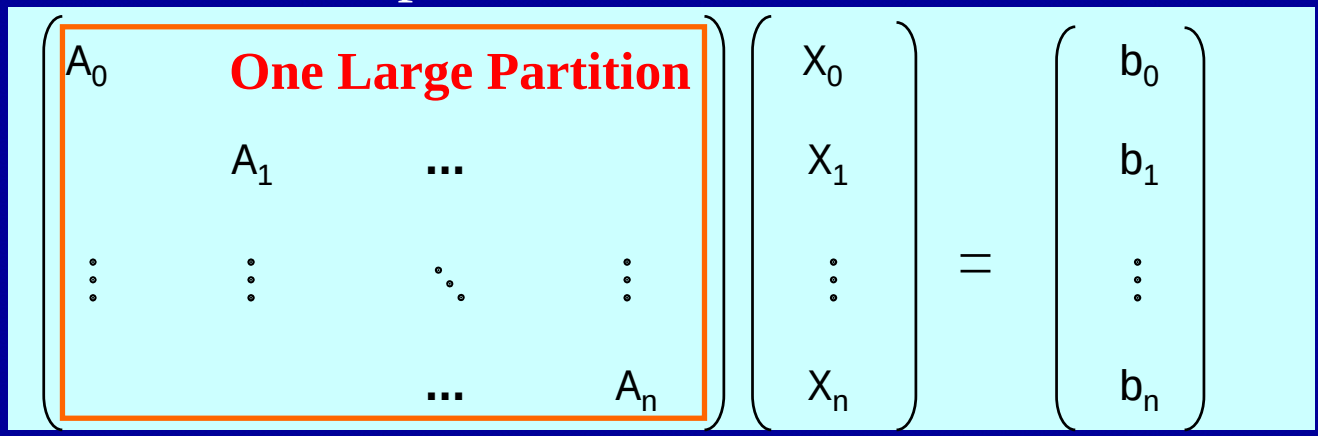


Simulation operations and memory spaces can be greatly reduced!

Circuit Partition

Build Tightly-grouped Sub-matrices

- Conventional Spice Simulator



- Fast Spice Simulator

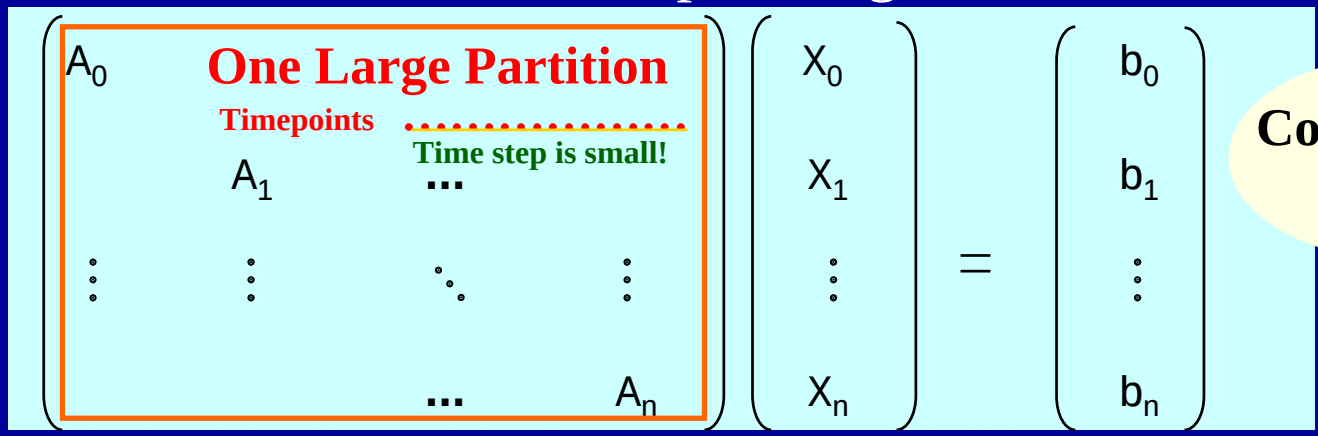
$$A_0 X_0 = b_0$$
$$A_1 X_1 = b_1$$
$$\ldots$$
$$A_n X_n = b_n$$

Many Small Partitions

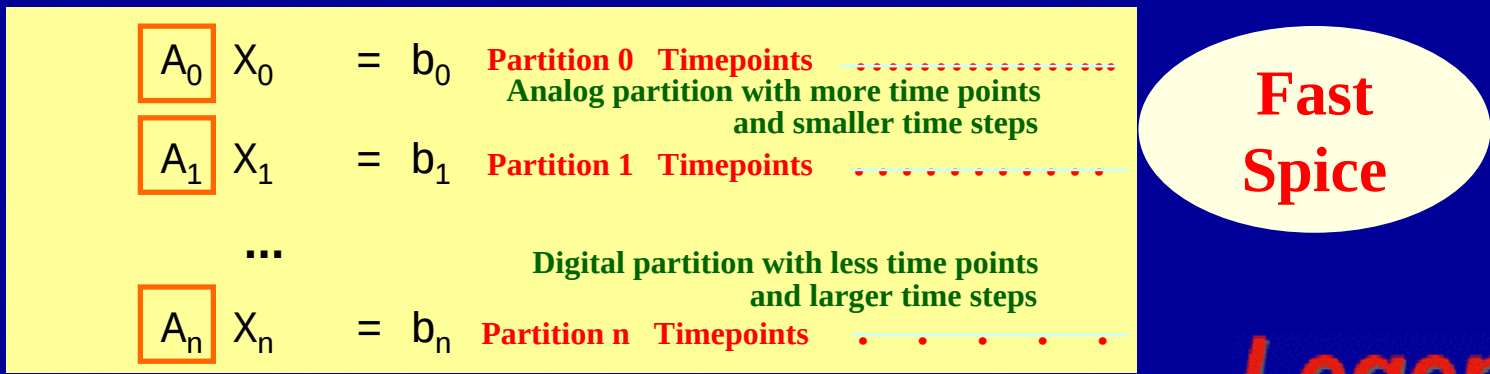
Solving small matrices is faster and less memory used.

Multi-Rate Control
Optimize Sub-matrix Simulation

- Use the minimum time step among all sub-matrices



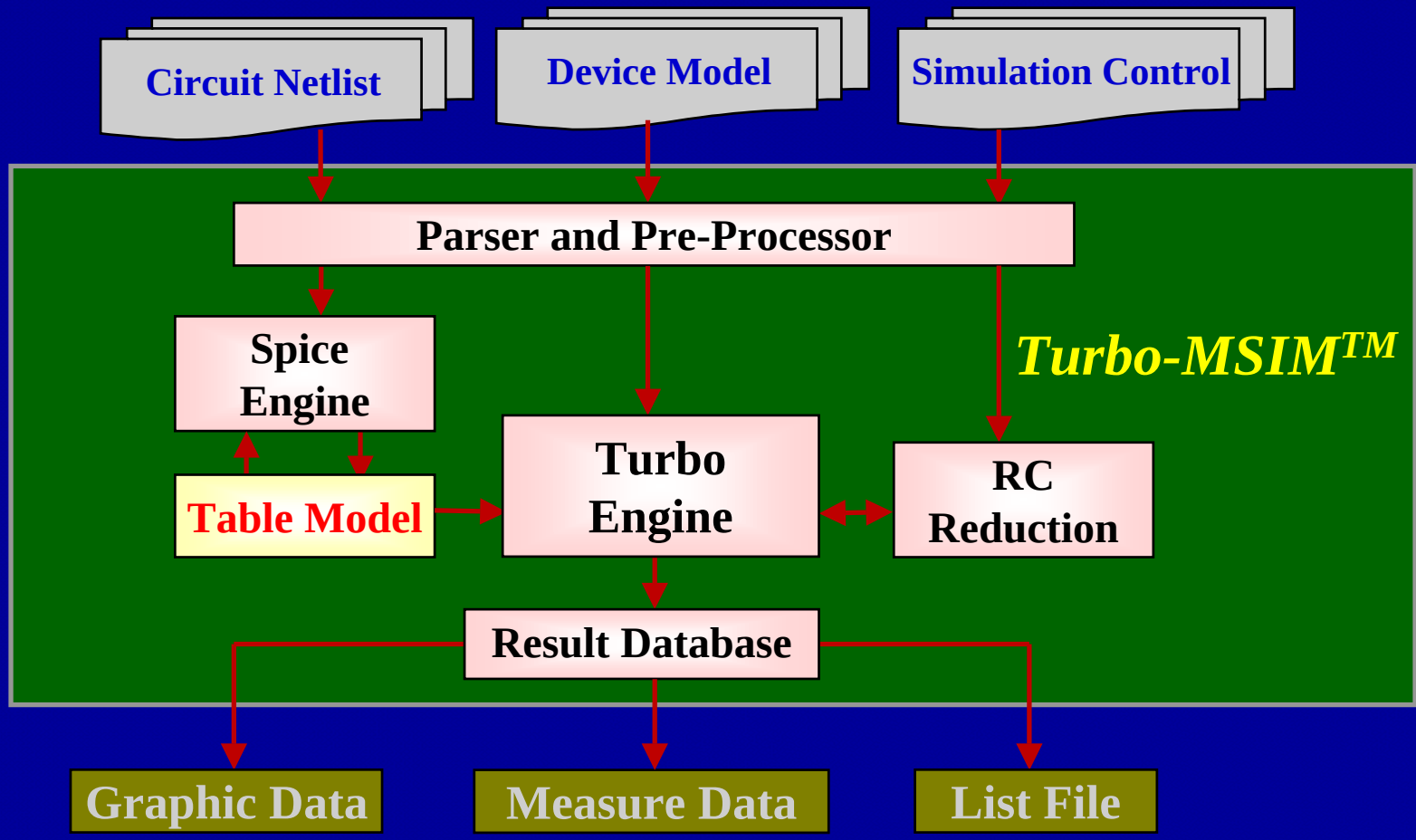
- Each partition has its own time step and control



Turbo-MSIM™ Applications

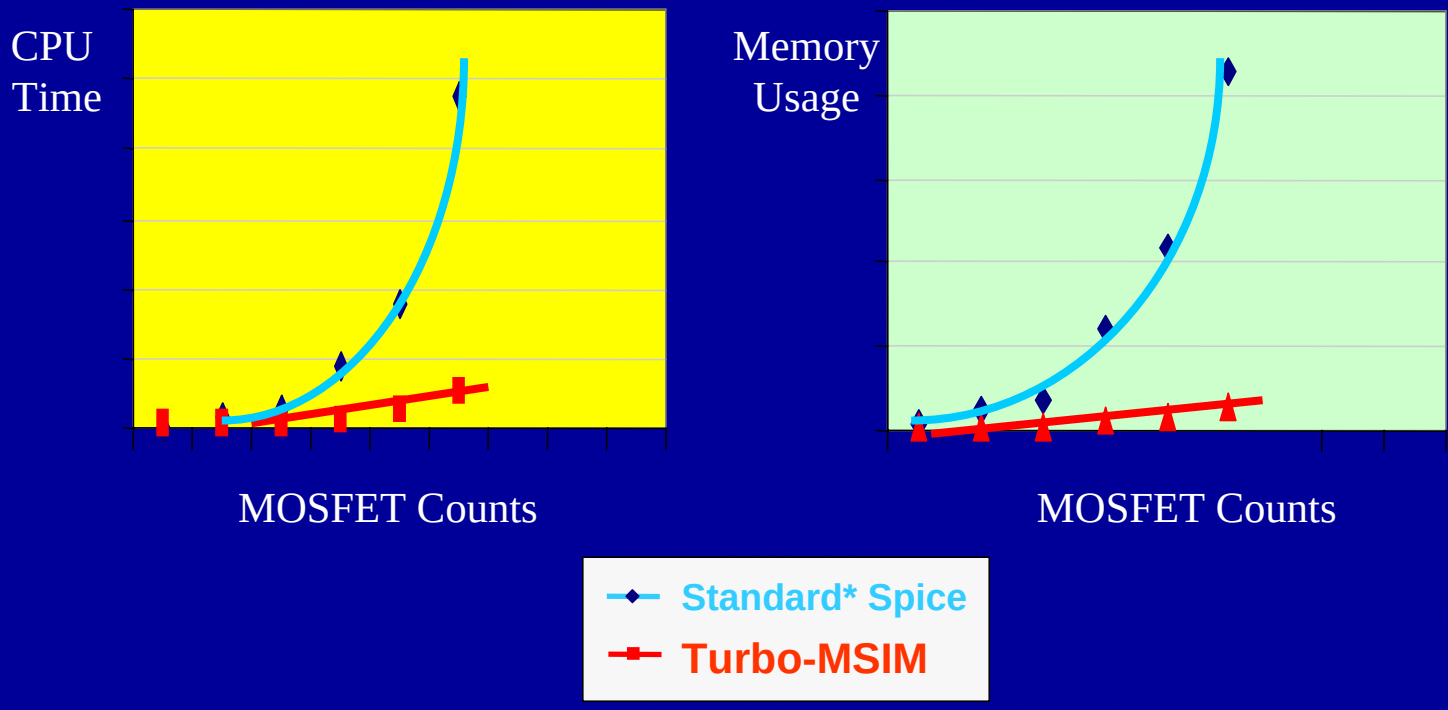
- Mixed-signal circuit designs
- Memory circuit designs
- Complex IO circuit designs
- Hierarchical circuit simulation/verification
- Post-Layout circuit simulation/verification
- Timing, power and noise analysis

Turbo-MSIM™ Flow



Turbo-MSIM™ vs SPICE

Performance and Memory Usage



** Standard means the most popular Spice simulator*

Turbo-MSIM™
Extensive Modeling Support

- Turbo-MSIM delivers silicon-accurate models with proven implementations of
  - * BSIM3
  - * BSIM4
  - * BSIM4 SOI
  - * HiSIM1 and HiSIM2
  - * RPI TFT
- Direct access of updated SPICE models from
  - * TSMC
  - * UMC
  - * IBM
  - * Chartered
  - * SMIC
  - * Tower

Turbo-MSIM™ Multi-Thread

Multi-Core and Parallelism Support

- Enable multi-threaded application on a multi-core configuration
- Utilize the multi-thread functions for decomposing and solving matrices, and calculating device model
- Parallelize the parameter sweeping jobs like .DATA/.MONTE/.DC/.AC
- Prove its outstanding efficiency on the circuits with a large number of extracted post-layout parasitics

Turbo-MSIM™ Maxtrix Solving

Automatic Matrix Solver Selector

- Conventionally, sparse matrix solving technique is used to take advantage of the sparse in circuit matrix for the efficiency
- For nanometer technology, sparse matrix solving technique could be not efficient for the layout extracted circuits with large RC networks
- A Matrix Solver Selector has been implemented in Turbo-MSIM, for simulation throughputs.

Speed/Accuracy Benchmark
With Accurate-Spice

Circuit Type: High-Speed SRAM

Type	MOS Count	Standard* CPU Time	Turbo-MSIM CPU Time	Speed Up	Accuracy
Circuit 1	31,741	11,707 sec	37 sec	**319 X**	**0.66 %**
Circuit 2	57,079	21,483 sec	46 sec	**467 X**	**1.50 %**
Circuit 3	110,567	73,355 sec	78 sec	**942 X**	**0.37 %**
Circuit 4	3,176,890	N/A	208 sec	N/A	N/A
Circuit 5#	12,636,544	N/A	34 sec	N/A	N/A
Circuit 6#	50,546,176	N/A	99 sec	N/A	N/A

* Standard means most popular Spice simulator
\# No resistors and highly repeated memory cell structure

Speed/Accuracy Benchmark

With Other Fast-Spice

Circuit Type	Turbo-MSIM CPU Time	Other* CPU Time	Turbo-MSIM Memory Use	Other* Memory Use	Diff.
65nm SRAM	4,217 sec	Fail	1,969 MB	**Out of Mem.**	-
65nm SRAM	359 sec	1,099 sec	638 MB	1,614 MB	1.50 %
90nm SRAM	317 sec	1,414 sec	482 MB	827 MB	1.42 %
0.13um SRAM	304 sec	824 sec	188 MB	173 MB	1.73 %
90nm HSTL	131 sec	329 sec	229 MB	802 MB	1.73 %
90nm SMBUS	15.6 sec	52 sec	42 MB	156 MB	0.05%

* Other means the most popular fast Spice simulator

Speed/Accuracy Benchmark
With Other Analog Fast-Spice

- Layout-extracted PLL based on TSMC 90nm process
  10,916 MOSFETs, 48,722 Capacitors, 19,191 Resistors

Benchmark Data	Turbo-MSIM	Other Analog Fast-Spice	Standard* Accurate Spice
Accuracy *Max-Min Cycle*	5ps	7ps	0 ps
CPU Time	10 hrs	36 hrs	172 hrs

- Turbo-MSIM speed-up over other analog Fast-Spice
  3.6X
- Turbo-MSIM speed-up over standard Accurate-Spice
  17.2X

* Standard means most popular Accurate-Spice simulator

Turbo-MSIM™ Success
10 Bit ADC Circuit Simulation

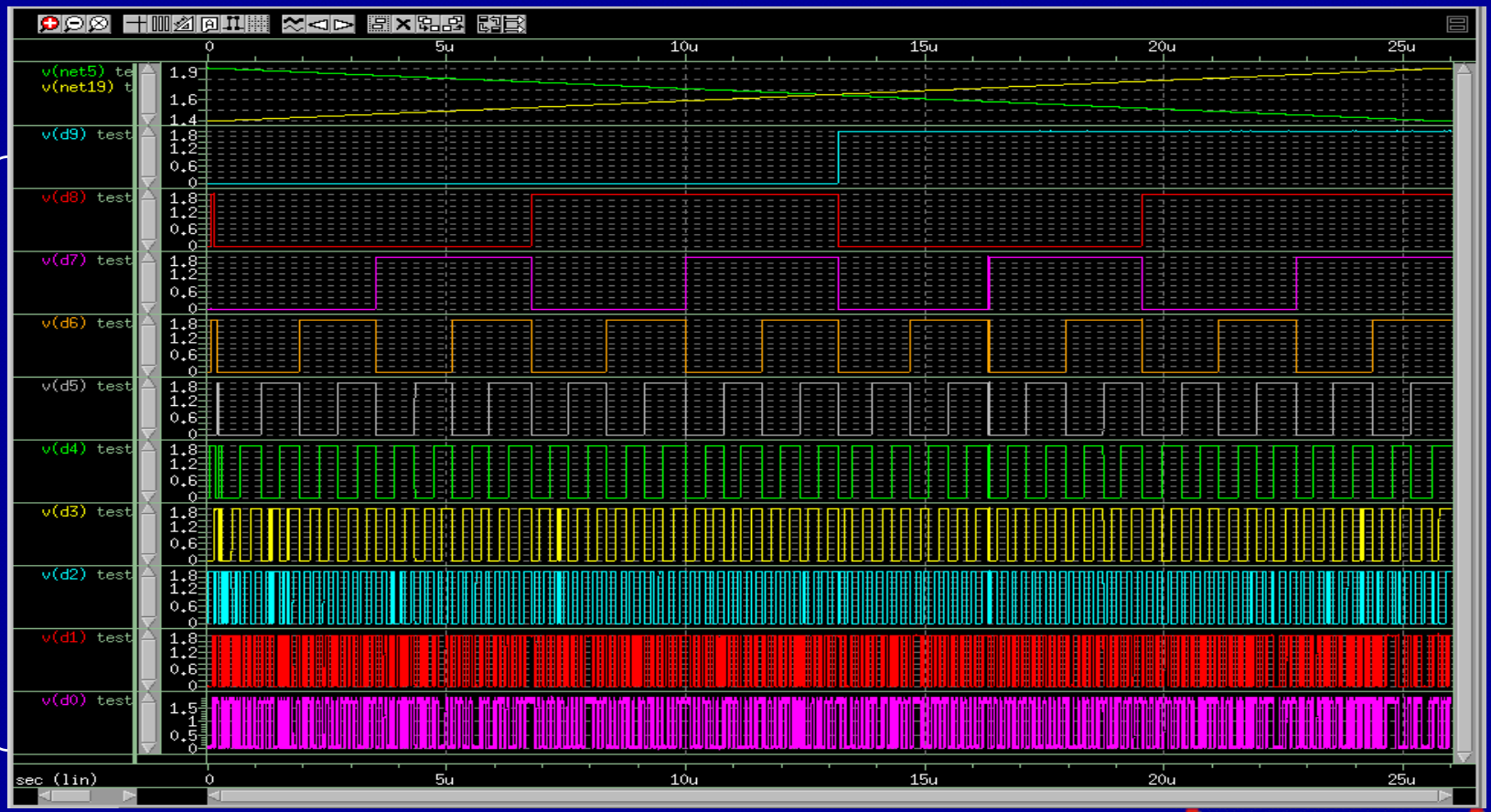
- 10 Bit ADC circuit data
  - Number of transistors: 4,150
  - Number of capacitors: 381
  - Total nodes: 2,110
- Simulation period: 26 us
- CPU Time Data
  - Conventional Spice: 86,362 sec
  - Turbo-MSIM: 6,596 sec

Turbo-MSIM™ Success

10 Bit ADC Circuit Simulation

Input voltage

10bits

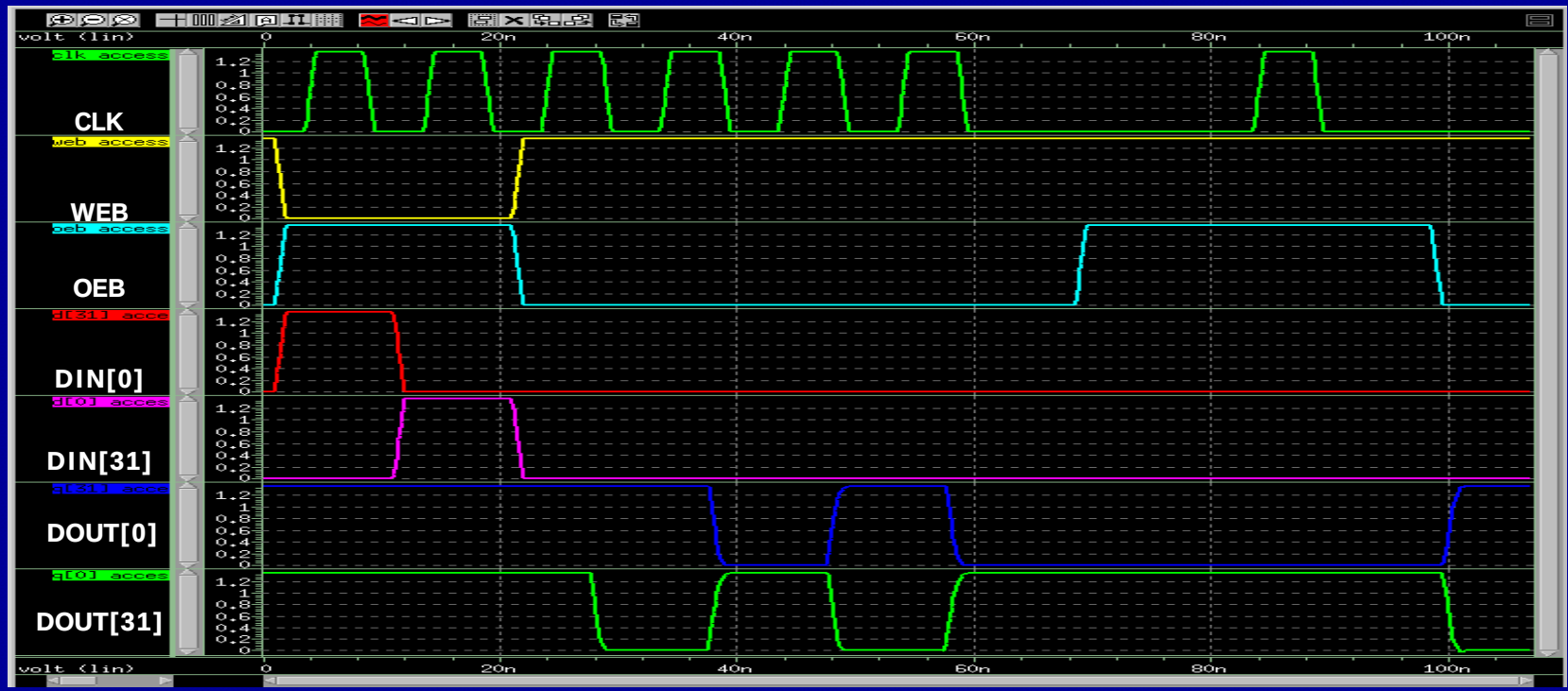


Technology Leader in IP Characterization and IC/PCB Simulation

Legend Design Technology

Turbo-MSIM™ Success

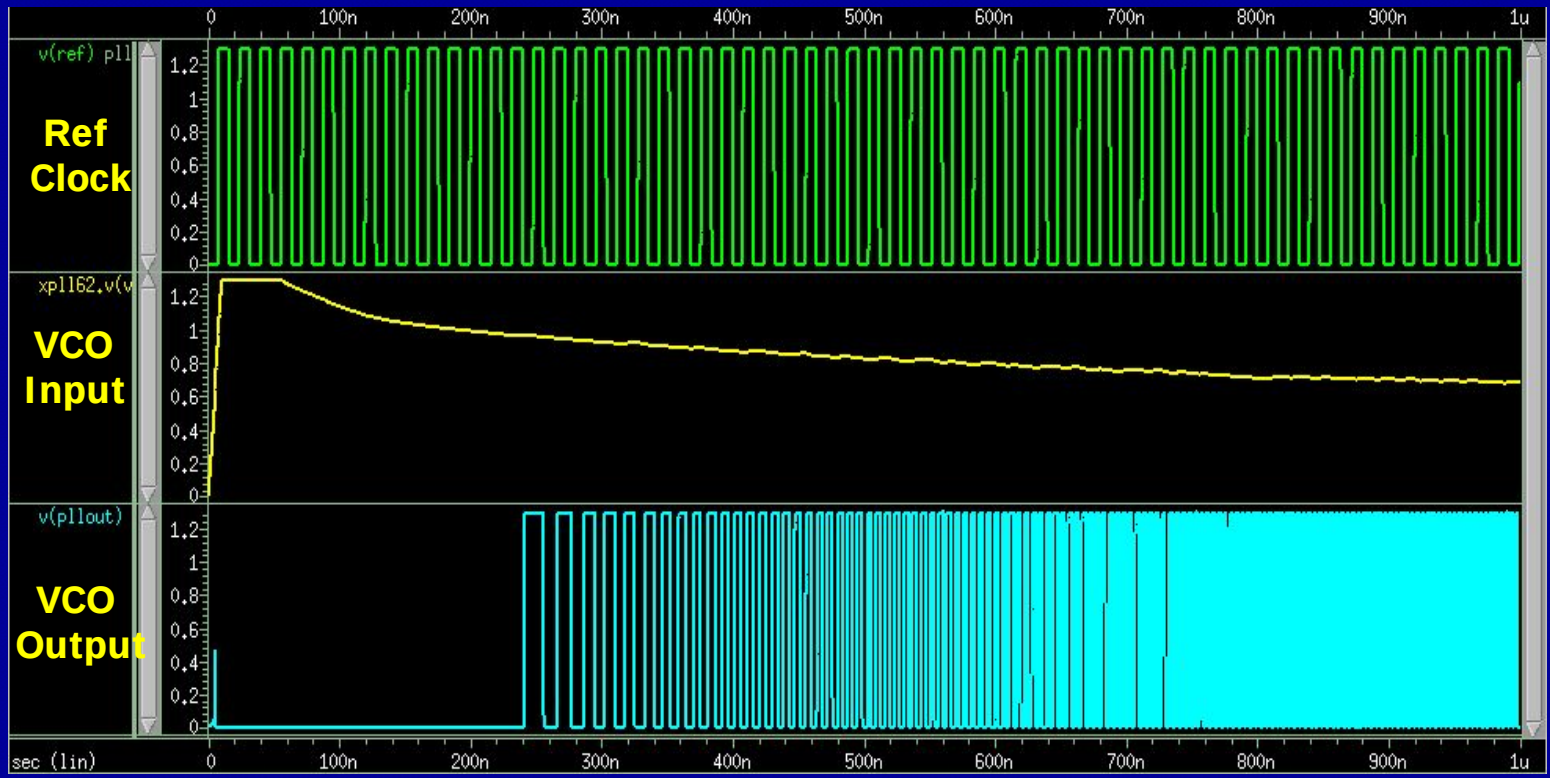
3 Million MOSFET SRAM Simulation



Single-Port 16Kx32 SRAM

Turbo-MSIM™ Success

Fast and Accurate PLL Simulation



58 minutes and < 3% accuracy

Turbo-MSIM™ Success

Mixed mode LCD Display Controller

- Mixed mode LCD display controller SoC
  - Multiple voltage sources. (15v, 3.3v)
  - Embedded DRAM (768k bits)
  - Number of transistors: 2,053,916
  - Number of capacitors: 1,572,878
  - Total nodes: 1,835,434

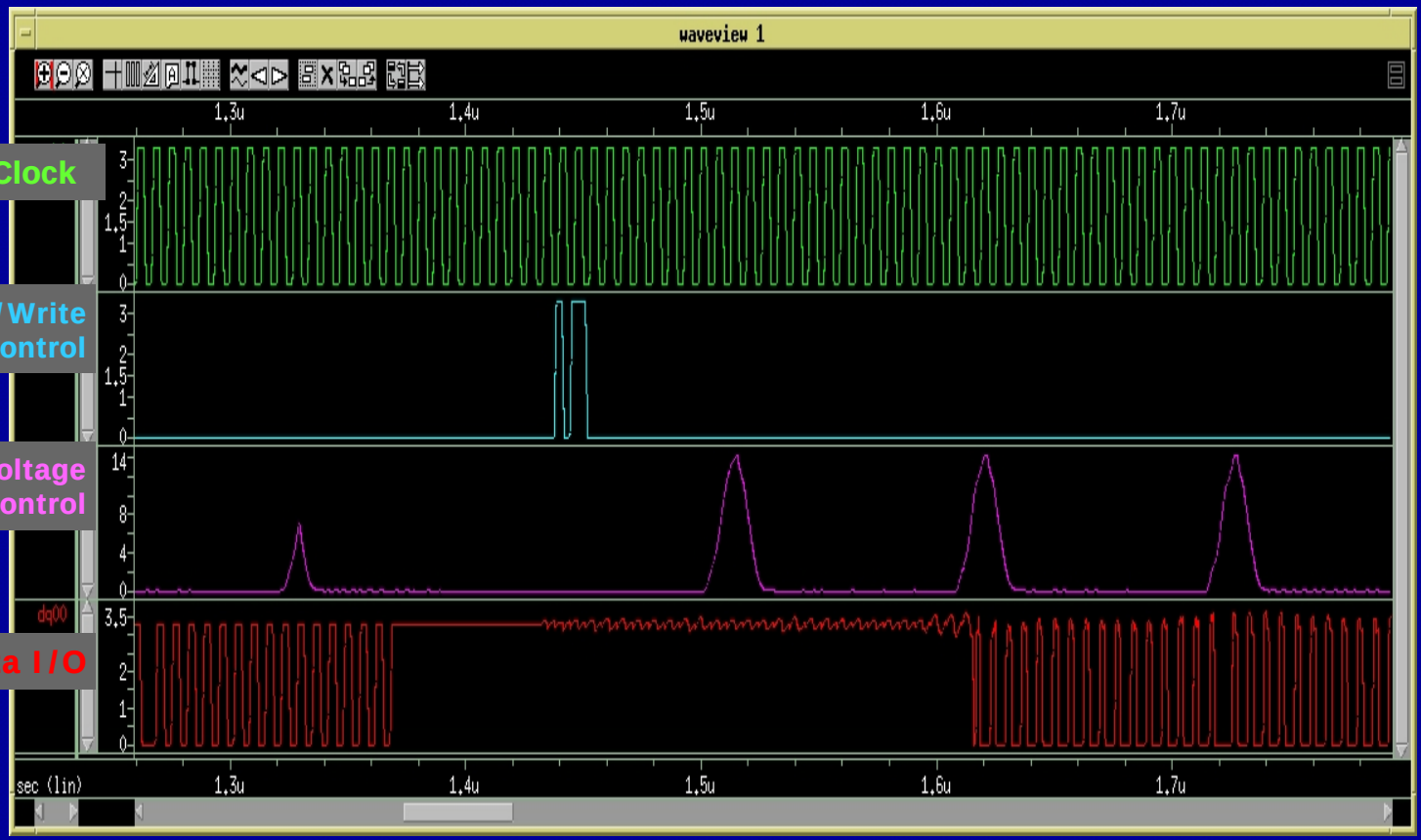
Simulations Goals

Mixed mode LCD Controller

- Functional verification
  - Verify full-chip functionality
  - Verify analog block functionality
- Ground bounce simulation
  - Verify full-chip functionality with ground bounce
  - Simulate inductance and coupling effects

Simulation Waveforms

Mixed mode LCD Controller

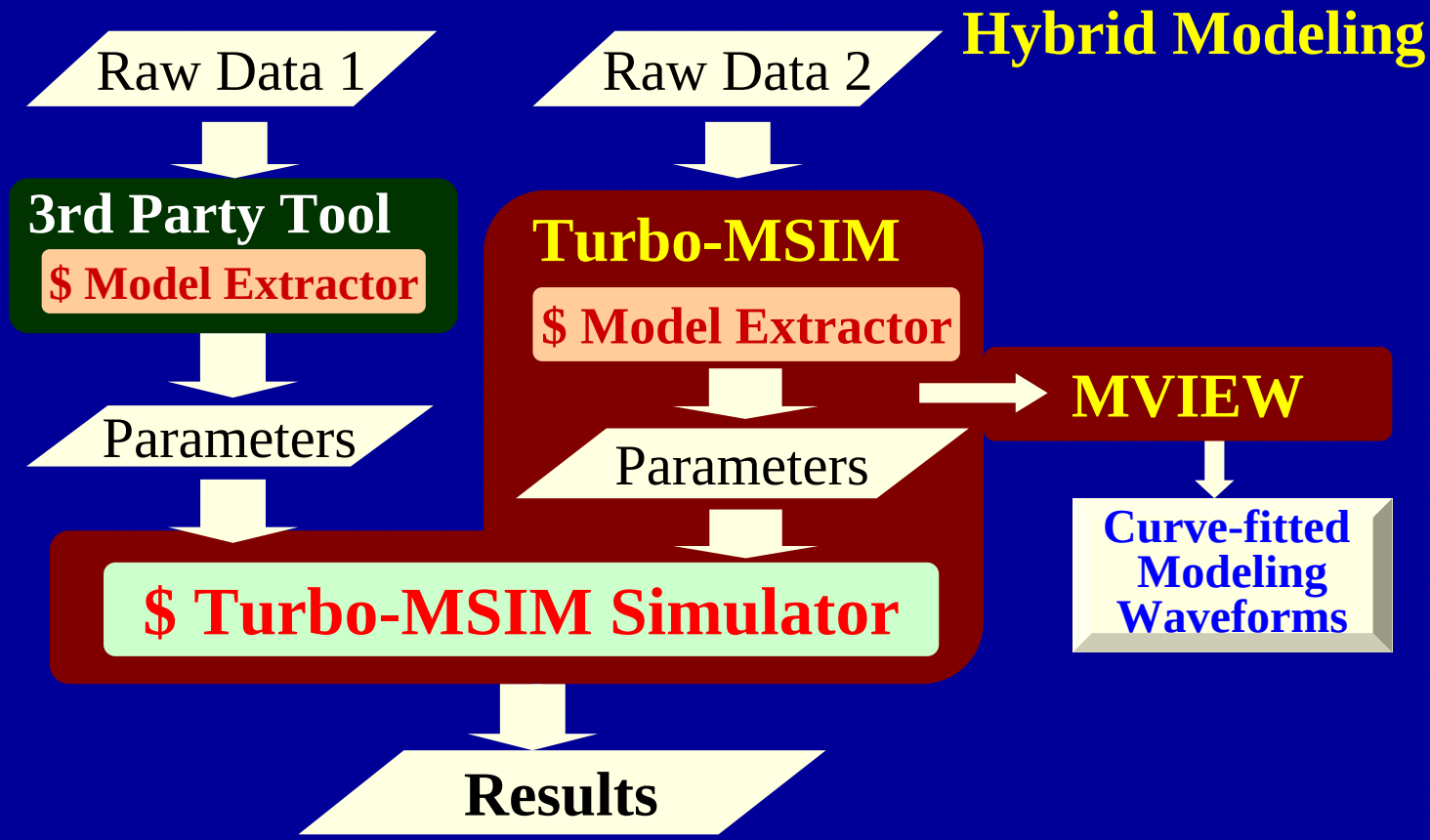


Special Model Support

- Verilog-A model
- CMI (Common Model Interface) model
- TMI (TSMC Model Interface) model
- LCD panel model
- TFT advanced model

Hybrid Modeling Flow

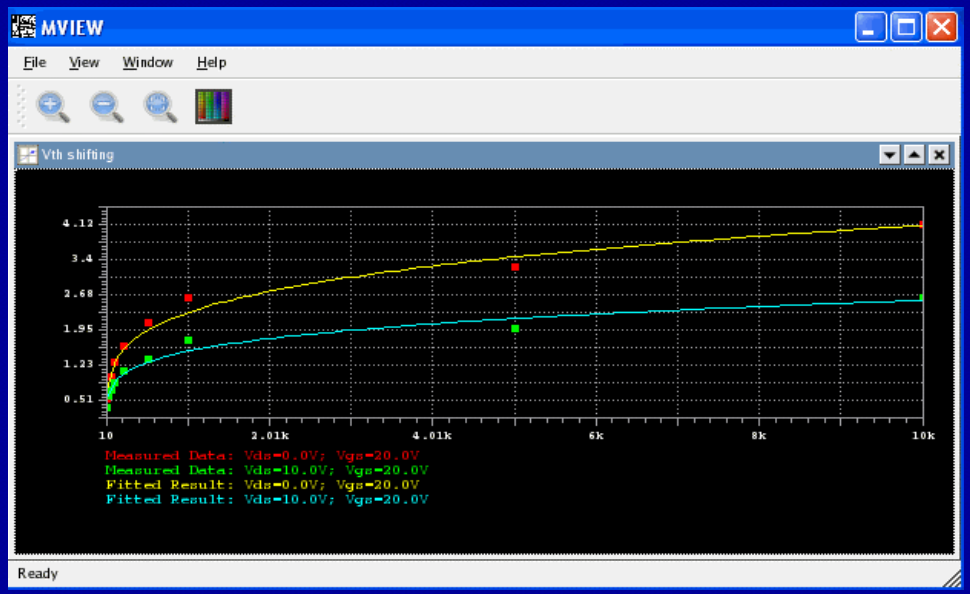
A Complete Device Modeling Solution



Hybrid Modeling Example

Model Parameters by Curve Fitting

Advanced Threshold Voltage Shift Model

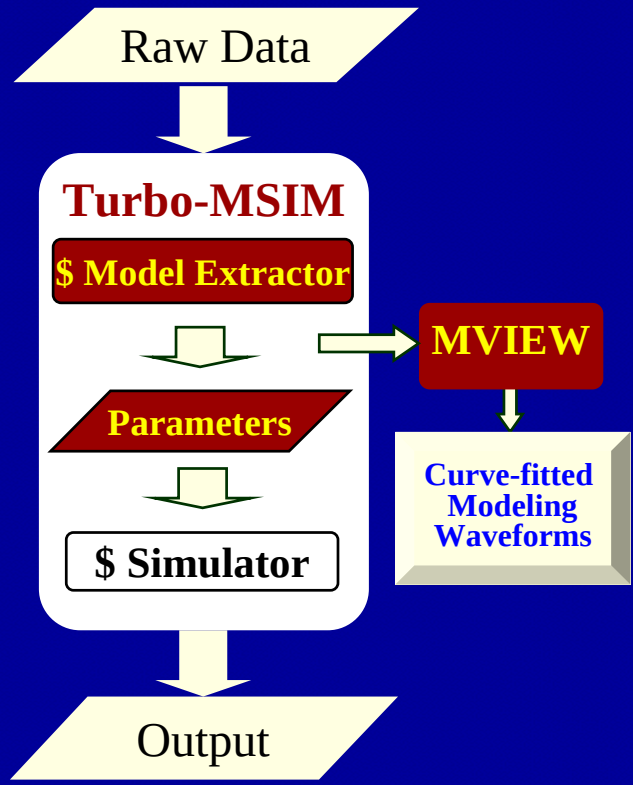


Parameters extracted from Turbo-MSIM built-in Model Extractor by curve-fitting

A = 0.0280863

β = 0.247142

Turbo-MSIM Hybrid Flow



Turbo-MSIM™ Platforms

- Redhat Enterprise Linux
- Windows XP
- Solaris on X86

Turbo-MSIM™ Benefits

- Enhancing design productivity

  Reduce simulation time from days to hours/minutes
- Full-chip hierarchical simulation for timing and power analysis
- Fast post-layout circuit verification with extracted RCs in SPICE/DSPF format
- Scalable accuracy, performance and capacity
- Superior price-performance