Turbo-MSIM™
High Speed and High Capacity Circuit Simulator
Legend’s Products

◆ IP Library Characterization Products
  - Charflo-Cell!™: *Automatic Cell/IO Library Characterization*
  - Charflo-Memory!™: *Automatic Memory Characterization*

◆ IP Library Model Quality Assurance Products
  - Model Diagnoser™
    *Cell/IO Library .Lib Quality Assurance and Defect Repair*

◆ Circuit Simulation Products
  - MSIM®: Accurate-Spice Simulator
  - Turbo-MSIM™: Fast-Spice Simulator

*Legend*

*Technology Leader in IP Characterization and IC/PCB Simulation*
MSIM® Certifications

- MSIM certified by TSMC’s Spice Tool Qualification Program
  http://www.legenddesign.com/BW/021009.shtml

- MSIM certified by TSMC’s TMI (TSMC Model Interface) Qualification Program

Technology Leader in IP Characterization and IC/PCB Simulation
Turbo-MSIM™ Introduction

Turbo-MSIM is a leading-edge Fast Spice circuit simulator with

• Super high speed
• Extremely large capacity
• Exceptional accuracy
• Extensive model support
• Multi-threaded applications on multi-core computer
• Automatic matrix solver selector for throughputs
• Full-scope applications including digital/ analog/ mixed-signal designs, and hierarchical/flatten netlists

Technology Leader in IP Characterization and IC/PCB Simulation
Turbo-MSIM™ Technology

- Mixed use of tabular and equation device models
- Hierarchical structures for running large circuits
- Circuit partition for tightly-grouped sub-matrices
- Multi-rate for simulating sub-matrices efficiently
- Event-driven (latency) for running active circuits only
- Isomorphism recognition and simulation results re-use
- Analog-nature subcircuits recognition and re-grouping
- Advanced RC reduction
- Innovative algorithms and structures for optimizing performance and minimizing memory usage

Technology Leader in IP Characterization and IC/PCB Simulation
Hierarchical Structure
Enable Huge Circuit Simulation

Simulation operations and memory spaces can be greatly reduced!
Circuit Partition
Build Tightly-grouped Sub-matrices

- Conventional Spice Simulator
  \[
  \begin{pmatrix}
  A_0 & \text{One Large Partition} \\
  A_1 & \ldots \\
  \vdots & \vdots \\
  \text{...} & A_n
  \end{pmatrix}
  \begin{pmatrix}
  x_0 \\
  x_1 \\
  \vdots \\
  x_n
  \end{pmatrix}
  =
  \begin{pmatrix}
  b_0 \\
  b_1 \\
  \vdots \\
  b_n
  \end{pmatrix}
  \]

- Fast Spice Simulator
  Many Small Partitions
  \[
  A_0 \begin{pmatrix} x_0 \end{pmatrix} = b_0
  \]
  \[
  A_1 \begin{pmatrix} x_1 \end{pmatrix} = b_1
  \]
  Solving small matrices is faster and less memory used.
  \[
  \text{...}
  \]
  \[
  A_n \begin{pmatrix} x_n \end{pmatrix} = b_n
  \]
Multi-Rate Control
Optimize Sub-matrix Simulation

- Use the minimum time step among all sub-matrices

\[
\begin{pmatrix}
A_0 & A_1 & \cdots & A_n \\
\end{pmatrix}
\begin{pmatrix}
X_0 \\
X_1 \\
\vdots \\
X_n \\
\end{pmatrix}
= 
\begin{pmatrix}
b_0 \\
b_1 \\
\vdots \\
b_n \\
\end{pmatrix}
\]

- Each partition has its own time step and control

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Turbo-MSIM™ Applications

- Mixed-signal circuit designs
- Memory circuit designs
- Complex IO circuit designs
- Hierarchical circuit simulation/verification
- Post-Layout circuit simulation/verification
- Timing, power and noise analysis
Turbo-MSIM™ Flow

- Circuit Netlist
- Device Model
- Simulation Control

Parser and Pre-Processor

- Spice Engine
- Table Model
- Turbo Engine
- RC Reduction

Result Database

- Graphic Data
- Measure Data
- List File

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Turbo-MSIM™ vs SPICE
Performance and Memory Usage

CPU Time

Memory Usage

MOSFET Counts

MOSFET Counts

* Standard means the most popular Spice simulator

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Turbo-MSIM™
Extensive Modeling Support

- Turbo-MSIM delivers silicon-accurate models with proven implementations of
  - BSIM3
  - BSIM4
  - BSIM4 SOI
  - HiSIM1 and HiSIM2
  - RPI TFT

- Direct access of updated SPICE models from
  - TSMC
  - UMC
  - IBM
  - Chartered
  - SMIC
  - Tower
Turbo-MSIM™ Multi-Thread Multi-Core and Parallelism Support

- Enable multi-threaded application on a multi-core configuration
- Utilize the multi-thread functions for decomposing and solving matrices, and calculating device model
- Parallelize the parameter sweeping jobs like .DATA/.MONTE/.DC/.AC
- Prove its outstanding efficiency on the circuits with a large number of extracted post-layout parasitics
Turbo-MSIM\textsuperscript{TM} Maxtrix Solving
Automatic Matrix Solver Selector

\begin{itemize}
  \item Conventionally, sparse matrix solving technique is used to take advantage of the sparse in circuit matrix for the efficiency
  \item For nanometer technology, sparse matrix solving technique could be not efficient for the layout extracted circuits with large RC networks
  \item A Matrix Solver Selector has been implemented in Turbo-MSIM, for simulation throughputs.
\end{itemize}
Speed/Accuracy Benchmark
With Accurate-Spice

<table>
<thead>
<tr>
<th>Type</th>
<th>MOS Count</th>
<th>Standard* CPU Time</th>
<th>Turbo-MSIM CPU Time</th>
<th>Speed Up</th>
<th>Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit 1</td>
<td>31,741</td>
<td>11,707 sec</td>
<td>37 sec</td>
<td>319 X</td>
<td>0.66 %</td>
</tr>
<tr>
<td>Circuit 2</td>
<td>57,079</td>
<td>21,483 sec</td>
<td>46 sec</td>
<td>467 X</td>
<td>1.50 %</td>
</tr>
<tr>
<td>Circuit 3</td>
<td>110,567</td>
<td>73,355 sec</td>
<td>78 sec</td>
<td>942 X</td>
<td>0.37 %</td>
</tr>
<tr>
<td>Circuit 4</td>
<td>3,176,890</td>
<td>N/A</td>
<td>208 sec</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Circuit 5#</td>
<td>12,636,544</td>
<td>N/A</td>
<td>34 sec</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Circuit 6#</td>
<td>50,546,176</td>
<td>N/A</td>
<td>99 sec</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

* Standard means most popular Spice simulator
# No resistors and highly repeated memory cell structure

Legend
Technology Leader in IP Characterization and IC/PCB Simulation
# Speed/Accuracy Benchmark

With Other Fast-Spice

<table>
<thead>
<tr>
<th>Circuit Type</th>
<th>Turbo-MSIM CPU Time</th>
<th>Other* CPU Time</th>
<th>Turbo-MSIM Memory Use</th>
<th>Other* Memory Use</th>
<th>Diff.</th>
</tr>
</thead>
<tbody>
<tr>
<td>65nm SRAM</td>
<td>4,217 sec</td>
<td>Fail</td>
<td>1,969 MB</td>
<td>Out of Mem.</td>
<td>-</td>
</tr>
<tr>
<td>65nm SRAM</td>
<td>359 sec</td>
<td>1,099 sec</td>
<td>638 MB</td>
<td>1,614 MB</td>
<td>1.50 %</td>
</tr>
<tr>
<td>90nm SRAM</td>
<td>317 sec</td>
<td>1,414 sec</td>
<td>482 MB</td>
<td>827 MB</td>
<td>1.42 %</td>
</tr>
<tr>
<td>0.13um SRAM</td>
<td>304 sec</td>
<td>824 sec</td>
<td>188 MB</td>
<td>173 MB</td>
<td>1.73 %</td>
</tr>
<tr>
<td>90nm HSTL</td>
<td>131 sec</td>
<td>329 sec</td>
<td>229 MB</td>
<td>802 MB</td>
<td>1.73 %</td>
</tr>
<tr>
<td>90nm SMBUS</td>
<td>15.6 sec</td>
<td>52 sec</td>
<td>42 MB</td>
<td>156 MB</td>
<td>0.05%</td>
</tr>
</tbody>
</table>

* Other means the most popular fast Spice simulator

Technology Leader in IP Characterization and IC/PCB Simulation
Speed/Accuracy Benchmark
With Other Analog Fast-Spice

- Layout-extracted PLL based on TSMC 90nm process
  10,916 MOSFETs, 48,722 Capacitors, 19,191 Resistors

<table>
<thead>
<tr>
<th>Benchmark Data</th>
<th>Turbo-MSIM</th>
<th>Other Analog Fast-Spice</th>
<th>Standard* Accurate Spice</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accuracy Max-Min Cycle</td>
<td>5ps</td>
<td>7ps</td>
<td>0 ps</td>
</tr>
<tr>
<td>CPU Time</td>
<td>10 hrs</td>
<td>36 hrs</td>
<td>172 hrs</td>
</tr>
</tbody>
</table>

- Turbo-MSIM speed-up over other analog Fast-Spice 3.6X
- Turbo-MSIM speed-up over standard Accurate-Spice 17.2X

* Standard means most popular Accurate-Spice simulator

Technology Leader in IP Characterization and IC/PCB Simulation
Turbo-MSIM™ Success
10 Bit ADC Circuit Simulation

- 10 Bit ADC circuit data
  - Number of transistors: 4,150
  - Number of capacitors: 381
  - Total nodes: 2,110

- Simulation period: 26 us

- CPU Time Data
  - Conventional Spice: 86,362 sec
  - Turbo-MSIM: 6,596 sec
Turbo-MSIM™ Success
10 Bit ADC Circuit Simulation

Input voltage

10bits

Technology Leader in IP Characterization and IC/PCB Simulation
Turbo-MSIM™ Success
3 Million MOSFET SRAM Simulation

Single-Port 16Kx32 SRAM
Turbo-MSIM™ Success
Fast and Accurate PLL Simulation

58 minutes and < 3% accuracy

Technology Leader in IP Characterization and IC/PCB Simulation
Turbo-MSIM™ Success
Mixed mode LCD Display Controller

- Mixed mode LCD display controller SoC
  - Multiple voltage sources. (15v, 3.3v)
  - Embedded DRAM (768k bits)
  - Number of transistors: 2,053,916
  - Number of capacitors: 1,572,878
  - Total nodes: 1,835,434
Simulations Goals
Mixed mode LCD Controller

- Functional verification
  - Verify full-chip functionality
  - Verify analog block functionality

- Ground bounce simulation
  - Verify full-chip functionality with ground bounce
  - Simulate inductance and coupling effects
Simulation Waveforms
Mixed mode LCD Controller

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Special Model Support

- Verilog-A model
- CMI (Common Model Interface) model
- TMI (TSMC Model Interface) model
- LCD panel model
- TFT advanced model
Hybrid Modeling Flow
A Complete Device Modeling Solution

Raw Data 1 → 3rd Party Tool
$ Model Extractor → Parameters
$ Turbo-MSIM Simulator → Results

Raw Data 2 → Turbo-MSIM
$ Model Extractor → Parameters
$ Model Extractor → Results

Hybrid Modeling

MVIEWS
Curve-fitted Modeling Waveforms

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Hybrid Modeling Example
Model Parameters by Curve Fitting

Advanced Threshold Voltage Shift Model

Parameters extracted from Turbo-MSIM built-in Model Extractor by curve-fitting

\[ A = 0.0280863 \]
\[ \beta = 0.247142 \]
Turbo-MSIM™ Platforms

- Redhat Enterprise Linux
- Windows XP
- Solaris on X86
Turbo-MSIM™ Benefits

- Enhancing design productivity
  
  Reduce simulation time from days to hours/minutes

- Full-chip hierarchical simulation for timing and power analysis

- Fast post-layout circuit verification with extracted RCs in SPICE/DSPF format

- Scalable accuracy, performance and capacity

- Superior price-performance