MSIM®

High Accuracy Spice Simulator

Legend's Products

- IP Library Characterization Products
  - Charflo-Cell!™ : *Automatic Cell/IO Library Characterization*
  - Charflo-Memory!™: *Automatic Memory Characterization*
- IP Library Model Qualify Assurance Products
  - Model Diagnoser™

    Cell/IO Library Quality Assurance and Defect Repair
- Circuit Simulation Products
  - MSIM®: Accurate-Spice Simulator
  - Turbo-MSIM™: Fast-Spice Simulator

MSIM®

High Accuracy Spice Simulator

- Extreme accuracy and excellent convergence
- High speed and large capacity
- Extensive model support
- Multi-threaded applications on multi-core computer
- Automatic matrix solver selector for throughputs
- Built-in AWE RC Reduction
- Best price-performance

MSIM® Certifications

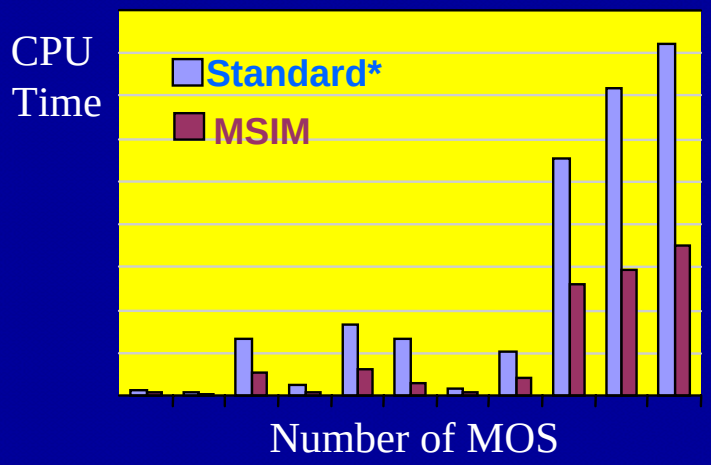
- MSIM certified by TSMC's Spice Tool Qualification Program

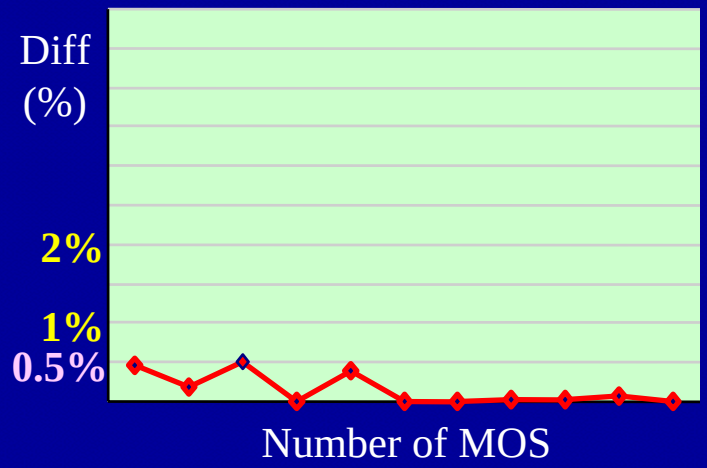
  http://www.legenddesign.com/BW/021009.shtml
- MSIM certified by TSMC's TMI (TSMC Model Interface) Qualification Program

MSIM® Advantages

High Accuracy and Fast Speed

- More than twice the speed of the Standard*
- Same accuracy (less than 1%) as the Standard*





** Standard means the most popular Spice simulator*

MSIM® Accuracy

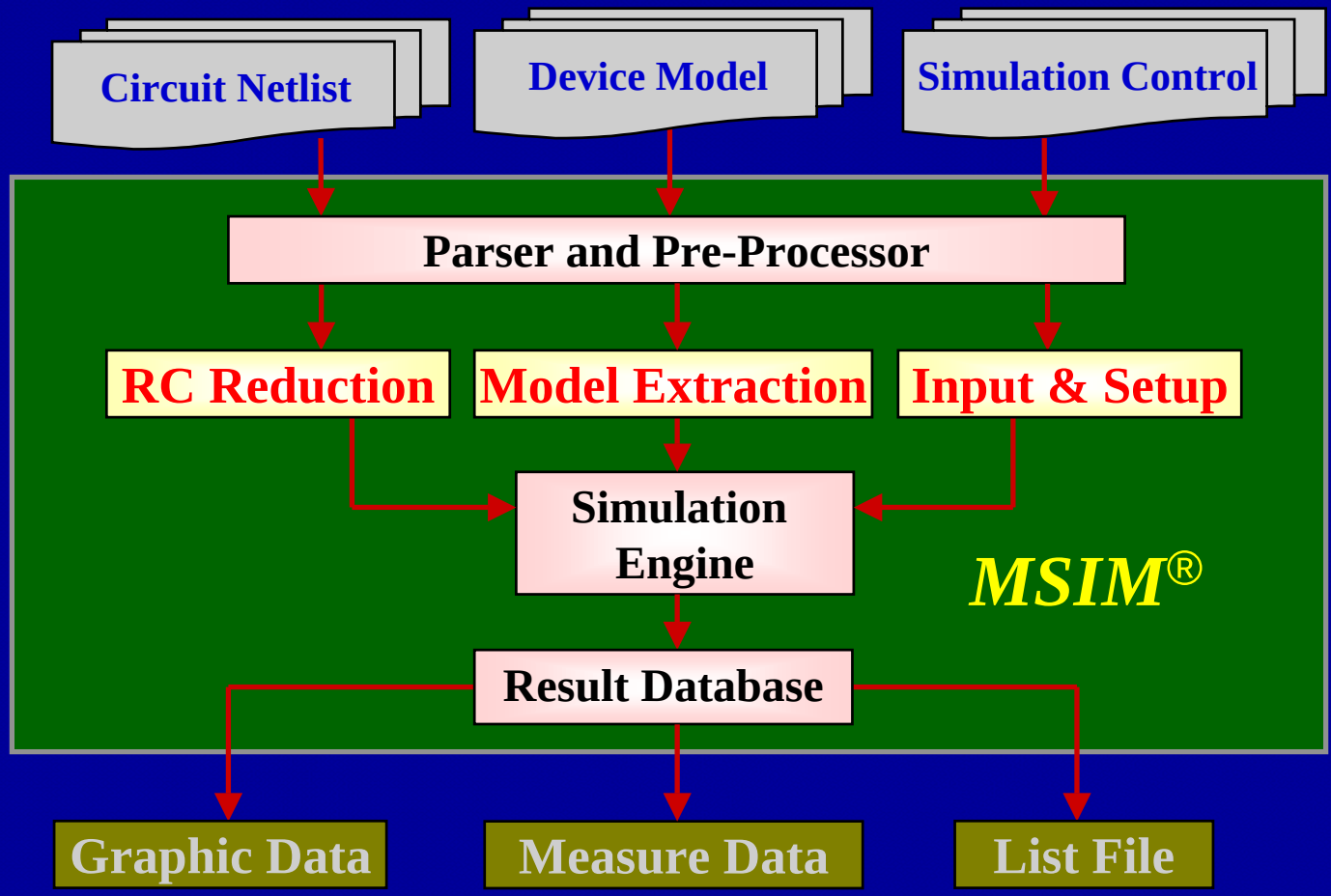
Benchmark on BSIM4 Model

MSIM® Model Support

Extensive Modeling Support

- MSIM delivers silicon-accurate models with proven implementations of
  - * BSIM3
  - * BSIM4
  - * BSIM4 SOI
  - * HiSIM1 and HiSIM2
  - * Philips MM9 & MM11
  - * RPI TFT
- Direct access of updated SPICE models from
  - * TSMC
  - * UMC
  - * IBM
  - * Chartered
  - * SMIC
  - * Tower

MSIM® Simulation Flow



MSIM® Multi-Thread

Multi-Core and Parallelism Support

- Enable multi-threaded application on a multi-core configuration
- Utilize the multi-thread functions for decomposing and solving matrices, and calculating device model
- Prove its outstanding efficiency on the circuits with a large number of extracted post-layout parasitics

MSIM® Multi-Thread
Benchmark Data

- Benchmark on 2 Quad-Core CPU system

Threads	Run Time	Speed-up
1	319 seconds	1.00 X
2	171 seconds	1.87 X
3	121 seconds	2.64 X
4	97 seconds	3.29 X
5	80 seconds	3.99 X
6	68 seconds	4.69 X
7	64 seconds	4.98 X
8	57 seconds	5.60 X

MSIM® Maxtrix Solving

Automatic Matrix Solver Selector

- Conventionally, sparse matrix solving technique is used to take advantage of the sparse in circuit matrix for the efficiency
- For nanometer technology, sparse matrix solving technique could be not efficient for the layout extracted circuits with large RC networks
- A Matrix Solver Selector has been developed and implemented in MSIM, for simulation throughputs.

MSIM® Maxtrix Solving
Benchmark Data

- Benchmark circuit data

  MOSFET: 6,926 Resistor: 65,662 Capacitor: 11,178

- Simulation statistics using Sparse Matrix

  Max allocated memory = 251 mb
  Total CPU time = 36,092.59 seconds

- Simulation Data using Matrix Solver Selector

  Max allocated memory = 97 mb
  Total CPU time = 2,589,.69 seconds

- **14X** Speed up, and **2.6X** less usage of memory

MSIM® RC Reduction

Layout-Extracted Circuit Simulation

- Benchmark on D-Type Flip Flop circuit

  MOSFET: 18 Resistor & Capacitor: 1,000+

	Standard*	MSIM™	Comparison
CPU Time	300 sec	10 sec	30 X

The inaccuracy is less than 1%.

- Benchmark on SRAM 'RR256x16'

  MOSFET: 39,464 Resistor : 200,526 Capacitor: 316,934

	Standard*	MSIM™	Comparison
Accuracy	3.41 ns	3.39 ns	0.59 %
CPU Time	3,867 sec	317 sec	12.2 X

** Standard means the most popular Spice simulator*

Subcircuit Spice Model

Memory Usage/CPU Time Benchmark

- Subcircuit Spice models are popular in 65nm and below due to its flexibility. Each MOSFET has its own model.
- Subcircuit Spice models cause huge memory usage and degrade the performance.

Circuit Type	MOSFET Count	MSIM		Other Popular Spice	
		CPU Time	Memory Usage	CPU Time	Memory Usage
Data_in.sp	~10K	551 sec	293 MB	2,294 sec	6.7 GB
Access.sp	~40K	3,007 sec	1.4 GB	Can not run	Can not run

MSIM®
Applications in IC and IP

- Analog circuit design verification
  - Frequency response and transient analysis for verifying analog circuits like PLL, A/D and D/A converters, amplifiers and IO devices etc.
- Mixed-signal circuit design verification
  - Support Verilog-A behavioral modeling, vector input stimulus and vector output verification
- RF design analysis
- Cell library and memory characterization

MSIM®

Ring Oscillator Benchmark

101 Stage NAND2 Ring Oscillator Simulation Results / Comparison

Measurement	Standard* Accurate Mode*	MSIM Accurate Mode	
	Time	Time	Difference
Time_rr	**4.2711e-09**	4.2527e-09	**0.43%**
Time_ff	**4.2711e-09**	4.2520e-09	**0.45%**
Average Current	**-1.4119e-04**	-1.4096e-04	**0.16%**
Power Parameter	**-7.2364e-13**	-7.1936e-13	**0.59%**
Time_rf	**2.1422e-09**	2.1325e-09	**0.45%**
Duty Parameter	**5.0156e+01**	5.0144e+01	**0.02%**

MSIM (Accurate Mode)

98.23 sec

Standard* (Accurate Mode)

328.68 sec

MSIM Speed-Up

3.35 X

** Standard means the most popular Spice simulator*

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Memory Benchmark

Full-Circuit 'Access Time' Simulation Results / Comparison

This SRAM circuit has 21,087 MOS, 73,374 Rs and 44,639 Cs

Access Time	Standard* Accurate Mode	MSIM Accurate Mode		HSPICE Default Mode		MSIM Default Mode	
	Time	Time	Difference	Time	Difference	Time	Difference
O[0] rise	**1.4776ns**	1.4769ns	**-0.0474%**	1.4541ns	**-1.5904%**	1.4849ns	**0.4940%**
O[24] rise	**1.4832ns**	1.4823ns	**-0.0607%**	1.4560ns	**-1.8339%**	1.4880ns	**0.3236%**
O[0] fall	**1.5448ns**	1.5441ns	**-0.0453%**	1.5219ns	**-1.4824%**	1.5552ns	**0.6732%**
O[24] fall	**1.5446ns**	1.5445ns	**-0.0065%**	1.5221ns	**-1.4567%**	1.5633ns	**1.2107%**

Standard* Accurate Mode is taken as 'GOLD' for comparison

** Standard means the most popular Spice simulator*

MSIM®

Phase Locked Loop Benchmark

250MHz PLL Circuit Simulation Results /Comparison

Measurement	Standard* Accurate Mode	MSIM Accurate Mode	
	Time	Time	Difference
Lock Time	**2.0040e-06**	2.0038e-06	**0.01%**
Last Single Clock Cycle Time	**3.9999E-09**	3.9971e-09	**0.07%**
Average Clock Cycle Time	**4.0000E-09**	3.9998e-09	**0.00%**
Power	**3.2518e-04**	3.2295e-04	**0.69%**

MSIM (Accurate Mode)

2794 seconds

Standard* (Accurate Mode)

6096 seconds

MSIM Speed-Up

2.16 X

** Standard means the most popular Spice simulator*

MSIM®

Complex IO Circuit Benchmark

Complex IO Circuit Simulation Results / Comparison

Measurement	Standard* Accurate Mode	MSIM Accurate Mode	
	Time	Time	Difference
Rise delay	**1.095e-09**	**1.095e-09**	**0.00%**
Fall delay	**1.007E-09**	**1.0071e-09**	**0.01%**
Rise slew	**2.489E-09**	**2.496e-09**	**0.26%**
Fall slew	**2.493e-09**	**2.498e-04**	**0.22%**

MSIM (default Mode)

33.94 seconds

Standard* (default Mode)

1,550.14 seconds

MSIM Speed-Up

45.5 X

** Standard means the most popular Spice simulator*

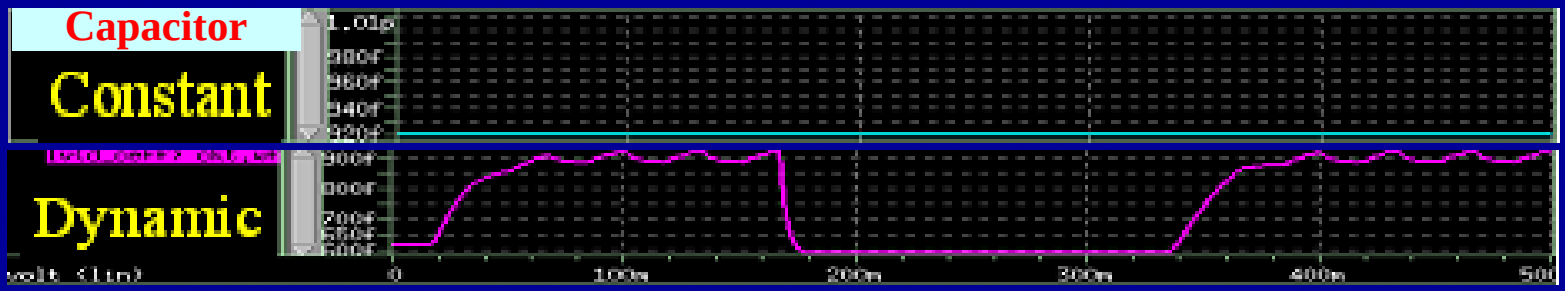
Special Model Interface

- Verilog-A model
- CMI (Common Model Interface) model
- TMI (TSMC Model Interface) model
- LCD Panel model
- S-Parameter model

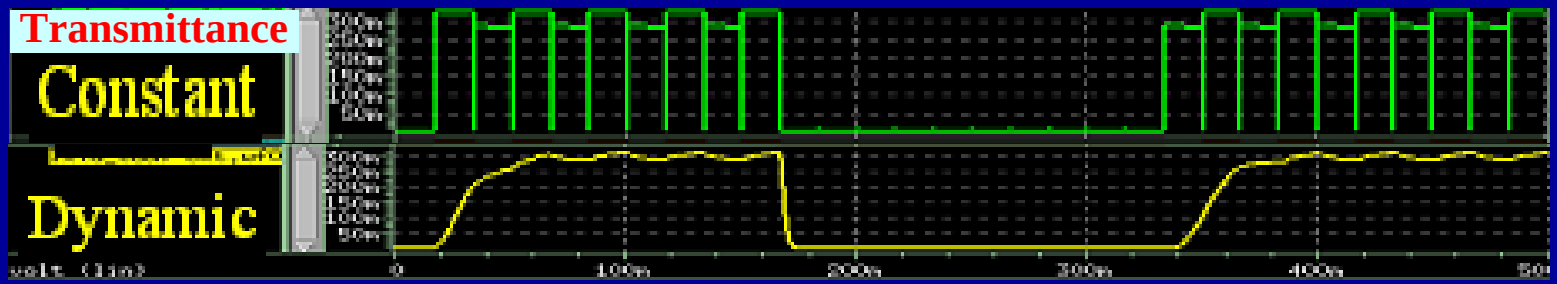
LCD Panel Circuit Simulation

Dynamic C_{LC} and Advanced TFT Model

- Dynamic effect of Effective Capacitor can be simulated by MSIM

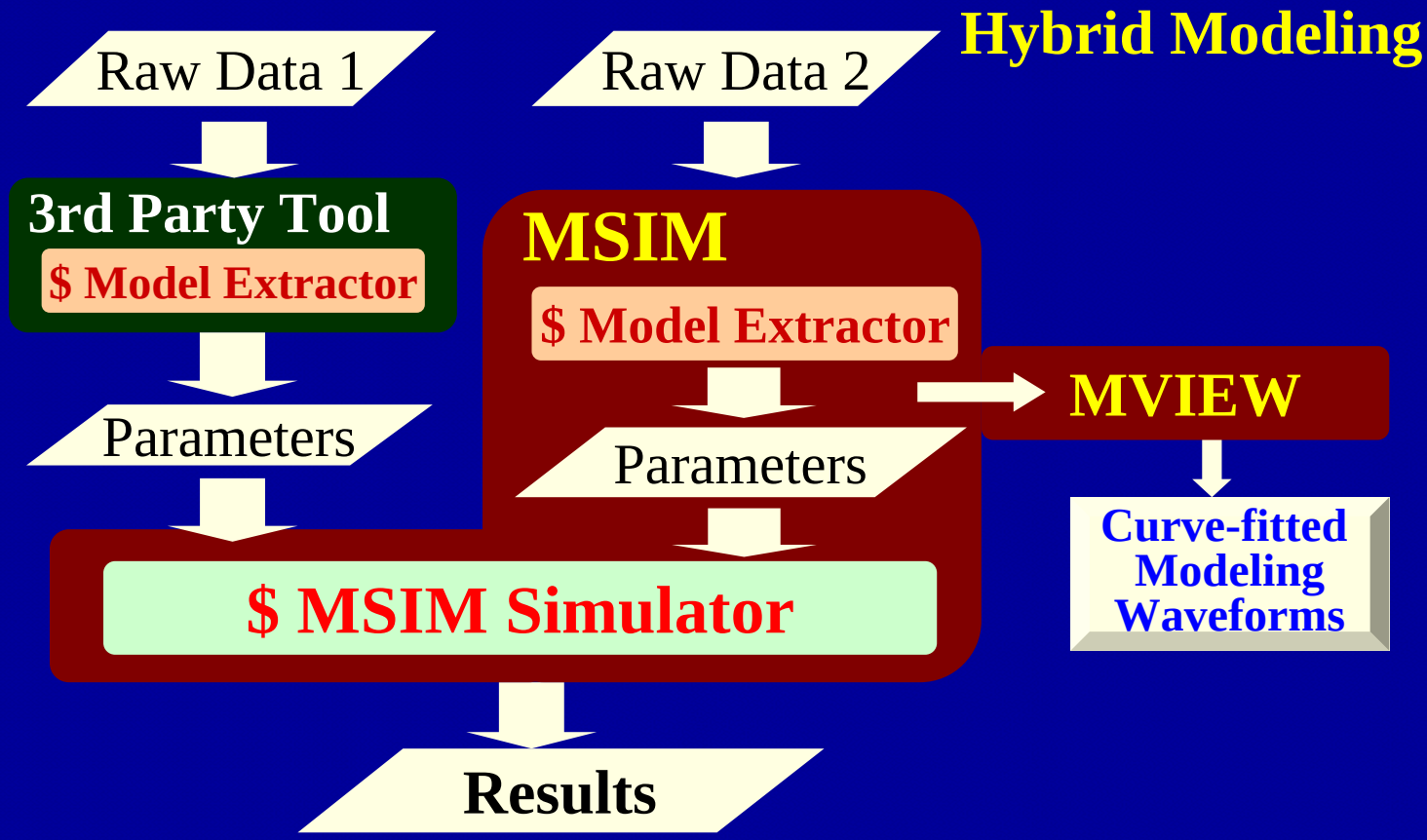


- Dynamic effect of Transmittance can be simulated by MSIM



Hybrid Modeling Flow

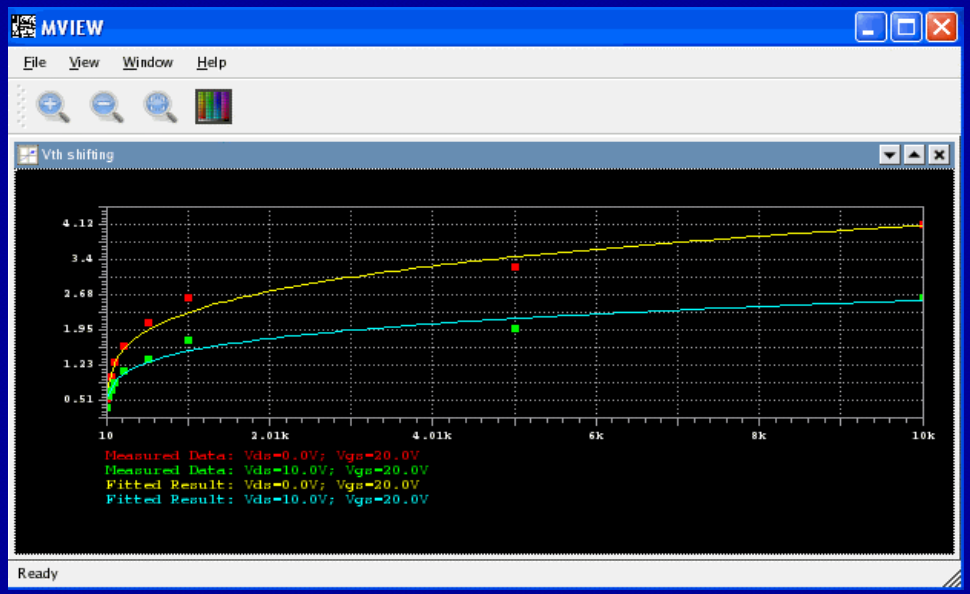
A Complete Device Modeling Solution



Hybrid Modeling Example

Model Parameters by Curve Fitting

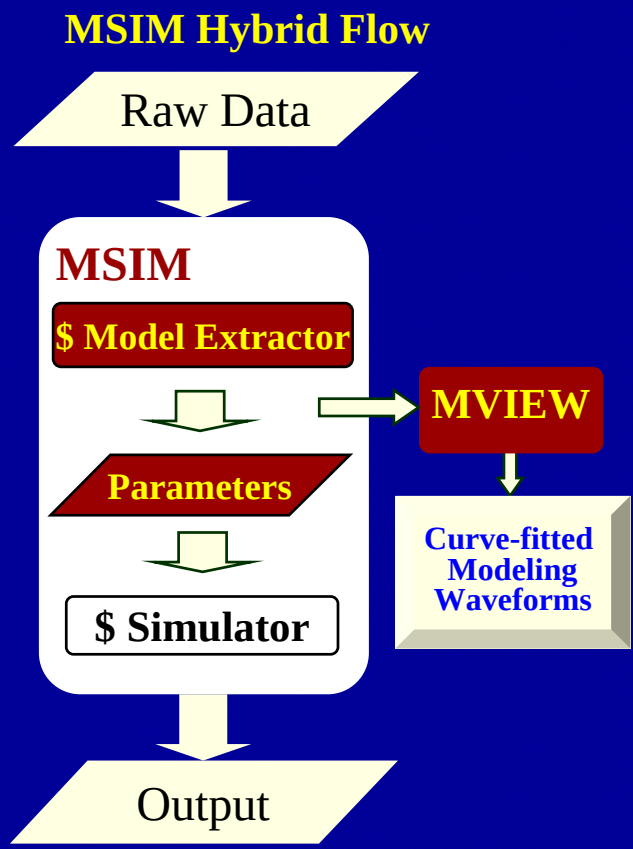
Advanced Threshold Voltage Shift Model



Parameters extracted from MSIM built-in Model Extractor by curve-fitting

A = 0.0280863

β = 0.247142



MSIM® for Optimization

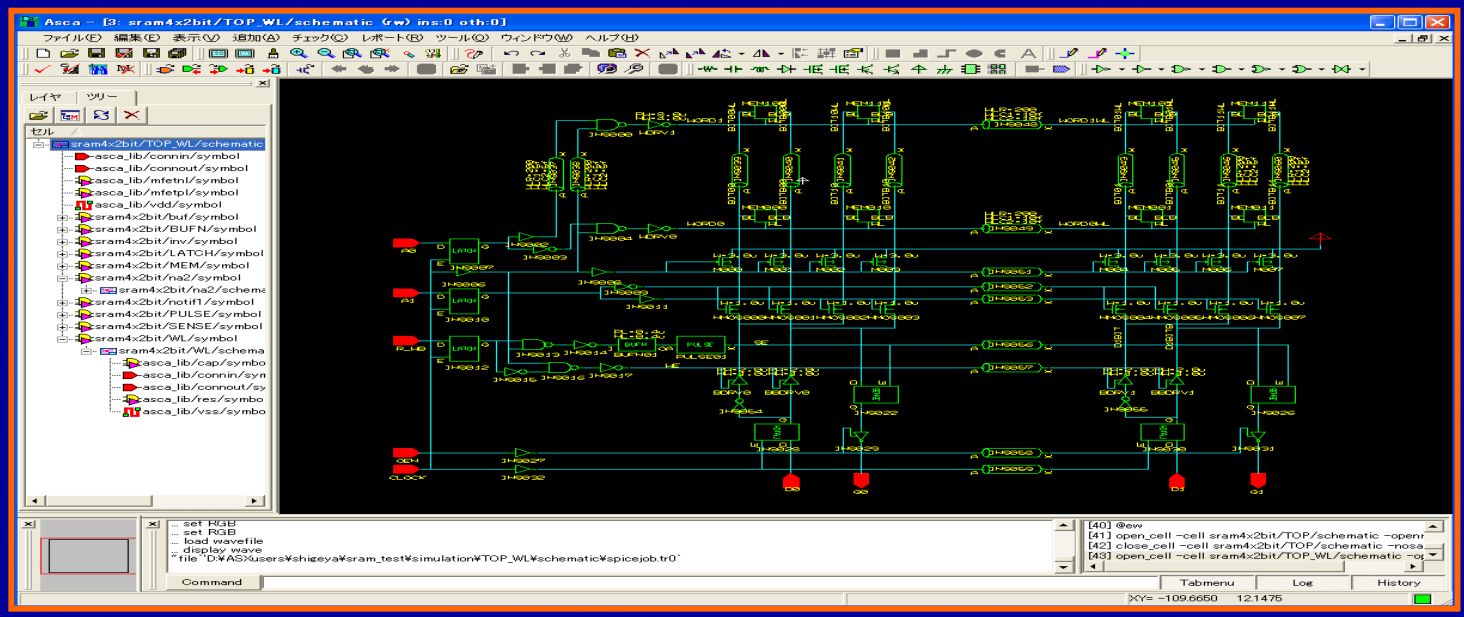
- A procedure for automatic searching instance or model parameters to meet design goal
- Optimization function can be applied for .DC, .AC and .TRAN analysis
- Optimization method can be native, bi-section or pass-fail
- Flexible measurements in optimization process
- HSPICE-compatible format

MSIM® Portability

- Platforms
  - Redhat Enterprise Linux
  - Windows XP
  - Solaris on X86
- Environments
  - JEDAT - ASCA
  - SpringSoft – Laker-ADP
  - Cadence - ADE
  - Mentor – DAIC

MSIM® with ASCA

Jedat's AnalogCreator Platform

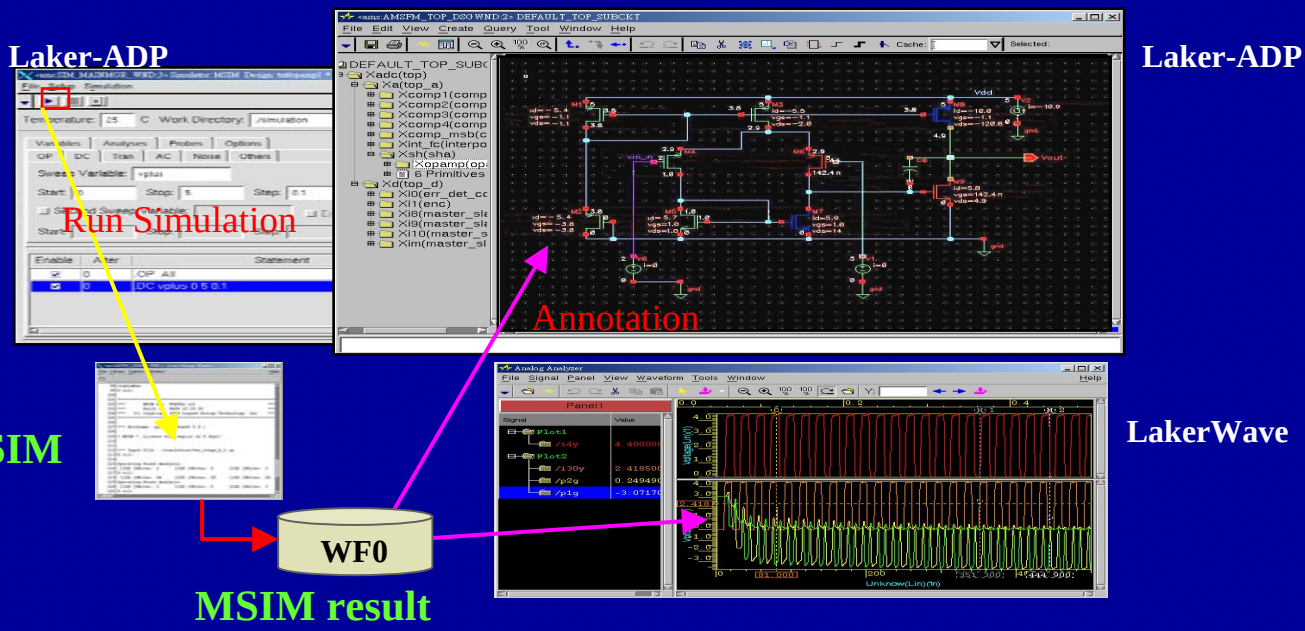


MSIM seamlessly integrated into Jedat's ASCA with

- High throughputs
- Optimized simulation and debugging setup

MSIM® with Laker-ADP

Silicon Canvas' Analog Design Platform



MSIM seamlessly integrated into Laker-ADP with

- Enhanced productivity
- Speedup of simulation and debugging process

MSIM® with Virtuoso

- MSIM-Virtuoso Ocean Interface
  - The input to MSIM is the circuit netlist from Virtuoso database, and simulation controls from users
  - The output from MSIM is the measurement, the list and waveform files including PSF format
- MSIM-Virtuoso ADE Interface
  - MSIM is fully compatible with HSPICE options including option ARTIST and PSF.
  - MSIM can be invoked in the same way as HSPICE does from ADE, after some simple environment setup.

MSIM® for Characterization

Cell / IO / Memory Characterization

- Standard / IO Cell Library Characterization
  - Legend Design Technology's CharFlo-Cell!
  - Magma's SiliconSmart
  - Cadence' SignalStorm
  - Library Technology's LibChar
  - In-house characterization tools
- Memory Compiler Characterization
  - Legend Design Technology's CharFlo-Memory!
  - In-house characterization tools

MSIM® with CharFlo-Cell!

Cell/ IO Library Characterization

- The integration of CharFlo-Cell! products and MSIM has been successfully completed
- MSIM has been the primary circuit simulator used in QA flow of CharFlo-Cell! products
- The speed and accuracy of MSIM complements the strengths of the CharFlo-Cell! technology
- MSIM circuit simulator runs multiple times faster than traditional SPICE simulators without loss of accuracy

MSIM® with Charflo-Memory!

Memory IP Characterization

- Register File ‘RF2R1W16X128S’

Access Time (5 input slopes and 5 output loadings)

25 Simulation Jobs

	CPU Time	Gains
1 MSIM®	7 Hours 17 Minutes	**1.0 X**
4 MSIM®	2 Hours 8 Minutes	**3.4 X**
8 MSIM®	1 Hour 13 Minutes	**6.0 X**
25 MSIM®	18 Minutes	**23.9X**

MSIM® Compatibility

- HSPICE format

  Command

  % msim –i ckt.sp –o ckt.lis -hsp

  The flag -*hsp* turns on HSPICE format and output naming convention

- Spectre Format

  Command

  % msim –i ckt.sp –o ckt.lis -spectre

  The flag -*spectre* turns on Spectre format.

- Eldo Format

  Command

  % msim –i ckt.sp –o ckt.lis -eld

  The flag -*eld* turns on Eldo format and output naming convention

Conclusion

- MSIM is an excellent circuit simulator by
  - Innovative algorithms and schemes
  - Optimized codes and structures
  - Silicon-accurate BSIM3 and BSIM4 modeling
- MSIM certified by TSMC Spice Tool Qualification
- MSIM supports multi-threaded applications on a multi-core computer, with flexible licensing
- MSIM automates the selecting matrix solver for layout-extracted circuits, with much higher speed-up
- MSIM provides best price-performance