

LAVIS

Ver.10.2

Multi-use Layout Analyzer

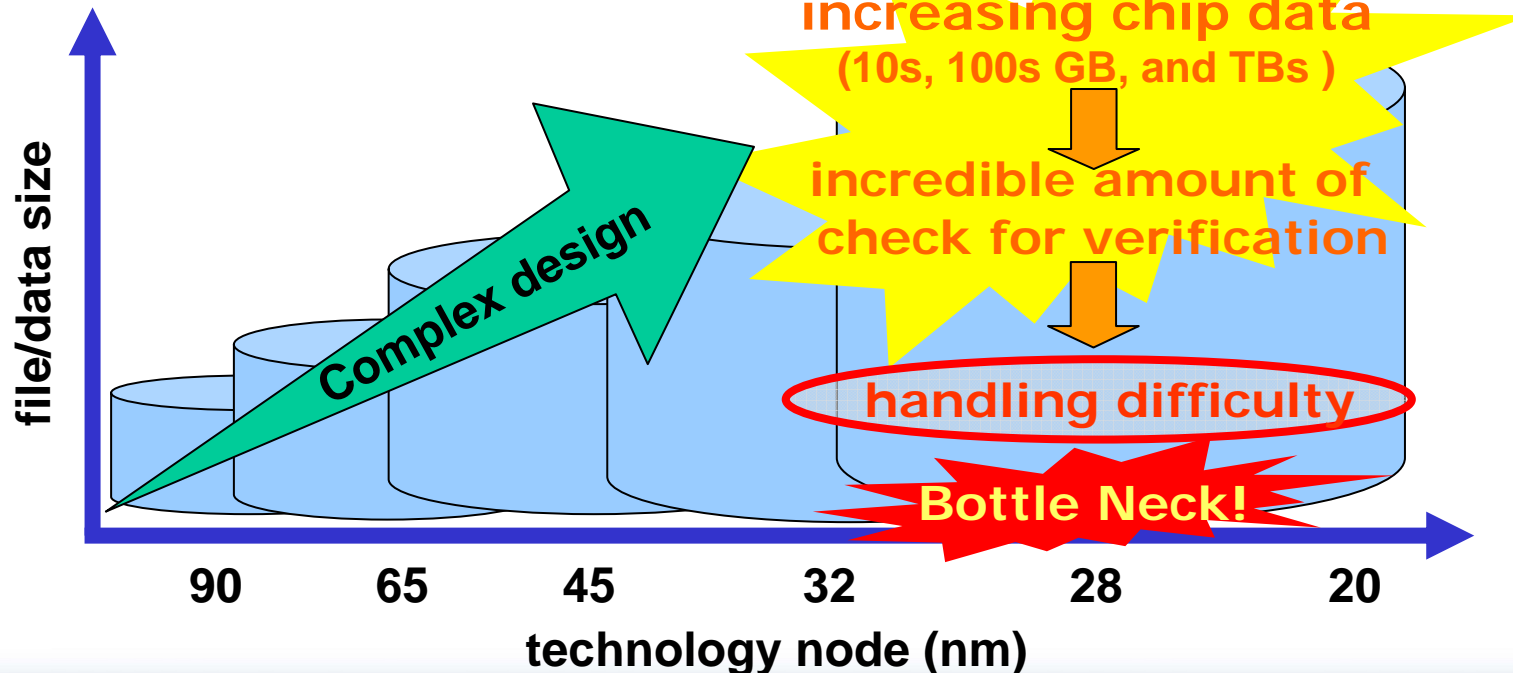
TOOL CORPORATION

[http:// www.tool.co.jp](http://www.tool.co.jp)

■ New issues

- Power, Signal Integrity, DFM, DFT, so on
- Many verifications and checks are required
- All those data is getting too large to handle

=> **Data explosion issue is simple,
But Extremely Big**



How to fix needs in each process ?

- How to handle incredible amount of data?
- How to check sea of results of verification?
- How to satisfy needs in each process?
(usually an individual tool in each process)
 - ✓ For Physical Design
 - ✓ For Failure Analysis
 - ✓ For MDP (Mask Data preparation)
- Not only performance but also useful functions
to improve the quality & the productivity

LAVIS Layout Analyzer Can Provide Solutions

LAVIS

Versatile Layout Platform

High-performance Layout Visualization Analysis Platform

- LAVIS provides:
 - Common operating **super high-speed** and **huge data** display
 - Powerful **analyzing capabilities** and abundant **Interfaces**
 - A simple, **cost-effective**, **easy to use** solution

Layout Design



Layout Verification



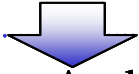
Mask Data Preparation



Mask Data Generation



Wafer Manufacturing



Failure Analysis

Automatic P&R

GDS/LEFDEF

DRC

DRC I/F

LVS

LVS I/F

OPC

Lith Sim I/F

Lithography Simulation

Lith Sim I/F

EB Data Generation

EBs I/F

CD Measurement Equipment

Equip. I/F

Layout data Navigation/Trace

GDS/LEFDEF

L

A

V

I

S

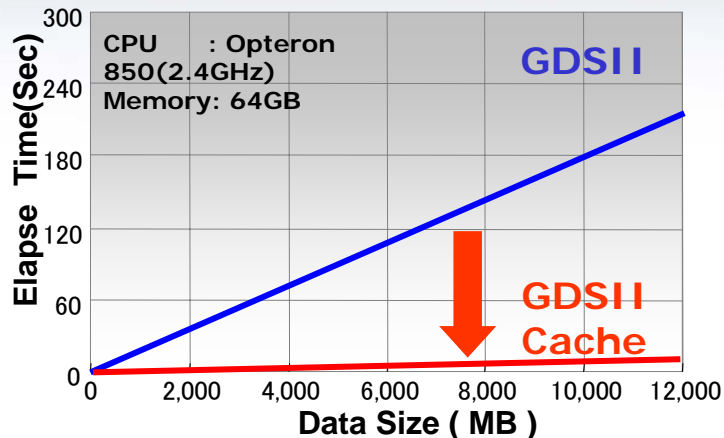
Improving
Layout
Quality

Improving
Productivity of
Model Validation &
Pattern check

Shortening
Cause Analysis

High-performance Layout Analyzer

- Super high-speed and enormous layout data display
 - Stress free opening and drawing any large layout data
 - Improve layout visualization checking productivity tremendously
- Powerful layout analysis capability to improve the quality of Layout Design and the productivity of MDP and Silicon FA
 - Multi-format and many sophisticated check/debug functions and utilities for Layout Verification, Si Failure Analysis, and Mask Data Preparation
- Abundant interfaces for physical verification, litho-simulation, CD-measurement, and Failure Analysis
 - Various interfaces with popular DRC/LVC, DFM/OPC tools and semiconductor equipment like Inspection and Failure Analysis
- Enable to reduce Verification/Analysis Cost & TAT by using affordable and convenient Layout Analyzer
 - Fill the gaps between the automatic and the nonautomatic checking processes in the one-pass sign-off design & verification flow
 - Common layout platform across the entire physical design flow



Opening Time

GDSII 1GB / 20sec.
x1/20(use cache)

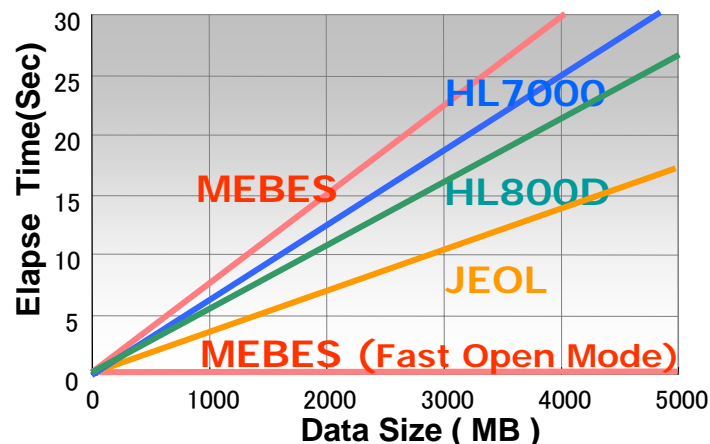
EB 1GB / 10sec.

Drawing Time

2-3sec.

Track Record

GDSII 500GB / 4 hours
(memory size: 100GB)



Other viewer can handle such huge data with High-performance?

■ Visual debug & check capabilities for all needs

Functions:

- Node-Trace
- Overlay & Image Paste
- Boolean Operation
- LEF/DEF, Find net&cell
- GDS/OASIS Simple Edit

- Synchronized Views
- Data Cutting out
- Set & Save Markers
- Measurement & Search
- Compressed data
- direct read
- Color Map Display
- X-section & 3D Display
- Remote Viewing

Interfaces:

- Calibre DRC Interface
- DRC & LVS I/Fs
- Litho. Sim. I/Fs
- CD Measurement I/Fs
- Other Equipment I/Fs

Utilities:

- Virtuoso env. conv.
- Boolean operation
- GDSII/ASCII conv.
- Cache file make
- Density calculation

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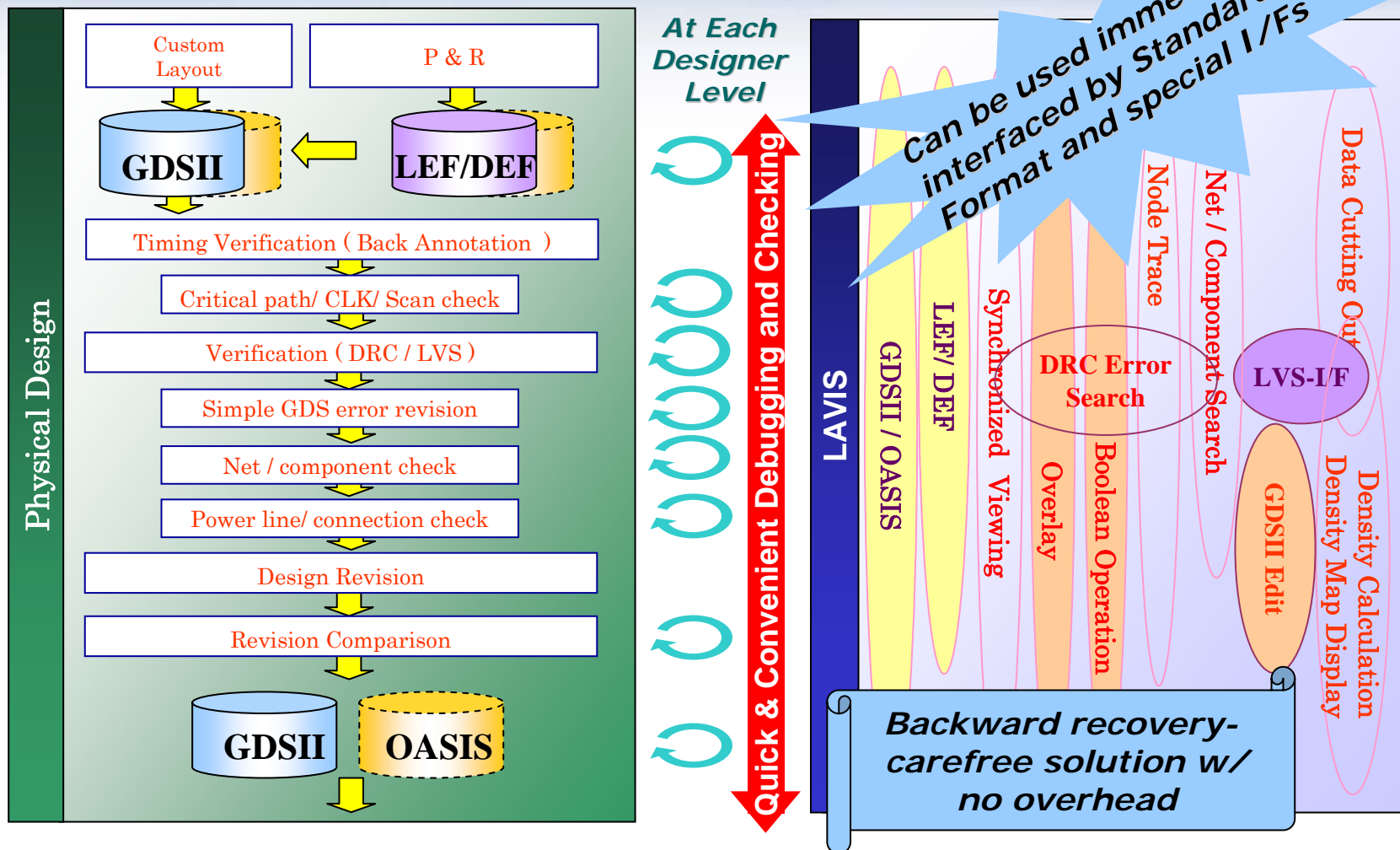
Versatile Layout Platform

Physical Design Flow

LAVIS

Versatile Layout Platform

*Quick & Convenient Visualization
Analysis in all parts of layout design*



*Improving the Efficiency of your Layout Design Work
and the Layout Quality*

TOOL CONFIDENTIAL

In Physical Design Process

(even for Analog/Mixed-signal Design)

LAVIS enables to improve your Layout Quality and Efficiency of Your Work by yourself using with a sense that you can check **CONVENIENTLY**

- *what you want*
- *when you want*
- *all you want*

in all parts of layout design
with No Iteration and No Overhead

■ Quick layout rule check in specified areas and on traced nodes - relatively small area

As "simple layout checker"

- Width/Space/Area/Density/Sliver Check
- Length/Perimeter/Redundant Via/Resistance Calc.
- Cell/Component/Block/IP, and Pins (Ports)
- Connectivity of Power, CLK, Signals -> electrical short
- ECO check/compare – difference/no-difference
- X-talk, Parallel lines, Symmetry properties, etc.

■ Check and debug of DRC/LVS results at a chip level and large nodes as Power line

As "layout debugger"

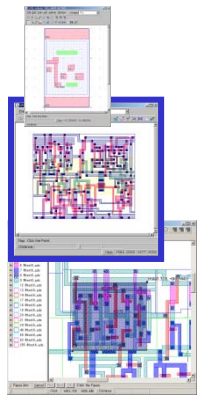
- Quick look at entire error distribution at chip level
- Check and what-if analysis of timing issues like critical path/CLK
- Check large node as PWR line for EM restriction

Incremental Checking to Improve the Quality

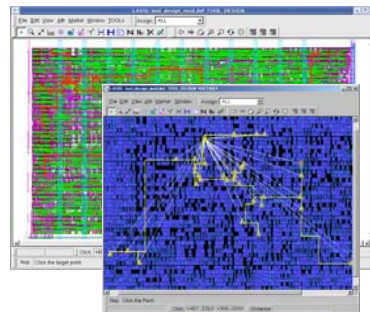
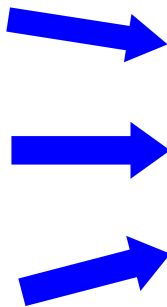
Enable to improve the Design Quality at individual designer level by Checking Incrementally at any design stage as Cell, Block/IP and a chip level whenever you want to avoid big issues at the last minute filling the gaps between automatic and nonautomatic checking flow

The total verification TAT is decided on by how to improve the quality at lower design levels

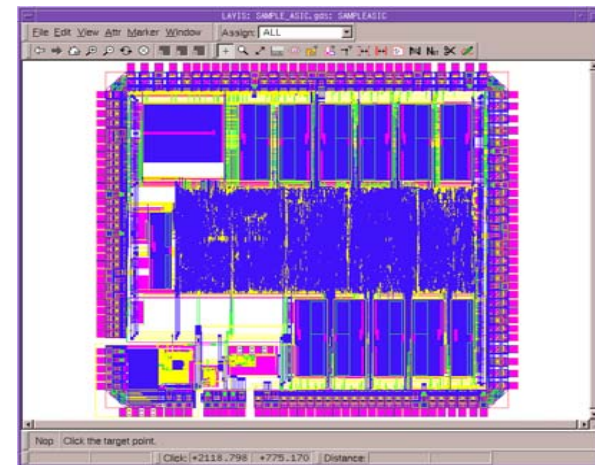
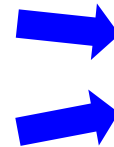
Final sign-off verification as DRC/LVS
No big fatal impact!



Cell level



Block/IP level



Chip level

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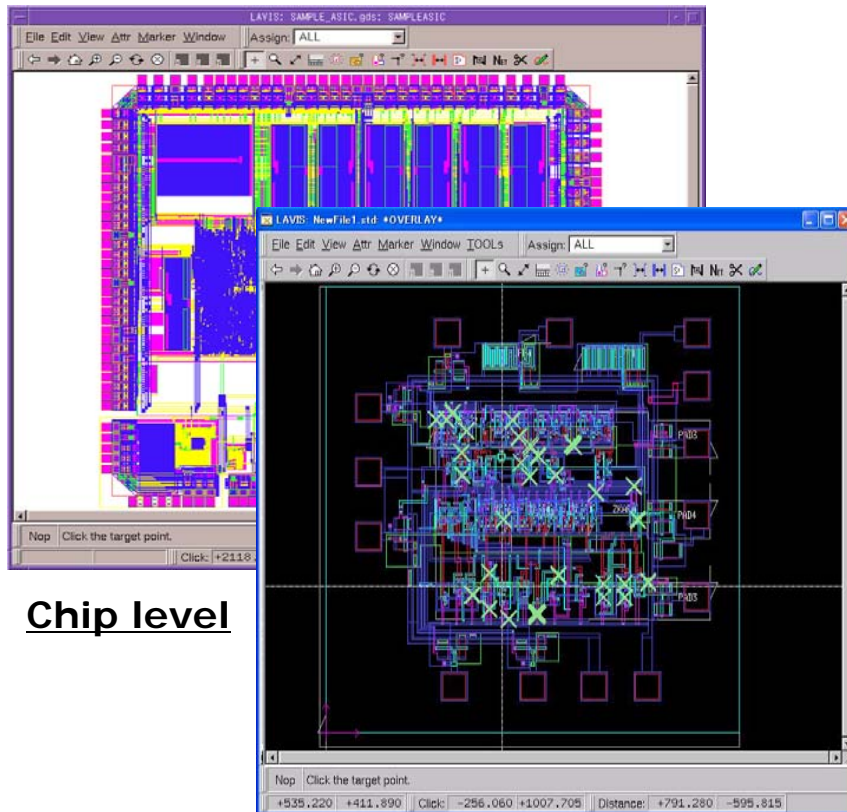
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Layout Check at chip level

- Power/CLK/SCAN, DRC, TA -

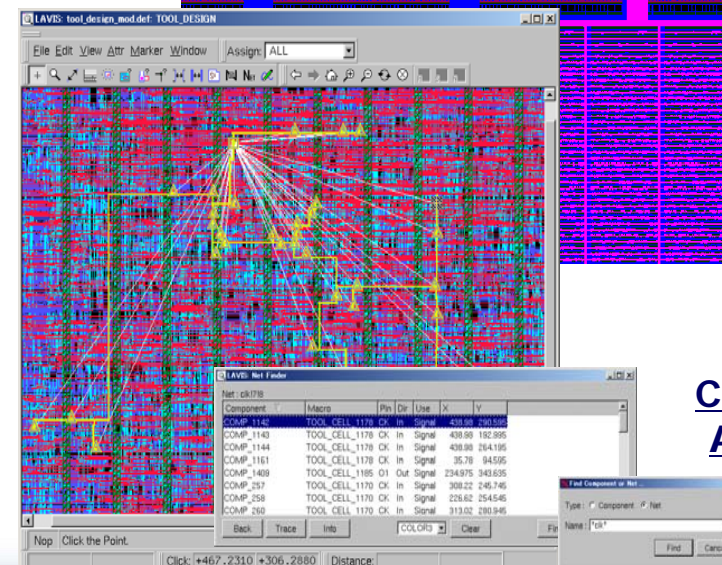
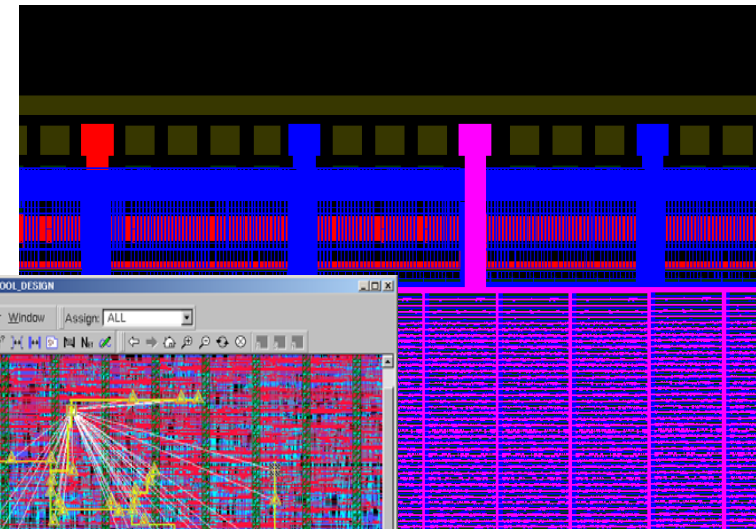
Enable to check a layout at chip level with high performance for tracing huge nodes like Power, Clock, Scan clk, Busses, and error distribution, critical paths

power lines check



Chip level

Quick look at error distribution

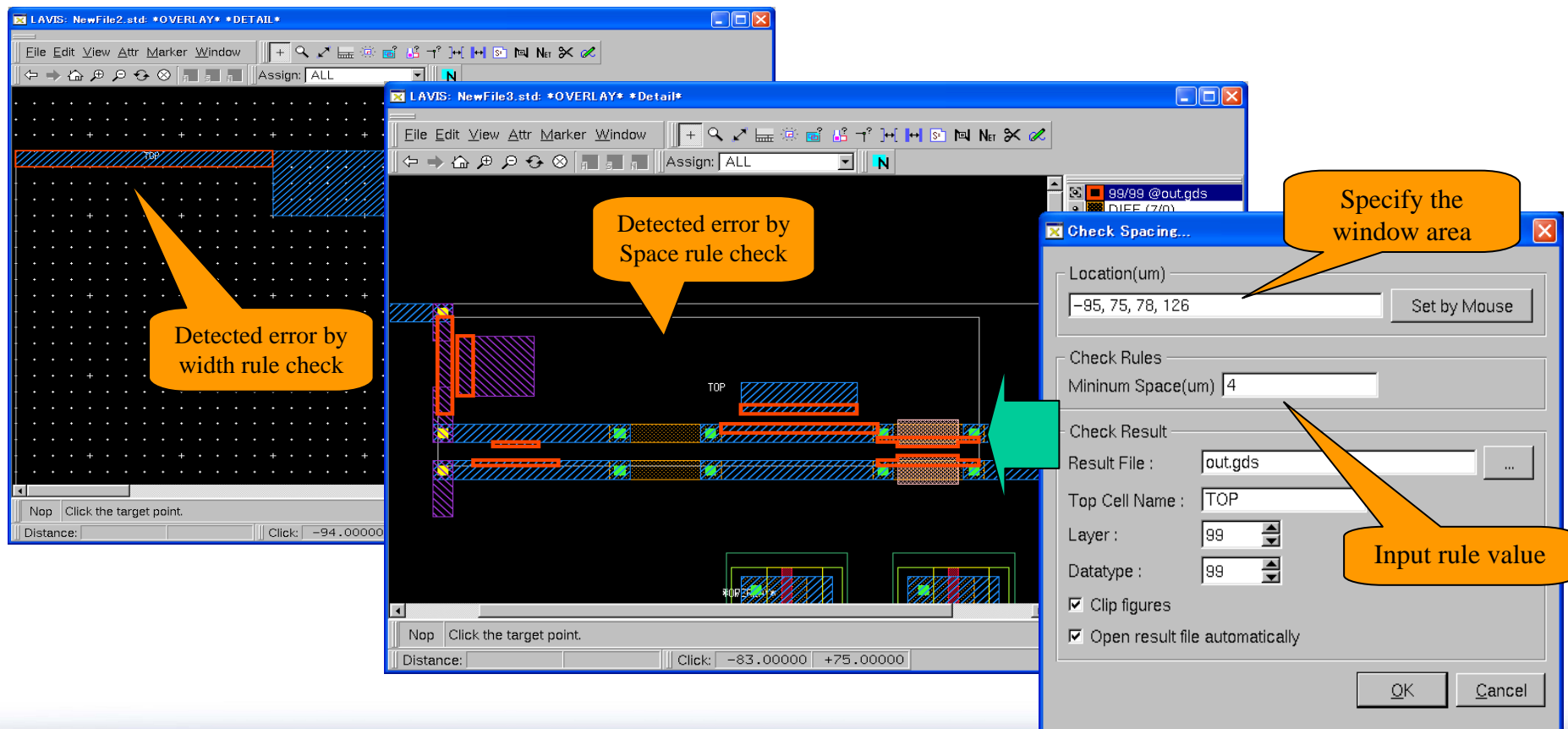


Critical path
Analysis on
Layout

Simple Rule Checking

New Minimum Width/Space Check

> Minimum width/space check within the specified window area is available



New Sliver Check

> Sliver check within the specified window area is available

Input Measurement dir.
Rule value
Step size

Figure count by size (step size)

Command Window Output:

```

INFO : Check Sliver Figures
INFO :
INFO : Region (um) : (-52,115, 114,872, 37,205, 183,602)
INFO : Measure : Shortest Edge
INFO : Max size (um) : 4
INFO : Step size (um) : 1
INFO :
INFO : Size (um) : Figures (Percentage)
INFO :
INFO : 0,000 - 1,000 : 0 (0,00)
INFO : 1,000 - 2,000 : 1 (10,00)
INFO : 2,000 - 3,000 : 1 (10,00)
INFO : 3,000 - 4,000 : 0 (0,00)
INFO :
INFO : Total slivers : 2 (20,00)
INFO : Total figures : 10 (100,00)
INFO :
INFO : NORMAL END
INFO : Elapsed-Time : 00:00 (0,029 sec.)
INFO : CPU-Time : 00:00 (0,01 sec.)
  
```

New Area Calculation within the specified window

> Enable to calculate Area/Coverage within the specified window area

Specify the window area

Area with in the window

Coverage retio

Calculate Area...

Location(um)

330.237, 81.799, 444.52, 199.917

Set by Mouse

OK Cancel

LAVIS: Command

Target: test6_src.mebes [tes]

```
INFO : Calc Area
INFO :
INFO : Region (um) : (330.237, 81.799, 444.52, 199.917)
INFO : Area (um^2) : 7092
INFO : Coverage (%) : 52.5377 %
INFO :
INFO : NORMAL END
INFO :
INFO : Elapsed-Time : 00:00 (0.077 sec.)
INFO : CPU-Time : 00:00 (0.08 sec.)
```

Command:

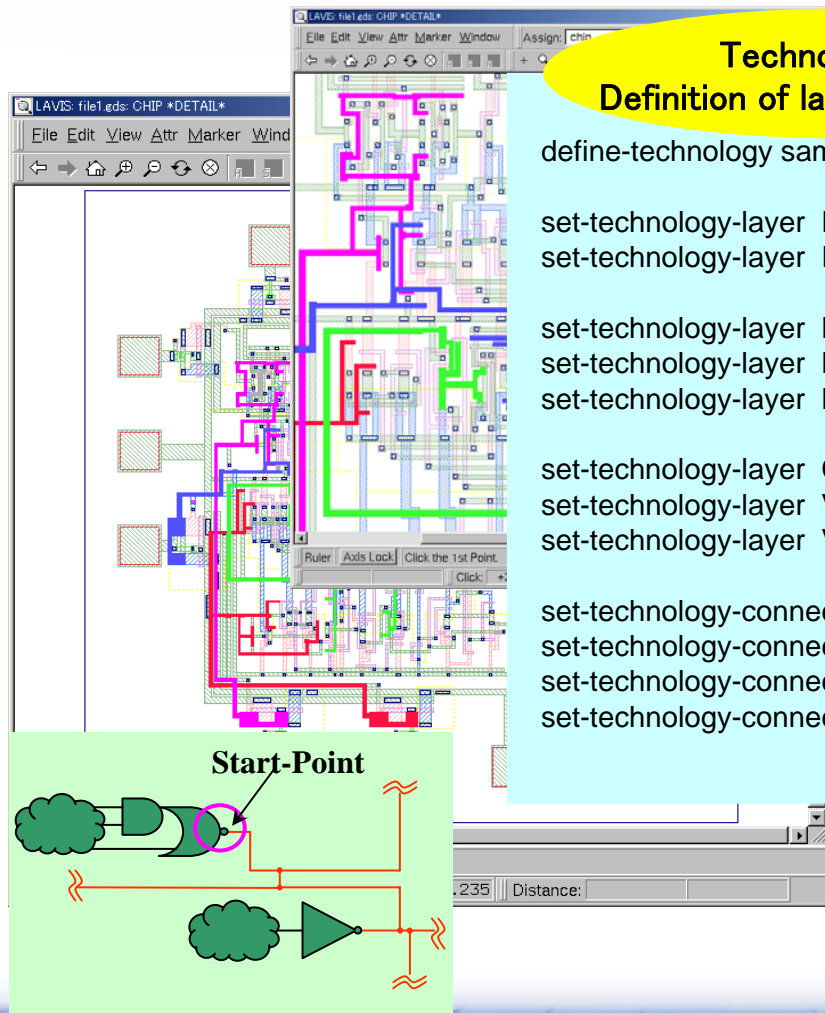
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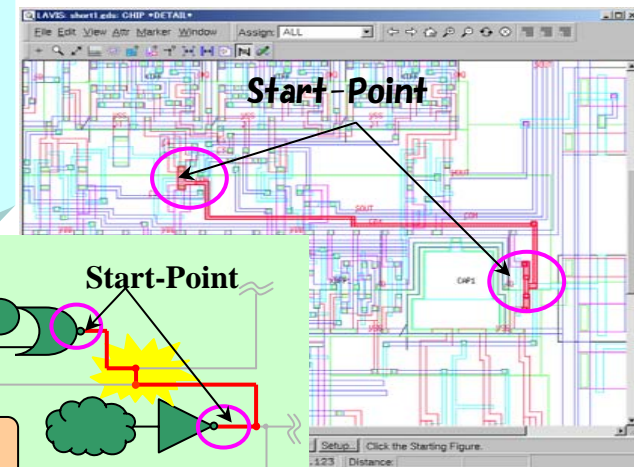
Node Checking on GDS

Tracing Node and Short

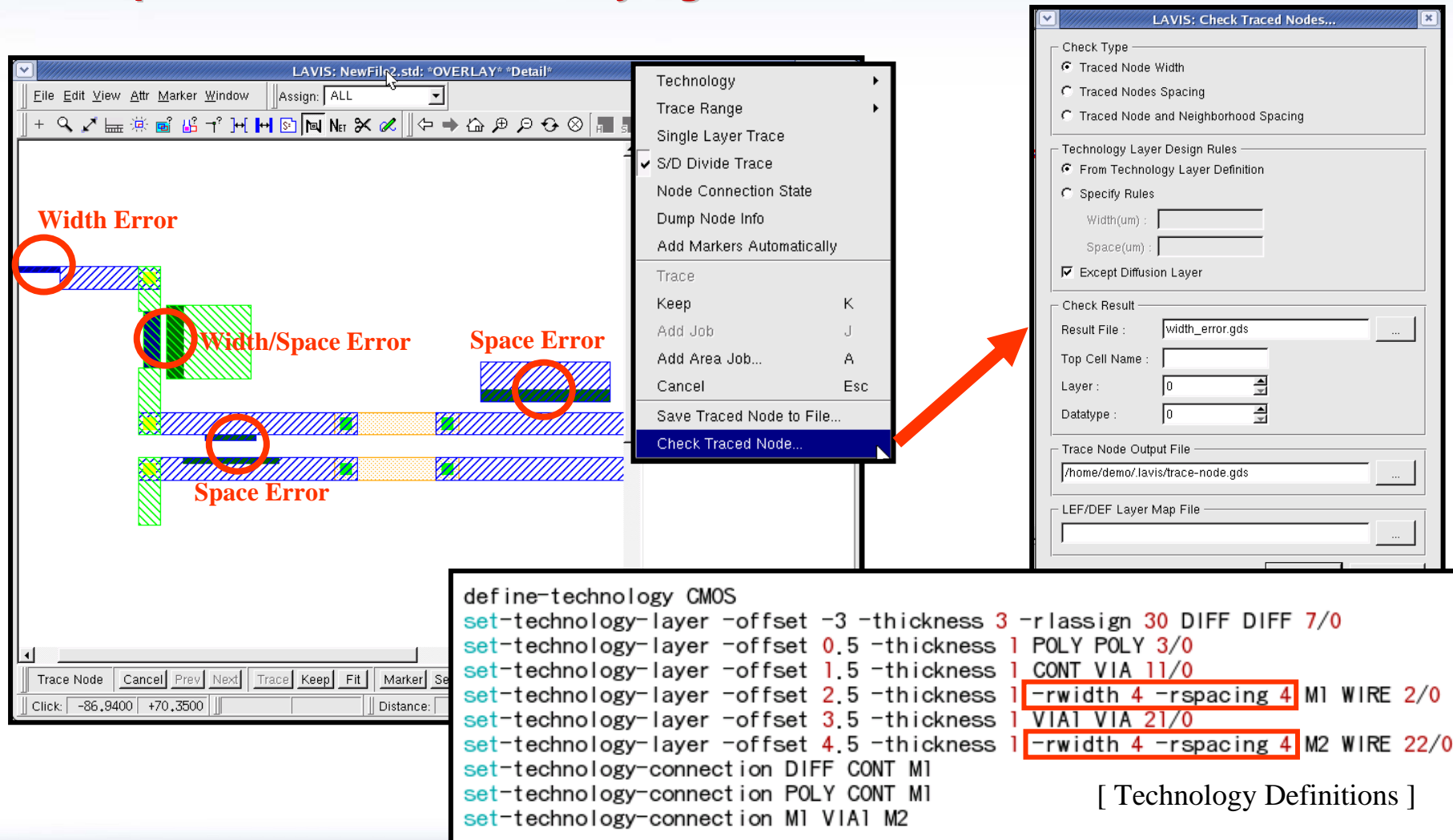
Easy to start node-trace analysis



- Only GDS is needed
- Simple Tech. File
- Trace & Highlight of the same nodes
- Trace the shortest connection of 2 points
- Detect a location of electrical short.



Simple rule check for nearby figures to the traced node



The screenshot shows the LAVIS software interface. The main window displays a layout with several error markers: a red circle labeled 'Width Error' on a blue wire, a red circle labeled 'Width/Space Error' on a green wire, and two red circles labeled 'Space Error' on blue wires. A context menu is open over the layout, with 'Check Traced Node...' selected. An arrow points from this menu item to the 'LAVIS: Check Traced Nodes...' dialog box. The dialog box has the following settings:

- Check Type:
 - ☒ Traced Node Width
 - ☐ Traced Nodes Spacing
 - ☐ Traced Node and Neighborhood Spacing
- Technology Layer Design Rules:
 - ☒ From Technology Layer Definition
 - ☐ Specify Rules
- Width(um):
- Space(um):
- ☒ Except Diffusion Layer
- Check Result:
 - Result File:
 - Top Cell Name:
 - Layer:
 - Datatype:
- Trace Node Output File:
- LEF/DEF Layer Map File:

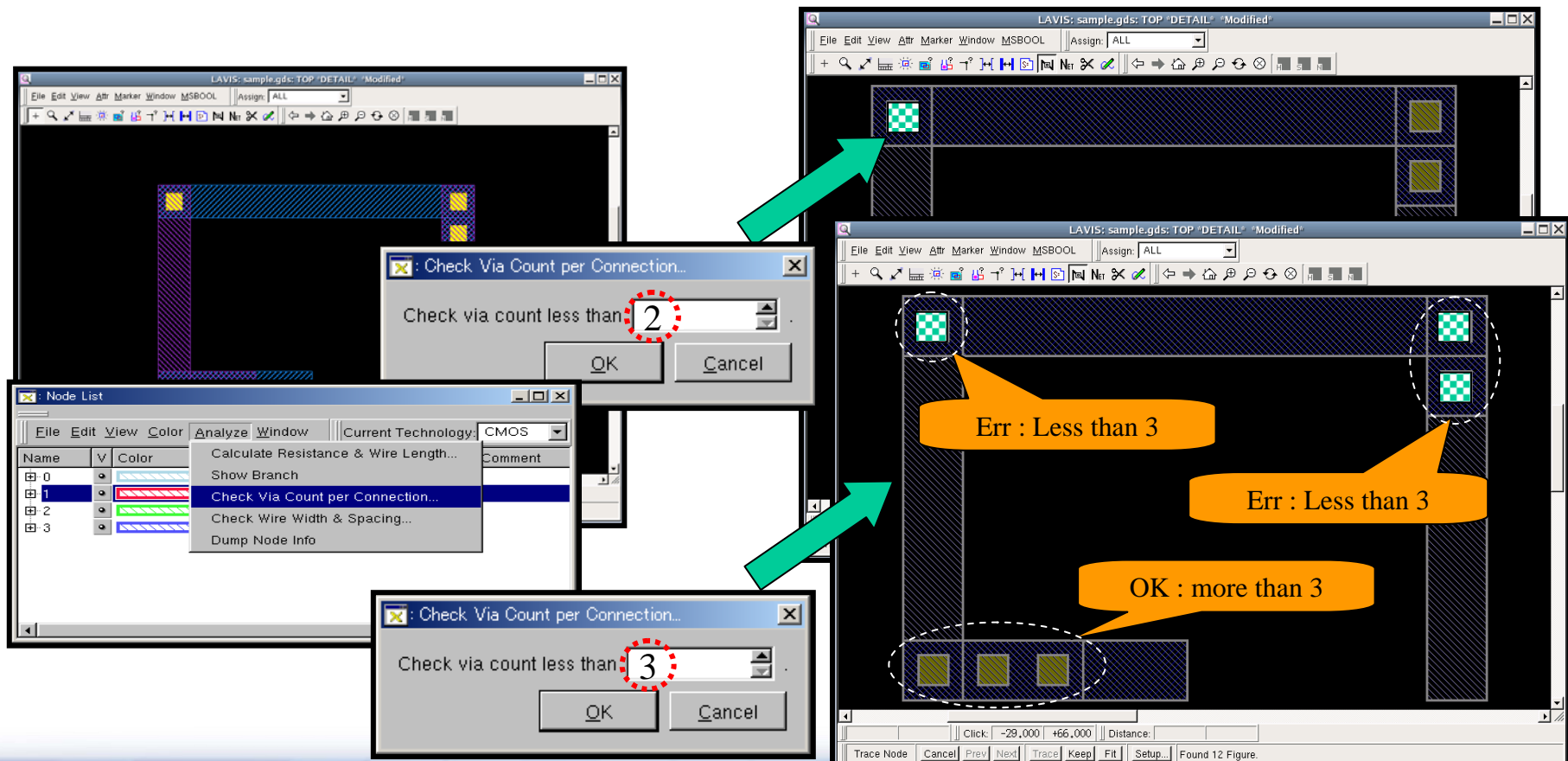
Below the dialog box, a text box contains the following technology definitions:

```
define-technology CMOS
set-technology-layer -offset -3 -thickness 3 -rassign 30 DIFF DIFF 7/0
set-technology-layer -offset 0.5 -thickness 1 POLY POLY 3/0
set-technology-layer -offset 1.5 -thickness 1 CONT VIA 11/0
set-technology-layer -offset 2.5 -thickness 1 -rwidth 4 -rspacing 4 M1 WIRE 2/0
set-technology-layer -offset 3.5 -thickness 1 VIA1 VIA 21/0
set-technology-layer -offset 4.5 -thickness 1 -rwidth 4 -rspacing 4 M2 WIRE 22/0
set-technology-connection DIFF CONT M1
set-technology-connection POLY CONT M1
set-technology-connection M1 VIA1 M2
```

[Technology Definitions]

Node-Trace Additional Function (3)

=> Redundant Via rule check:
Check Via Count per Connections



Node-Trace Additional Function

=> Resistance and Wire Length can be calculated and displayed

The screenshot displays the LAVIS software interface with the following components:

- Node List Window:** Shows a list of nodes (0, 1, 2, 3, 4) and their properties. The 'Analyze' menu is open, highlighting 'Calculate Resistance & Wire Length...'. Other options include 'Show Branch', 'Check Via Count per Connection...', 'Check Wire Width & Spacing...', and 'Dump Node Info'.
- 3D-Trace Window:** Displays a detailed view of the chip layout with various layers and components. A specific wire is highlighted in yellow.
- Calculate Resistance & Wire Length... Dialog:** A modal dialog box with fields for 'Start Point' (Technology Layer, Coordinate (X Y)) and 'End Point' (Technology Layer, Coordinate (X Y)). It also includes 'Via Group Pitch (um)' and 'Via Group Size(um)'.
- Resistance & Wire Length Calculation Result Window:** A window showing the results of the calculation. The results are circled in red and include:
 - Node : 2
 - SP : 948 105
 - EP : 958 675.9
 - R_TOTAL : 0.399
 - L_TOTAL : 570.9
- Callout:** An orange speech bubble points to the 'Resistance & Wire Length info.' text, which is associated with the calculation result window.

MinMax Wire Width by each tech. layer

=> Display Min/Max by each technology layer

The screenshot displays the LAVIS 10.1.0d software interface. The main window shows a circuit layout with various components and wires. A pink callout box highlights the 'Assign' dropdown menu, which is set to 'ALL'. The callout box contains the following text:

```
[TOP]
+--[METAL_1]
| +--[MIN_METAL_1]
| | +--[MIN_0]
| | +--[MIN_1]
| | ...
| +--[MAX_METAL_1]
+--[METAL_2]
+--[METAL_3]
...
+--[ALL] ... 全体のMIN/MAX
+--[MIN_ALL]
+--[MAX_ALL]
```

The right-hand pane shows a file tree for 'result.gds.gz' (GDS File). The tree structure is as follows:

- result.gds.gz (GDS File)
 - All
 - TOP >> 3
 - Poly >> 2
 - MIN_Poly >> 1
 - MIN_23
 - MAX_Poly >> 1
 - MAX_3
 - M1 >> 2
 - MIN_M1 >> 1
 - MIN_26
 - MIN_25
 - MIN_24
 - MAX_M1 >> 1
 - MAX_4
 - Diff >> 2
 - MIN_Diff >> 1

=> Node List can display an area and a perimeter information of traced node

The image shows two screenshots of the LAVIS Node List window. The first screenshot shows the 'View' menu with 'Show Perimeter and Area' highlighted. A blue arrow points to the second screenshot, which shows the 'Dump Node Info' option selected in the 'Analyze' menu. A second blue arrow points down to a third screenshot showing the resulting table with perimeter and area data.

LAVIS: Node List

File Edit View Color Analyze TraceArea Window

Current Technology: CMOS018 Brightness: 0 Node Select

Traced Node Special

Name V Color

00000

Calculate Resistance & Wire Length...
Show Branch
Check Via Count between 2 Points...
Check Via Count per Connection...
Check Max Via Resistance...
Check Min/Max Wire Width...
Check Wire Width...
Check Spacing...
Check Neighborhood Spacing...
Dump Node Info

Cell Technology Comment

[TraceSample.gds] CMOS018

LAVIS: Node List

File Edit View Color Analyze TraceArea Window

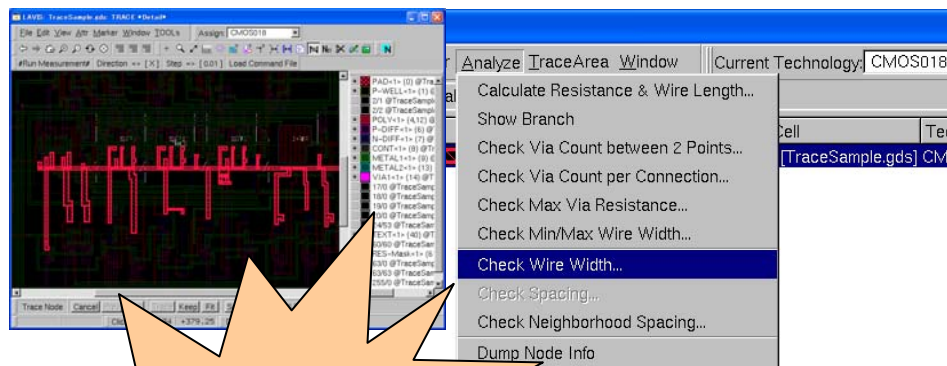
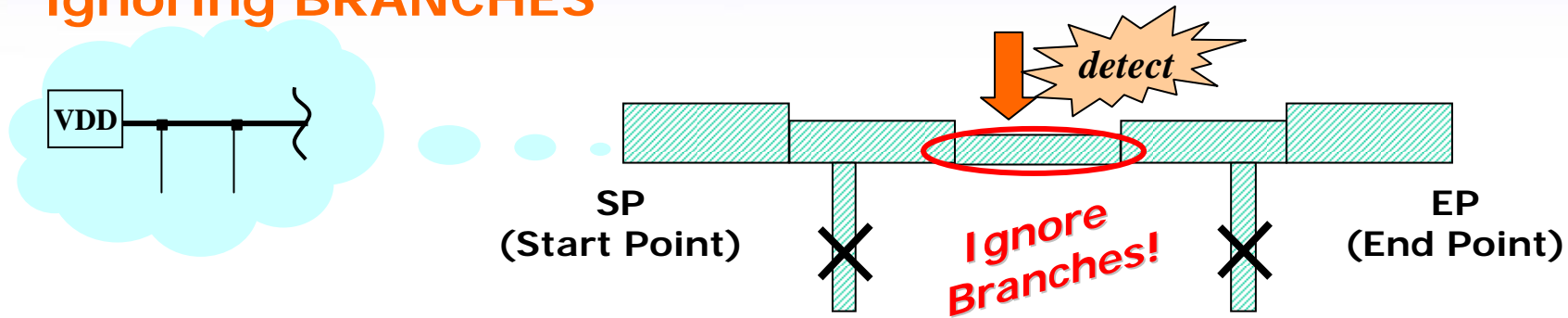
Current Technology: CMOS018 Brightness: 0 Node Select

Traced Node Special Node

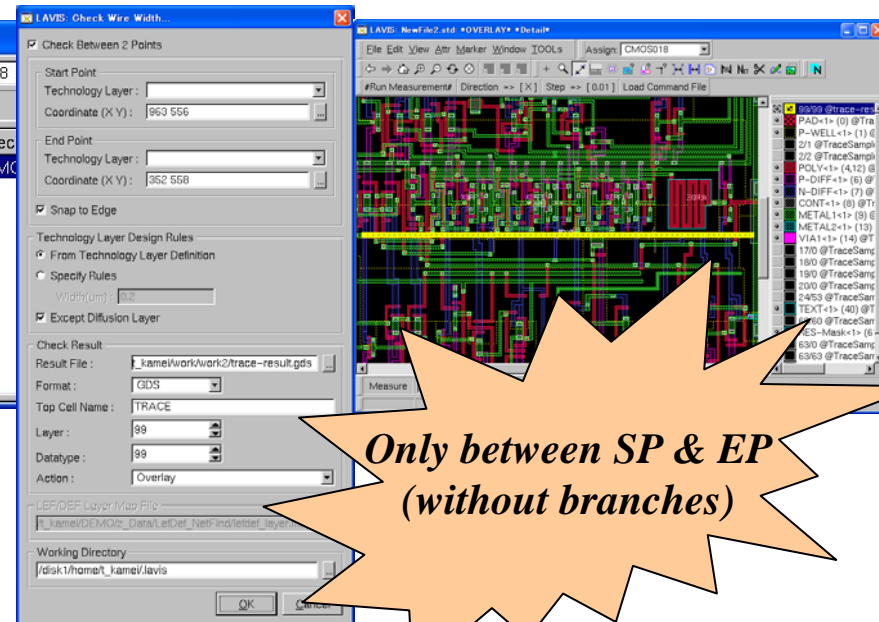
Name	V	Color	Figures	Perimeter	Area	Trace Area	Trace Cell	Technology	Comment
00000			66	7230	35333		TRACE [TraceSample.gds]	CMOS018	

Check wire width between 2 points

- Check Wire Width between the specified SP & EP points ignoring BRANCHES

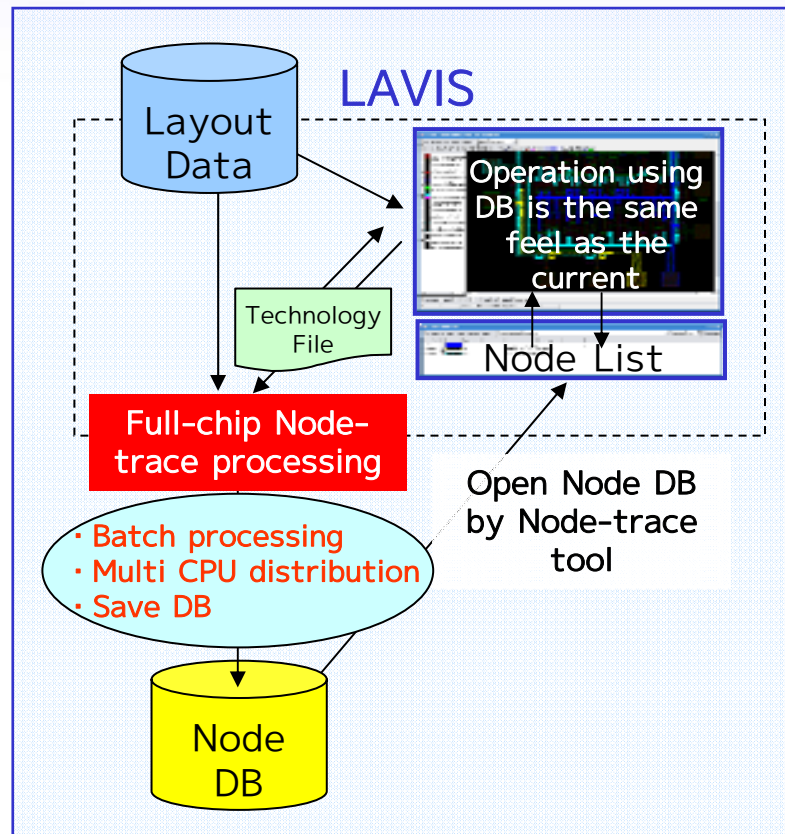


*Conventional way
check width
whole traced node*



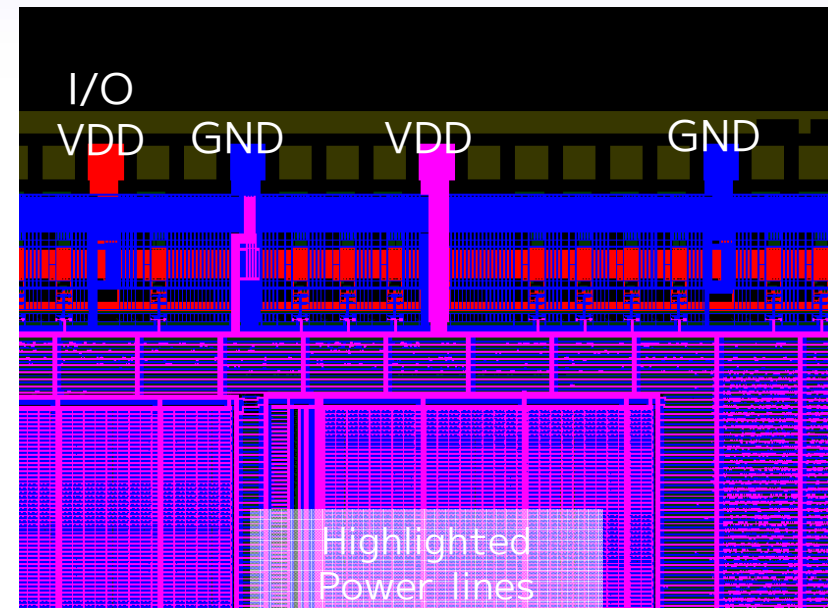
*Only between SP & EP
(without branches)*

Batch process Node-trace flow



◇ Batch process node-trace flow

All nodes extracted at chip level once are saved as a node DB



◇ Case of power lines tracing

Enables to check easily wires of huge net with many figures, and multi power lines running at chip level using a node DB

10s~100s times faster than interactive mode!

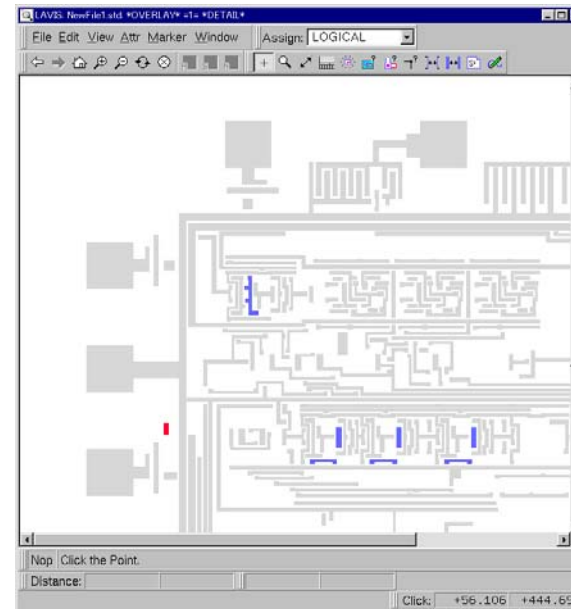
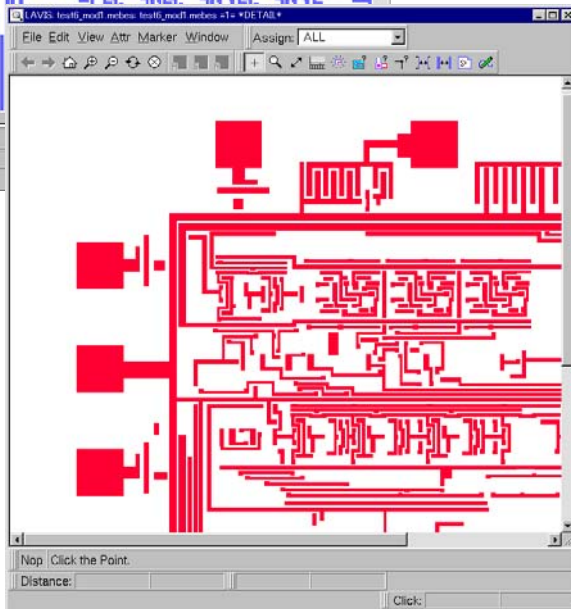
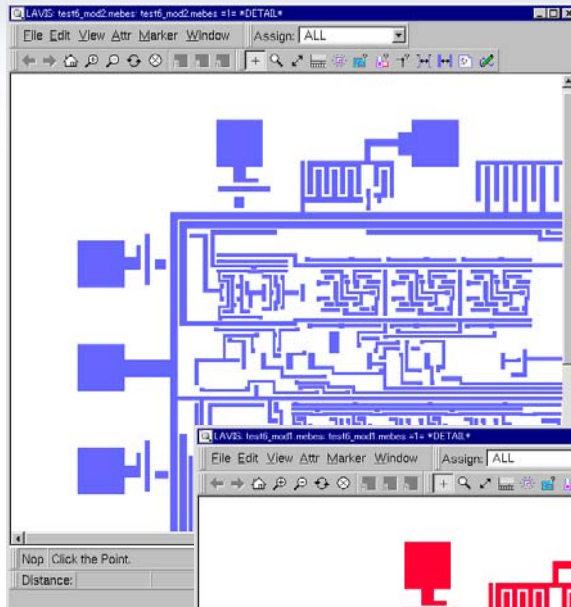
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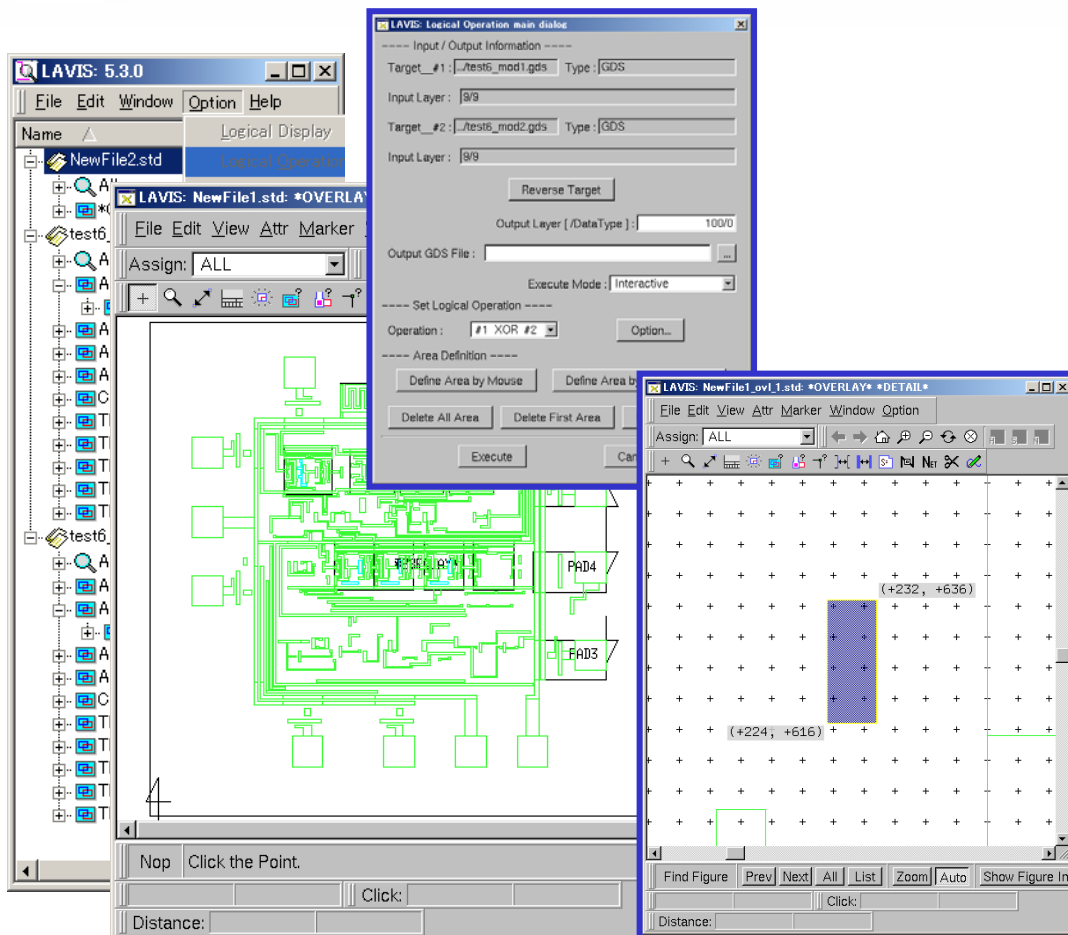
Layout Comparing Check

ECO Check & Compare

- **Overlay & Image Data Paste**
- **Overlay Display - GDS/LEFDEF/EBs**
- **Quick Comparison & Difference Check**
- **Easy to set - Scale/Origin/Rotation**



Boolean Operation & Display



Boolean Operation of overlaid data

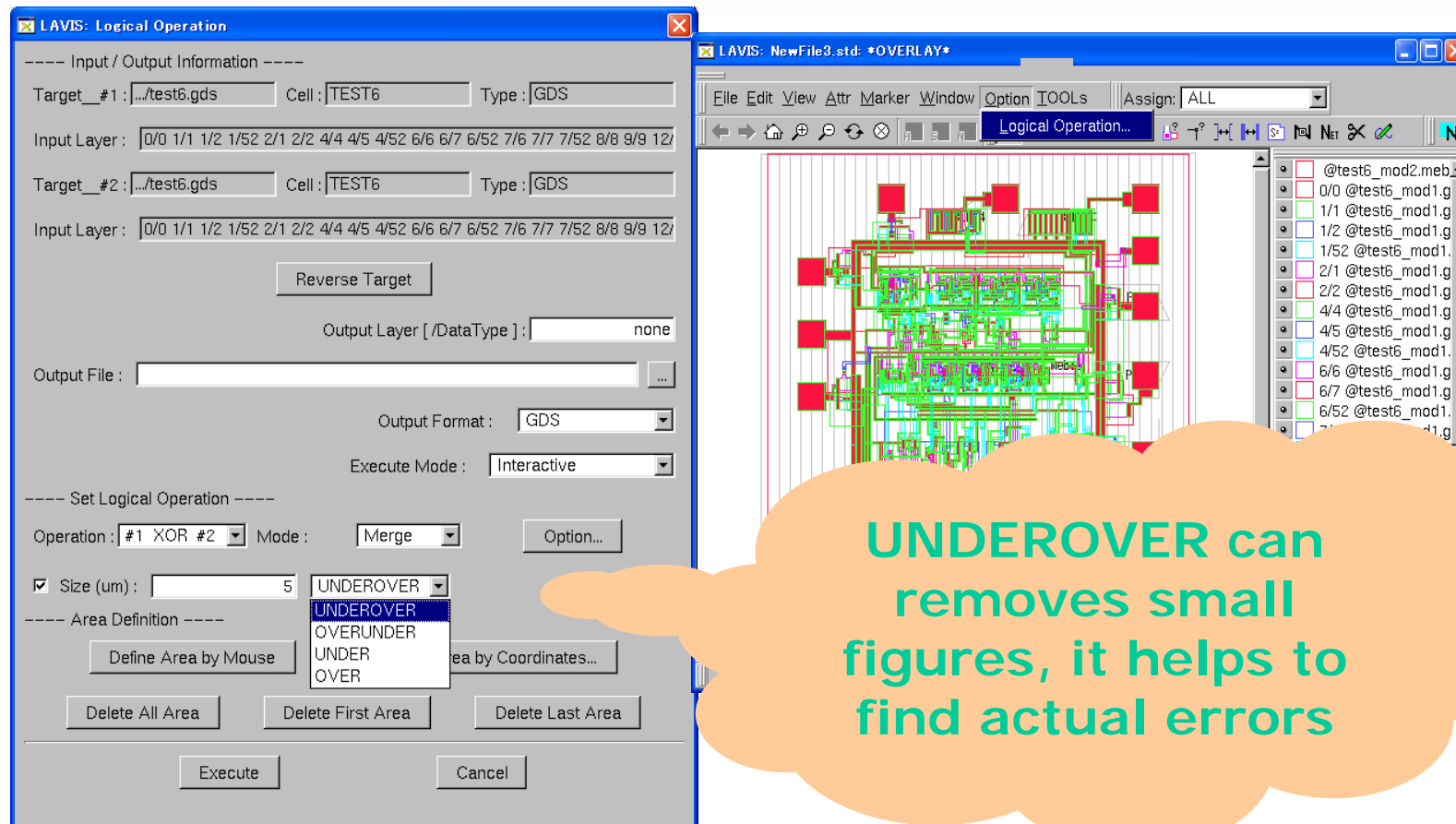
- XOR
- AND
- OR
- SUB

Display the result in GDSII

List up the results

Enable to navigate all geometries by selecting the line in the checklist

=> LogicalOperation/Ivlogic, resize(underover, etc)
operation after boolean operation.



UNDEROVER can
removes small
figures, it helps to
find actual errors

I/F with Sign-off DRC/LVS Tools

LAVIS

Layout Verification Analysis and Layout Revision

Layout Verification

Error DB

lverrdb2gds

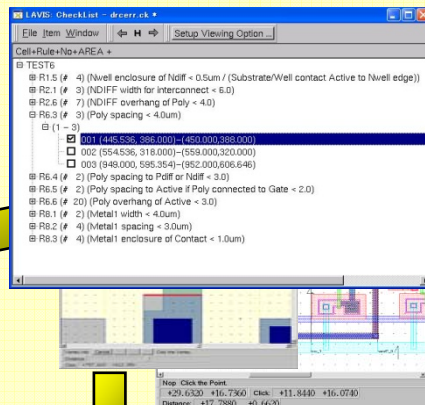
GDSII
(error data only)

LAVIS

Quick look at entire
error distribution

one-by-one review
& revision

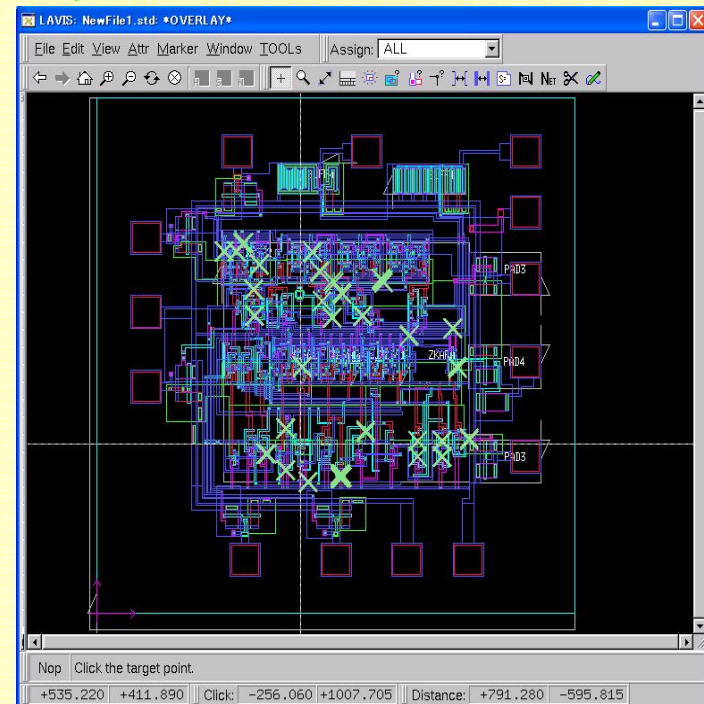
Check List



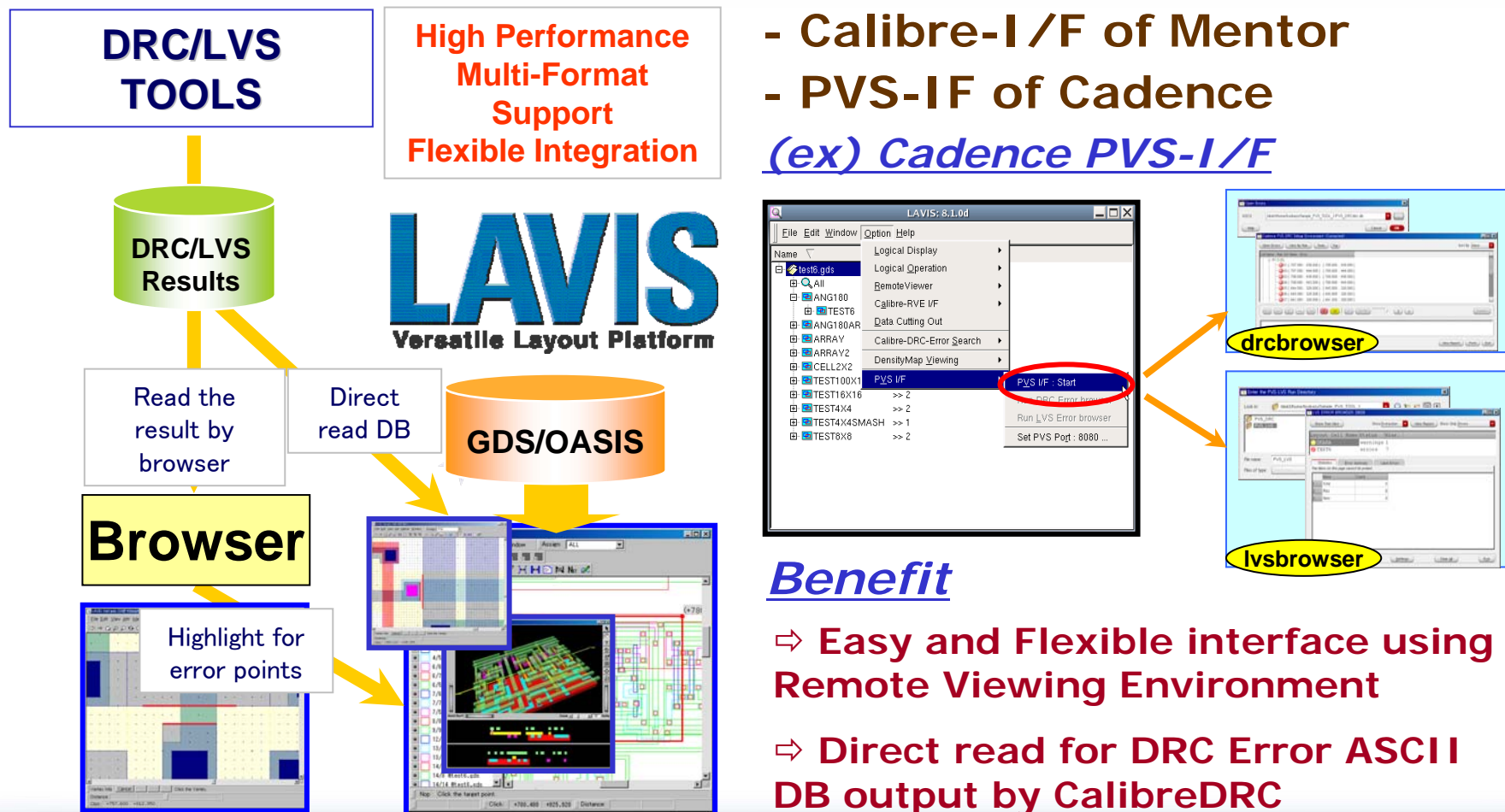
custom layout
capable editor

Out of capacity

Simple Edit



Interface with 3rd party tools



LAVIS

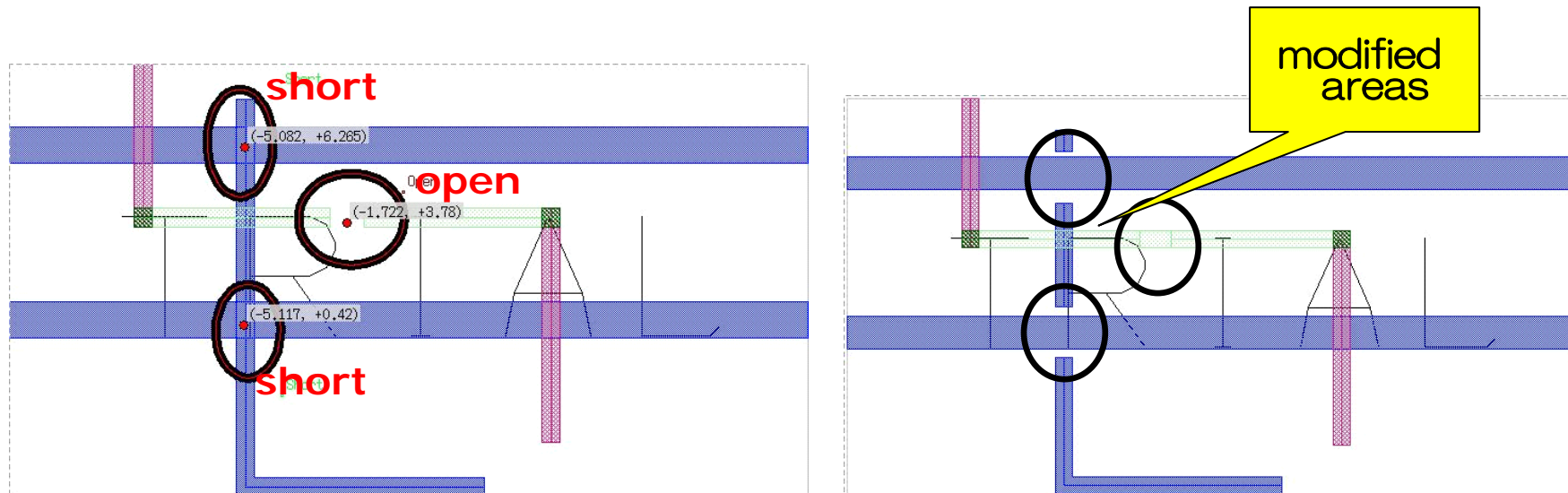
Versatile Layout Platform

ECO & Hot fixing On GDS/OASIS

❑ Hot Fix for Layout Verification

- ❖ Quick layout modification – add/delete/move text, elements & cell
- ❖ Create new GDS/OASIS data

For fixing a tiny bit of errors to get the short free data



⇒ Fix the DRC/LVS errors in the early phase of design flow, feedback to the original data, and shorten the total verification TAT

Items	Functions				
File Handling	Create File				
Cell Handling	Create Cell	Copy Cell	Delete Cell		
Figure, Cell Input	Input Boundary	Input PATH	Input TEXT	Input Cell (SREF)	Input Array Cell (AREF)
Figure, Cell Selection	Select Figure & Cell	Select Side of Figure	Select Vertex of Figure	Select Multi-Figure	
Selected Figure, Cell Editing	Move Selected Figure & Cell	Copy Selected Figure & Cell	Delete Selected Figure & Cell	Change Parameter of Selected BOUNDARY	Change Parameter of Selected PATH
	Change Parameter of Selected TEXT	Change Parameter of Selected Cell (SREF)	Change Parameter of Selected Array Cell (SREF)	Rotate Selected Figure & Cell	Mirror Selected Figure & Cell
	Add Sequential Figure	Divide Figure	Move Selected Figure & Side	Move Vertex of Selected Figure	Resize Figure
	Figure Logical Operation	Selected Figure & Cell Instantiation	Selected Array Cell Expansion	Selected Cell Expansion	Selected TEXT Expansion
Others	UNDO, REDO	Incorrect Figure Prohibition Mode	Resume Function for Abend	QUIT Editing Cell Information	QUIT All Editing Information



Available



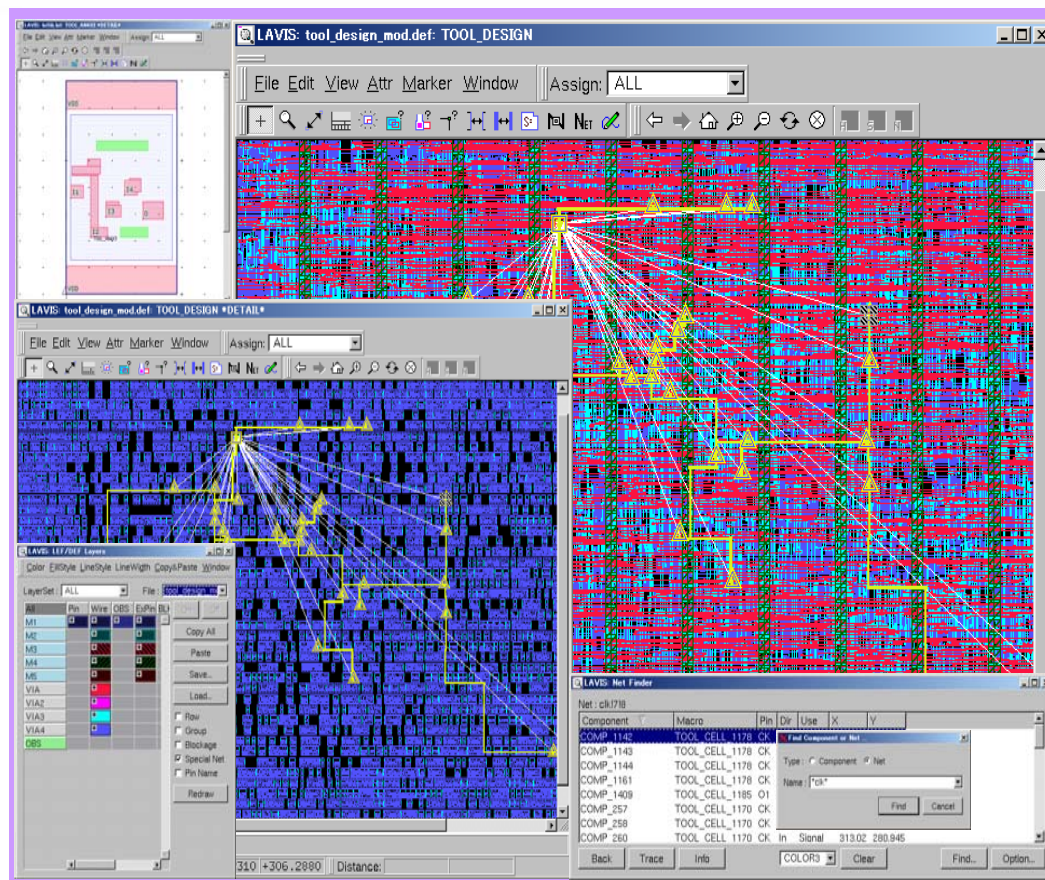
Not available

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LEF/DEF Interface

Trace net & component on LEF/DEF display



- Trace/Find Net & Component

- Visual Track/ Check of CLK Tree

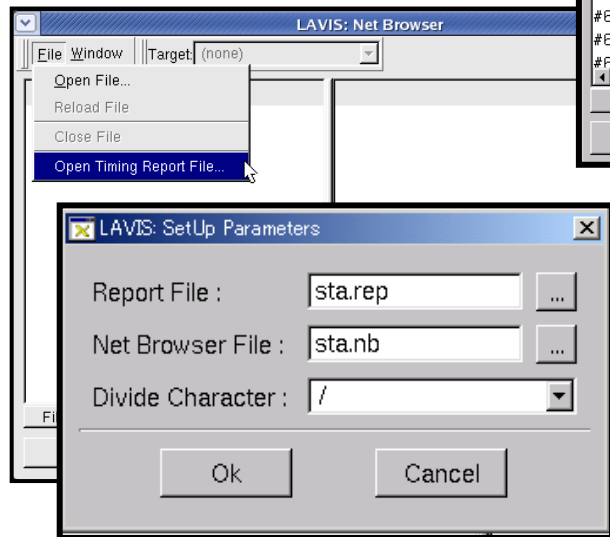
- Visual Track/Check of Critical Path by TA

- Scan Path check, etc.

- Overlay LEF vs GDSII

- Check Cell/IP ports & Obstacles

Timing Analyzer



LAVIS: Net Browser

File Window Target: tool_design_mod.def

No	Target(GroupName)	Edge/Type	Timing Information
#1_0	Primary (G1)	##max##	Slack=-0.360(VIOLATED)
#1_1	Data	rise	data arrival time=11.084
#1_2	Clock	fall	data required time=10.7
#2_0	Primary (G2)	##max##	Slack=1.361(MET)
#2_1	Data	rise	data arrival time=9.365
#2_2	Clock	fall	data required time=10.7
#3_0	Primary (G3)	##max##	Slack=1.362(MET)
#3_1	Data	rise	data arrival time=9.364
#3_2	Clock	fall	data required time=10.7
#4_0	Primary (G4)	##max##	Slack=1.305(MET)
#4_1	Data	fall	data arrival time=14.93
#4_2	Clock	rise	data required time=16.2
#5_0	Primary (G5)	##max##	Slack=1.305(MET)
#5_1	Data	fall	
#5_2	Clock	rise	
#6_0	Primary (G6)	##max##	
#6_1	Data	fall	
#6_2	Clock	rise	

No	Timing Path/Route	Prop./Note	In	Out	Fanout	Load	Incr	Path
1	Level0_0/Comp_0 (Cell_0)			pin0			0.000	0.000
2	Level0_0/net_0 (net)				2	0.034		
3	Level0_0/Comp_1 (Cell_1)		pin1	pin2			0.162	0.162
4	Level0_0/net_1 (net)				2	0.040		
5	Level0_0/Level1_2/Level2...		pin3	pin2			0.302	0.464
6	Level0_0/Level1_2/Level2...				1	0.011		
7	Level0_0/Level1_2/Level2...		pin1	pin2			0.134	0.598
8	Level0_0/Level1_2/Level2...				1	0.021		
9	Level0_0/Level1_2/Level2...		pin1	pin2			0.075	0.673
10	Level0_0/Level1_2/Level2...				1	0.021		
11	Level0_0/Level1_2/Level2...		pin1	pin2			0.099	0.772
12	Level0_0/Level1_2/Level2...				3	0.051		
13	Level0_0/Level1_3/Level2...	(gclock source)	pin3	pin2			0.133	0.905

LAVIS: tool_design_mod.def: TOOL DESIGN

File Edit View Attr Marker Window Help

Assign: ALL

Filter:

Open

Legend:

- \$M1-Pin @tool_design
- \$M1-Obs @tool_design
- \$M1-Wire @tool_design
- \$V1A-Wire @tool_design
- \$M2-Wire @tool_design
- \$V1A2-Wire @tool_design
- \$M3-Wire @tool_design
- \$V1A3-Wire @tool_design
- \$M4-Wire @tool_design
- \$V1A4-Wire @tool_design
- \$M5-Wire @tool_design
- \$M1-ExPin @tool_design
- \$M2-ExPin @tool_design
- \$M3-ExPin @tool_design
- \$M4-ExPin @tool_design
- \$M5-ExPin @tool_design
- \$M1-Track @tool_design
- \$M2-Track @tool_design
- \$M3-Track @tool_design
- \$M4-Track @tool_design
- \$M5-Track @tool_design

Click the target point.

Click: Distance:

LAVIS can read a timing report of TA tool

LAVIS

Versatile Layout Platform

Gate-pass Route Trace - LEFDEF I/F -

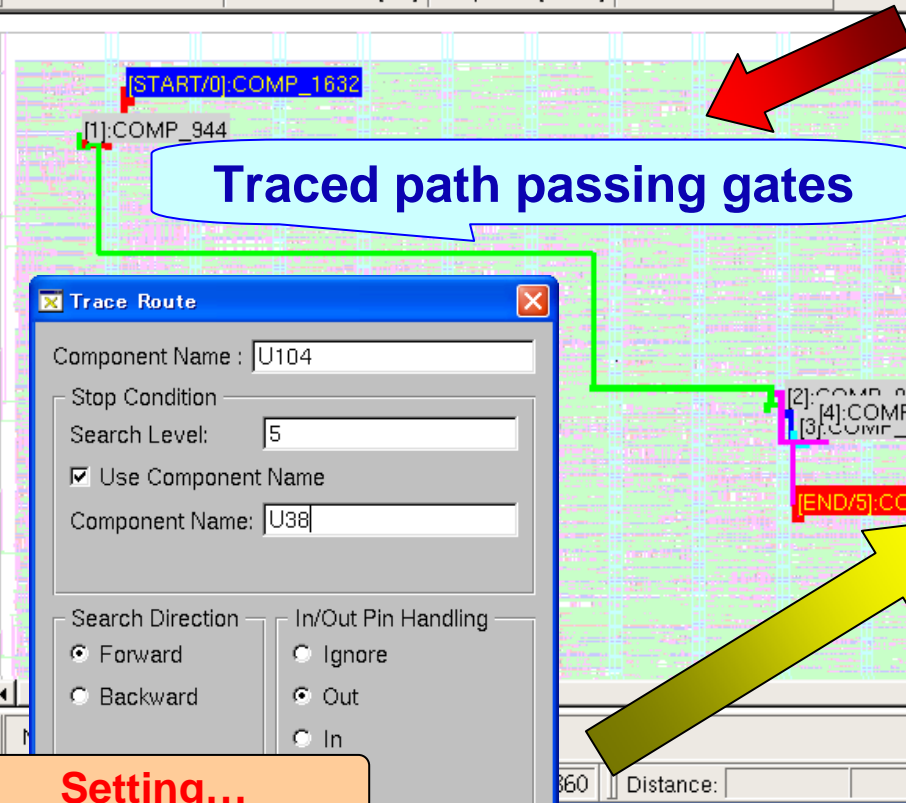
xwud: LAVIS: tool_design_mod.def: TOOL DESIGN

File Edit View Attr Marker Window TOOLS

Assign: ALL



#Run Measurement# Direction => [X] Step => [0.01] Load Command File



Trace Route

Component Name : U104

Stop Condition

Search Level: 5

☒ Use Component Name

Component Name: U38

Search Direction

☒ Forward

☐ Backward

In/Out Pin Handling

☐ Ignore

☒ Out

☐ In

Setting...

Technology: (none)

OK

Cancel

xwud: PathTrace: Component Tree

Tree Trace Option

Name	Dir	Pin(From)	Pin(To)	Net(To)
[*]COMP_1632	F		O1	NET_1458
COMP_944	F	I2	O1	NET_1462
COMP_949	F	I3	O1	NET_1472
COMP_974	F	I4	O1	NET_1476
COMP_513	F	D	Q	NET_1477
COMP_1637	F	I1	O1	NET_1953
COMP_1645	F	I1	O1	NET_1716
COMP_1660	F	I1	O1	NET_1479
COMP_2194	F	I3	O1	NET_1478
COMP_513	F	D	QB	NET_1266
COMP_975	F	I1	O1	NET_1481

Traced component tree

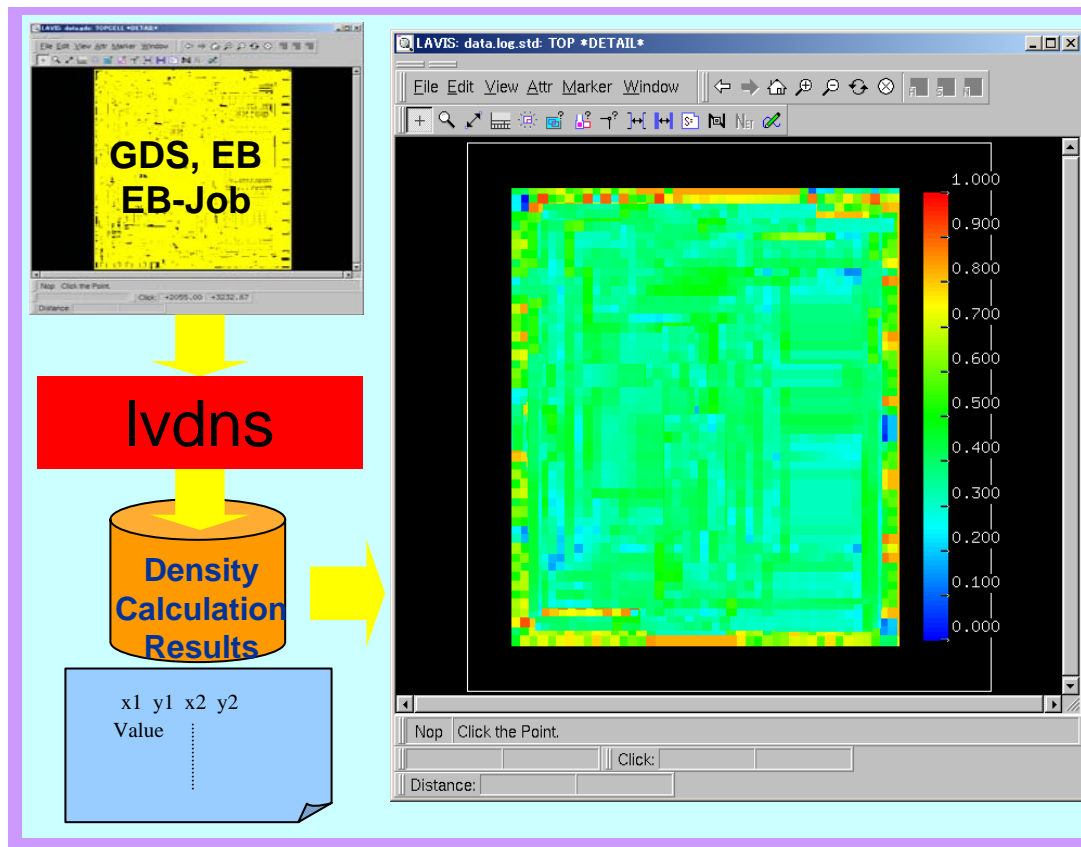
Useful debug window for analyzing paths

LAVIS

Versatile Layout Platform

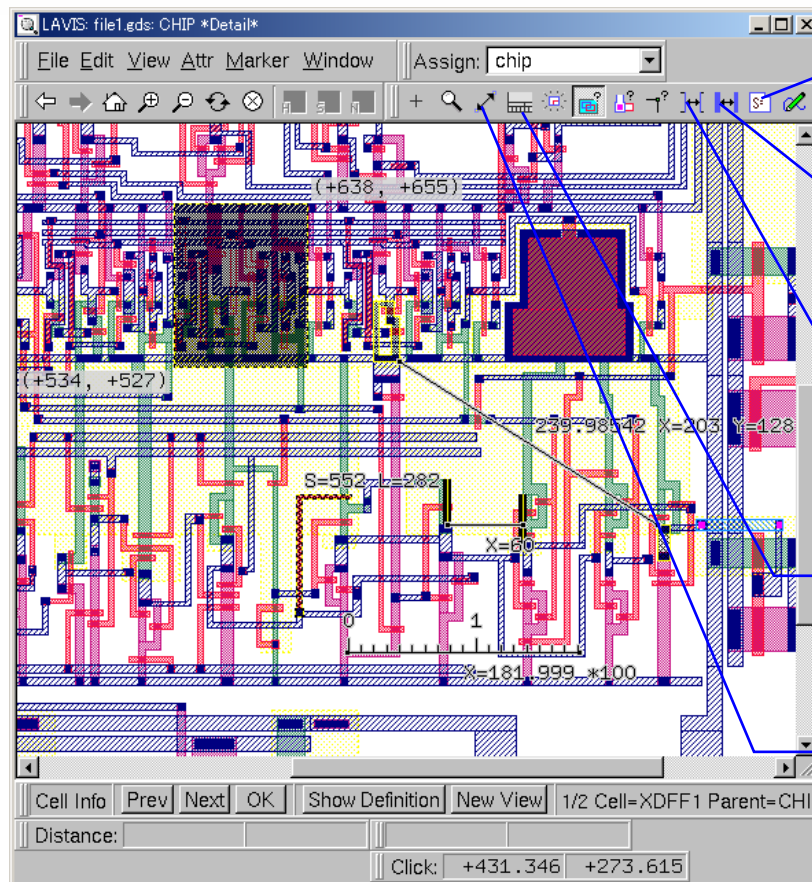
Other Features

■ Displaying a color map for an analytical calculation result



- Geometry-based (Layout patterns) density calculation result
- Voltage drop calculation
- The density calculation utility is bundled in LAVIS

■ Providing various types of measurement tools



Measure Area Tool
Area/Perimeter

Measure Figure Tool
2-figure interval

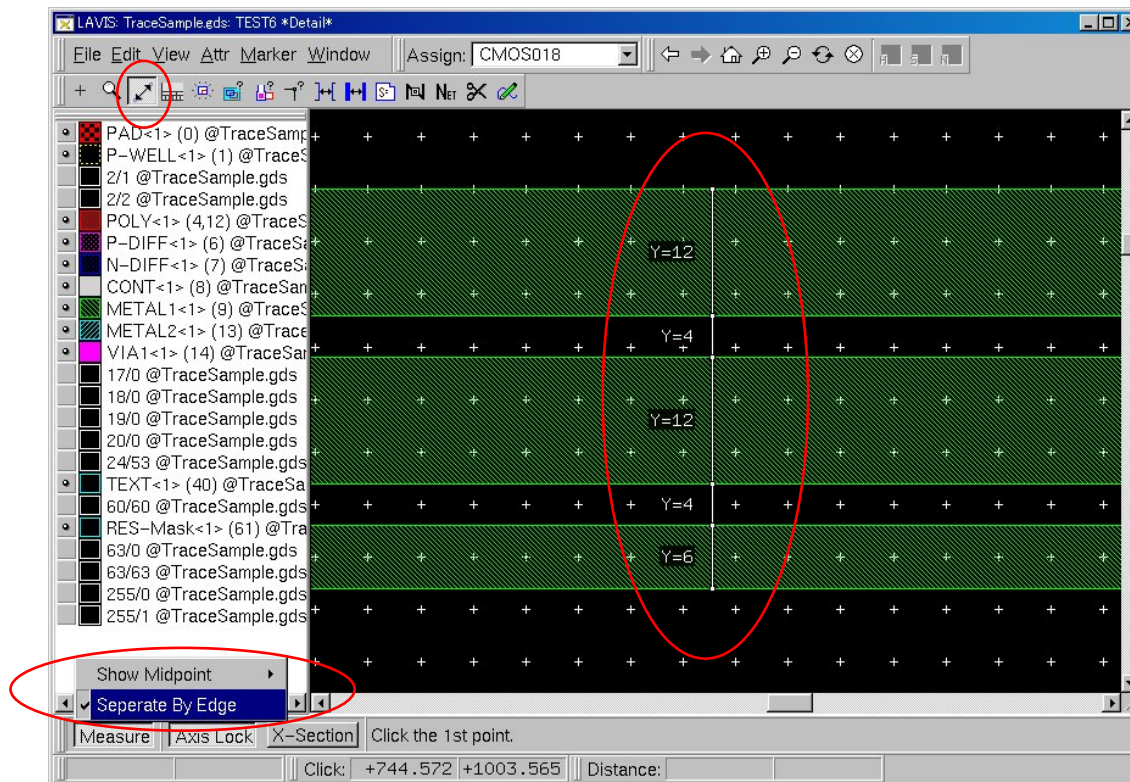
Measure Edge Tool
2-sided space/width

Ruler Tool (Scale)
2-point distance

Measure Tool
2-point distance

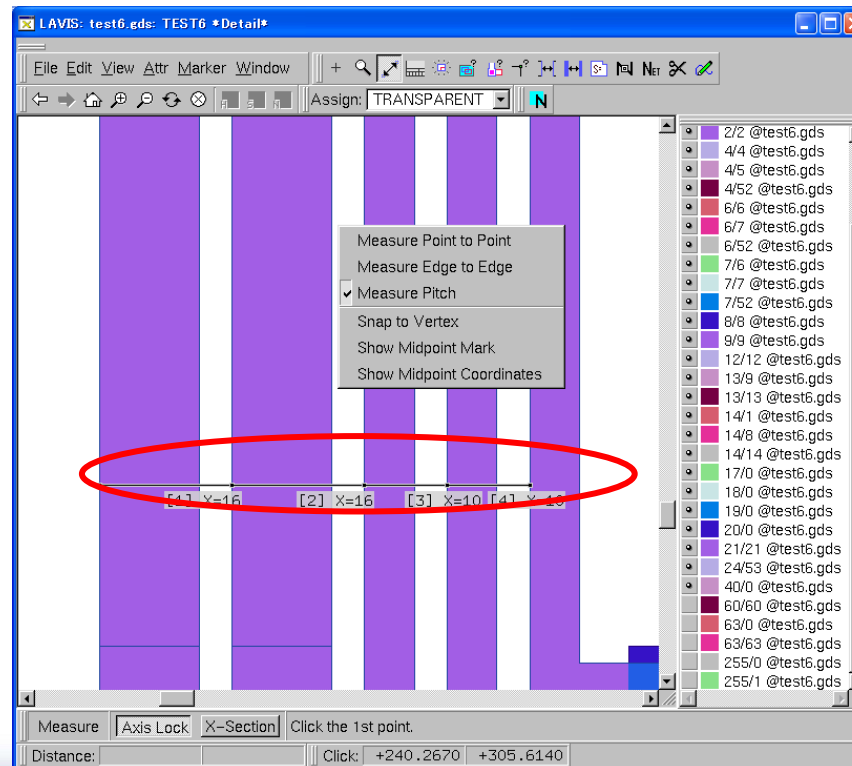
Measurement Tool has the new option

=> Line & Space can be measured at a time



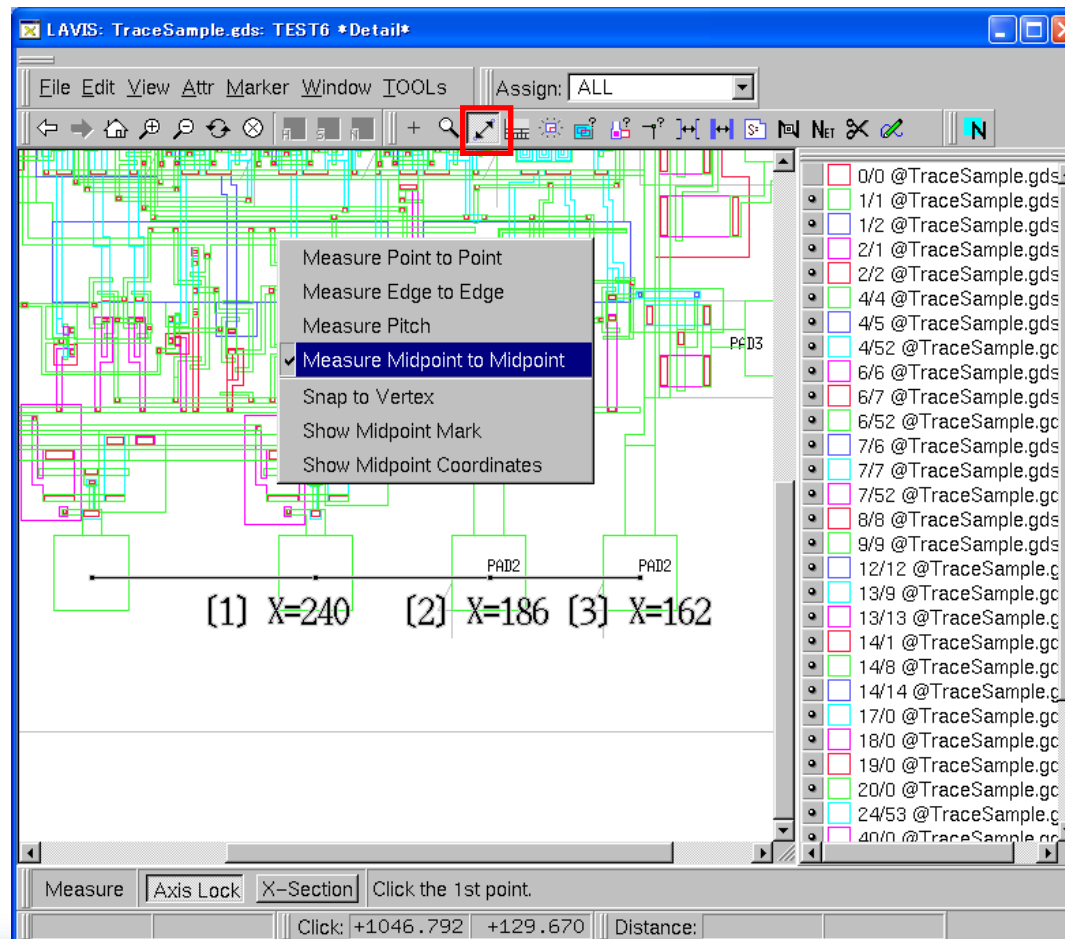
03. Pitch measurement for line & space

=> MeasureTool has pitch measurement function for L/S
(detect the same side edge)
Also it says the number which stands for how many
pitch(es) from the end



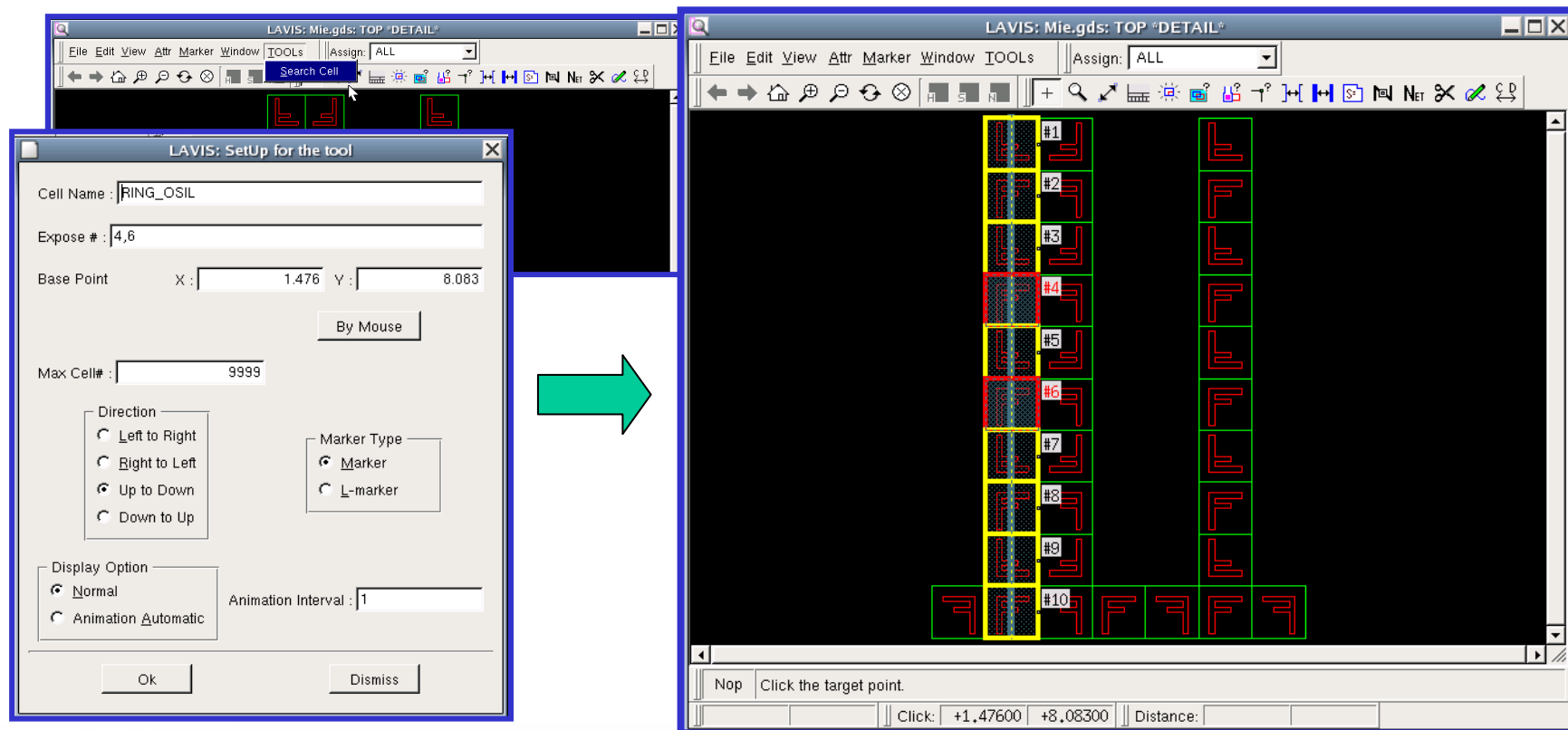
Measure between 2 midpoints

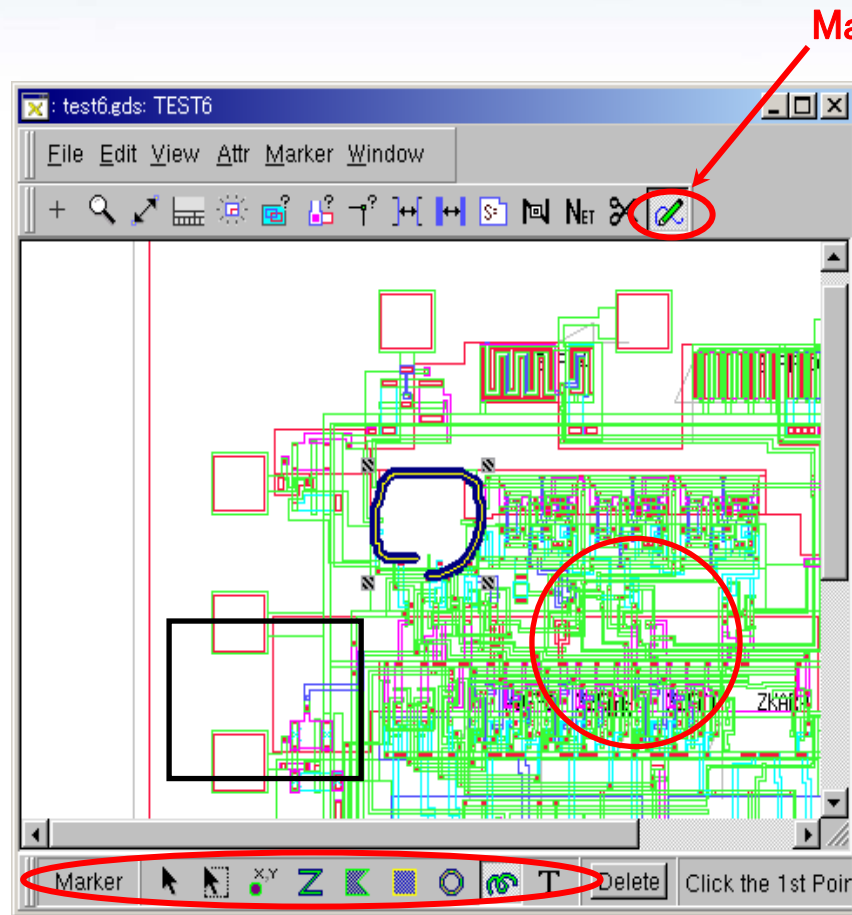
=> "Measure Midpoint to Midpoint" can be available on
MeasureTool



<>Feature: SerchCell

Easy finding cell for the specified view area and showing order number automatically





Marker

Enable to set & save various types of Marker

- Line
- Rectangle
- Polygon
- Circle
- Freehand
- Text
- Bitmap,etc ...

More Easy to do check and revision of layout data


By taking advantage of

LAVIS *High-performance Multi-use Layout Analyzer*

- Super high-speed & huge data display
- Powerful layout check and debug capabilities
- Abundant interfaces with popular EDA tools

for the physical design and verification flow

LAVIS *can shorten Turn Around Time
& provide the High Cost-Performance*



tool

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E-mail : lavis@tool.co.jp

