LAVIS

Ver.10.2

Multi-use Layout Analyzer

TOOL CORPORATION

http:// www.tool.co.jp

1105-1E

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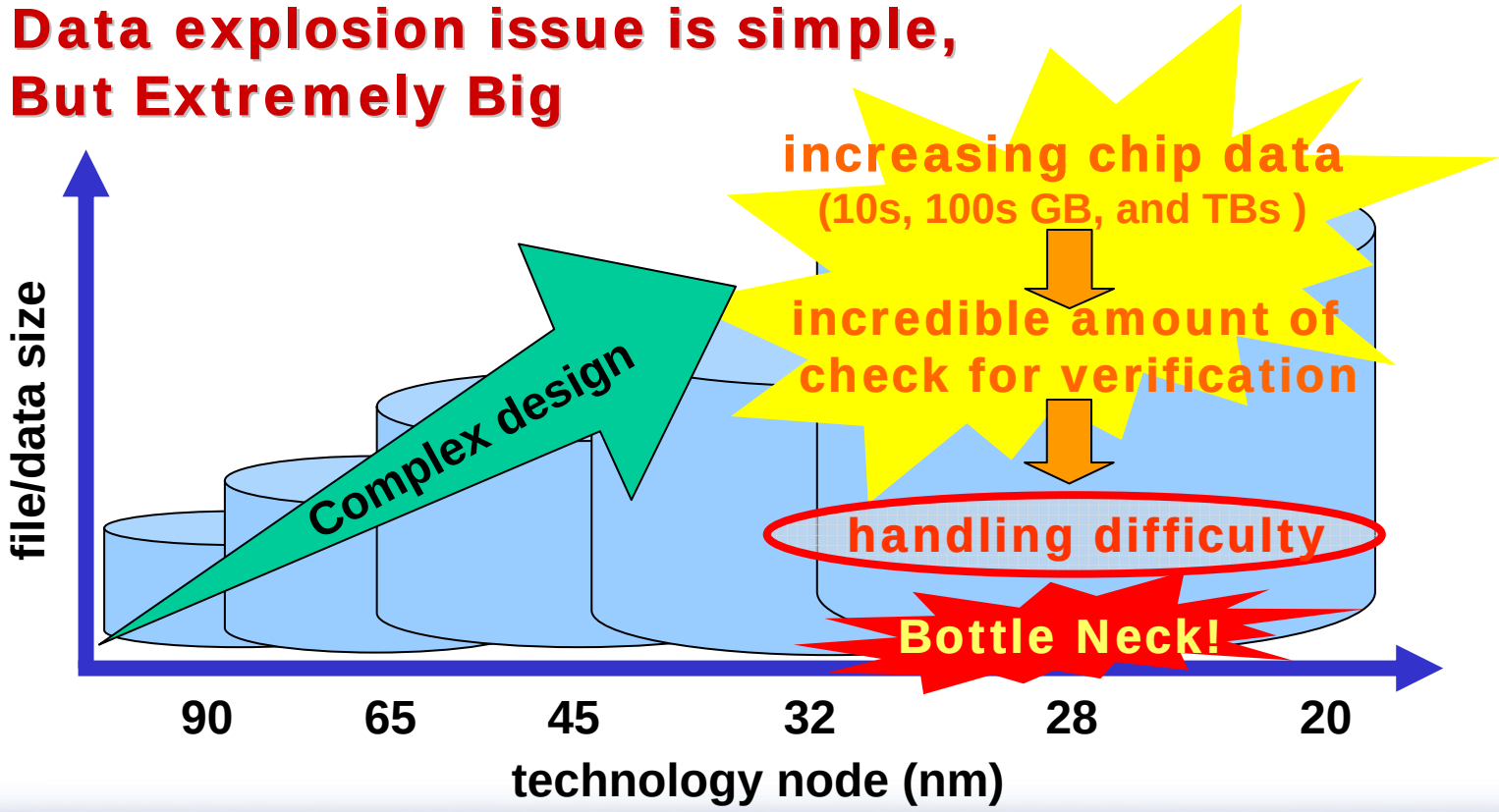
Various Issues in Advanced Process

New issues

- Power, Signal Integrity, DFM, DFT, so on
- Many verifications and checks are required
- All those data is getting too large to handle

=> Data explosion issue is simple, But Extremely Big



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How to fix needs in each process ?

- How to handle incredible amount of data?
- How to check sea of results of verification?
- How to satisfy needs in each process?
  (usually an individual tool in each process)
  - ✓ For Physical Design
  - ✓ For Failure Analysis
  - ✓ For MDP (Mask Data preparation)
- Not only performance but also useful functions
  to improve the quality & the productivity

LAVIS Layout Analyzer Can Provide Solutions

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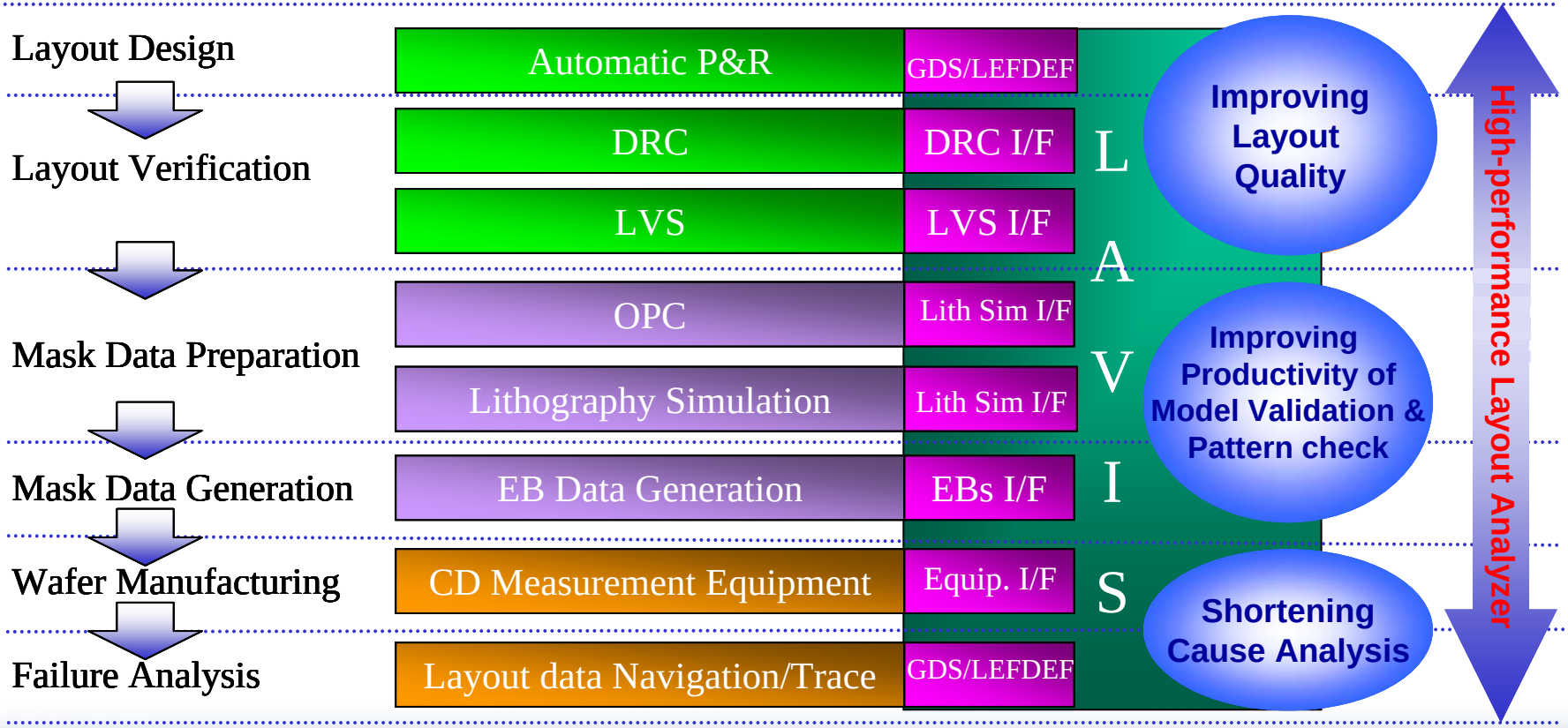
High-performance Layout Visualization Analysis Platform

- LAVIS provides:
  - Common operating super high-speed and huge data display
  - Powerful analyzing capabilities and abundant Interfaces
  - A simple, cost-effective, easy to use solution



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LAVIS High-performance Multi-use Layout Analyzer

- Super high-speed and enormous layout data display
  - Stress free opening and drawing any large layout data
  - Improve layout visualization checking productivity tremendously
- Powerful layout analysis capability to improve the quality of Layout Design and the productivity of MDP and Silicon FA
  - Multi-format and many sophisticated check/debug functions and utilities for Layout Verification, Si Failure Analysis, and Mask Data Preparation
- Abundant interfaces for physical verification, litho-simulation, CD-measurement, and Failure Analysis
  - Various interfaces with popular DRC/LVC, DFM/OPC tools and semiconductor equipment like Inspection and Failure Analysis
- Enable to reduce Verification/Analysis Cost & TAT by using affordable and convenient Layout Analyzer
  - Fill the gaps between the automatic and the nonautomatic checking processes in the one-pass sign-off design & verification flow
  - Common layout platform across the entire physical design flow

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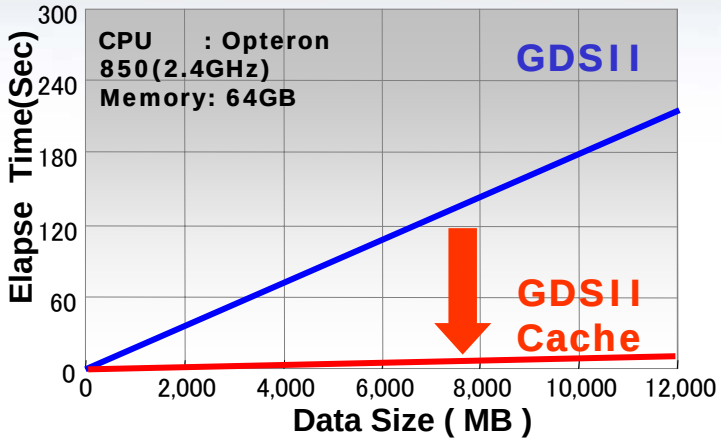
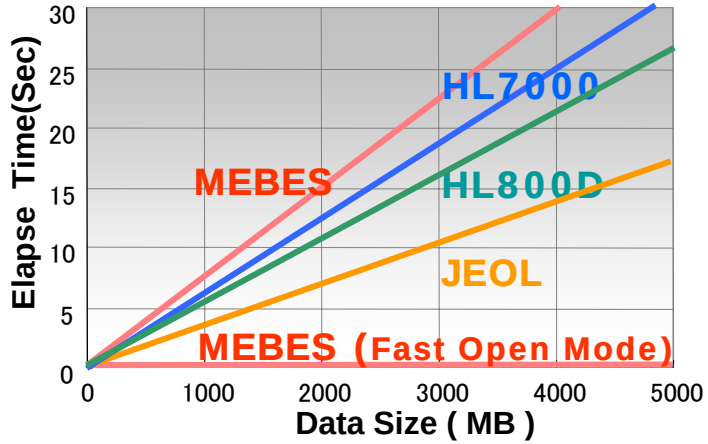
Super High Performance





Opening Time

GDSII 1GB / 20sec.
x1/20(use cache)

EB 1GB / 10sec.

Drawing Time

2-3sec.

Track Record

GDSII 500GB / 4 hours
(memory size: 100GB)

Other viewer can handle such huge data with High-performance?

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Powerful Functions & Useful Interfaces

■ Visual debug & check capabilities for all needs

Functions:

- **Node-Trace**
- **Overlay & Image Paste**
- **Boolean Operation**
- **LEF/DEF, Find net&cell**
- **GDS/OASIS Simple Edit**

- Synchronized Views
- Data Cutting out
- Set & Save Markers
- Measurement & Search
- Compressed data
- direct read
- Color Map Display
- X-section & 3D Display
- Remote Viewing

Interfaces:

- Calibre DRC Interface
- DRC & LVS I/Fs
- Litho. Sim. I/Fs
- CD Measurement I/Fs
- Other Equipment I/Fs

Utilities:

- Virtuoso env. conv.
- Boolean operation
- GDSII/ASCII conv.
- Cache file make
- Density calculation

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Physical Design Flow

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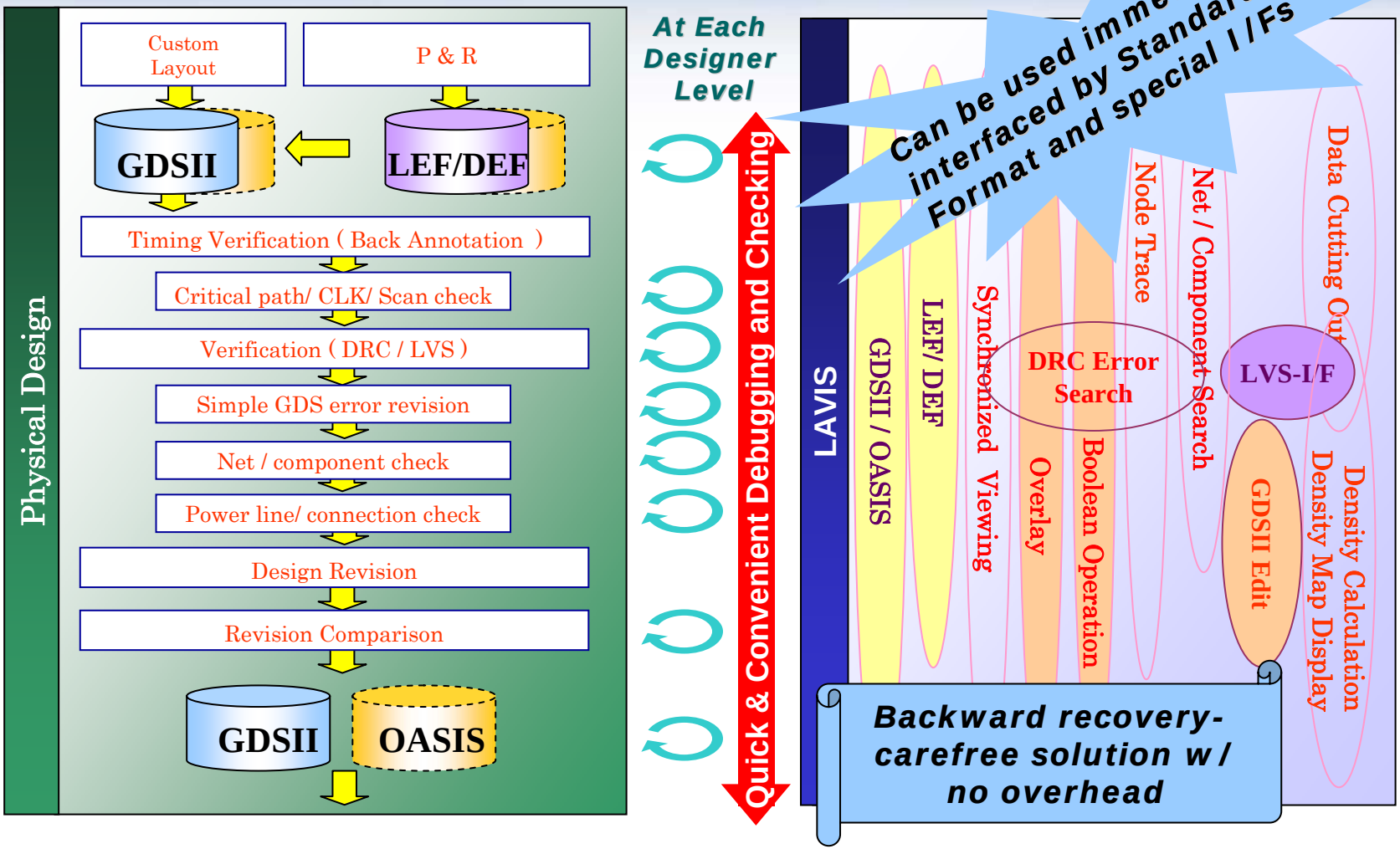
Quick & Convenient Visualization Analysis in all parts of layout design



Improving the Efficiency of your Layout Design Work and the Layout Quality

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How LAVIS works in your Physical Design Flow

In Physical Design Process

(even for Analog/Mixed-signal Design)

LAVIS enables to improve your **Layout Quality** and **Efficiency of Your Work** by yourself using with a sense that you can check **CONVENIENTLY**

- ***what you want***
- ***when you want***
- ***all you want***

in all parts of layout design

with **No Iteration** and **No Overhead**

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How LAVIS works for Physical Design (2)

- **Quick layout rule check in specified areas and on traced nodes - relatively small area**

  As “simple layout checker”

  - Width/Space/Area/Density/Sliver Check
  - Length/Perimeter/Redundant Via/Resistance Calc.
  - Cell/Component/Block/IP, and Pins (Ports)
  - Connectivity of Power, CLK, Signals -> electrical short
  - ECO check/compare – difference/no-difference
  - X-talk, Parallel lines, Symmetry properties, etc.

- **Check and debug of DRC/LVS results at a chip level and large nodes as Power line**

  As “layout debugger”

  - Quick look at entire error distribution at chip level
  - Check and what-if analysis of timing issues like critical path/CLK
  - Check large node as PWR line for EM restriction

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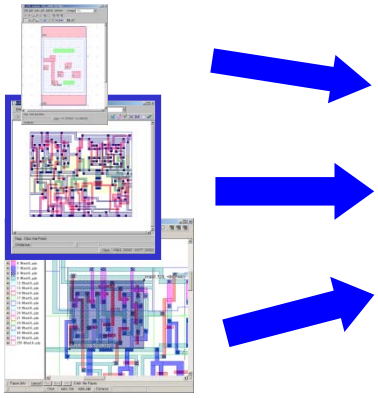
Incremental Checking to Improve the Quality

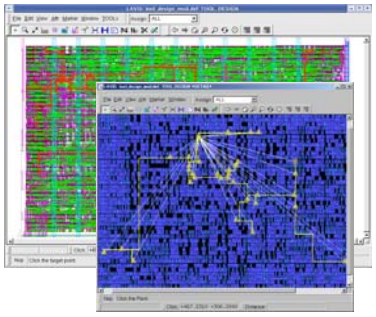
Enable to improve the Design Quality at individual designer level by Checking Incrementally at any design stage as Cell, Block/IP and a chip level whenever you want to avoid big issues at the last minute filling the gaps between automatic and nonautomatic checking flow

The total verification TAT is decided on by how to improve the quality at lower design levels

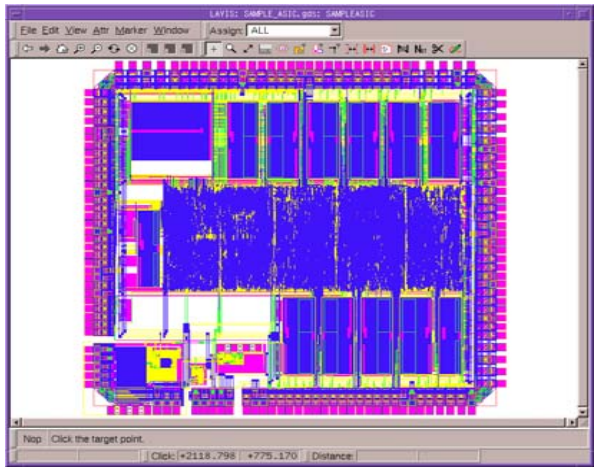
Final sign-off verification as DRC/LVS
No big fatal impact!



Cell level



Block/IP level



Chip level

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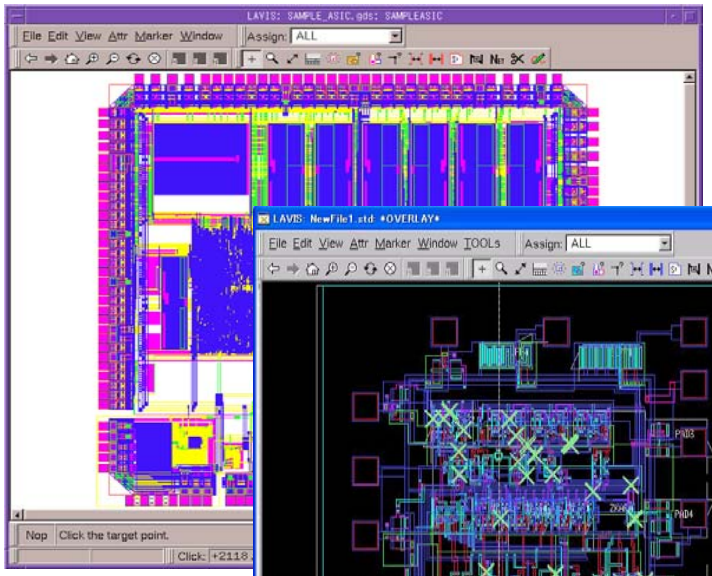
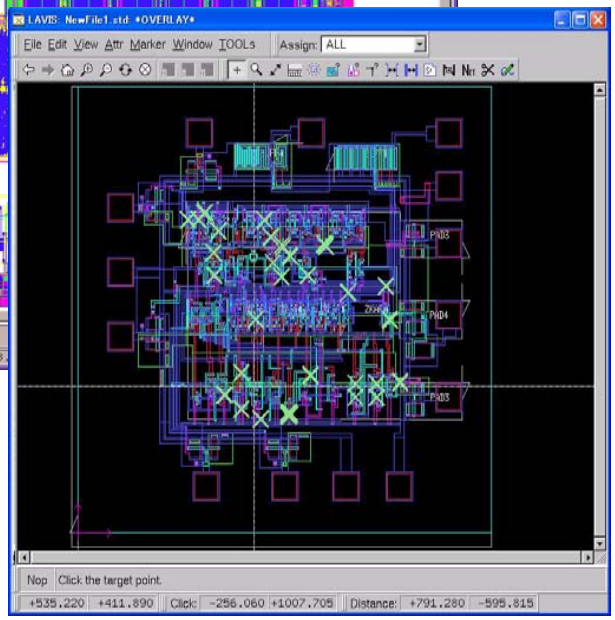
Layout Check at chip level

- Power/CLK/SCAN, DRC, TA -

Enable to check a layout at chip level with high performance for tracing huge nodes like Power, Clock, Scan clk, Busses, and error distribution, critical paths

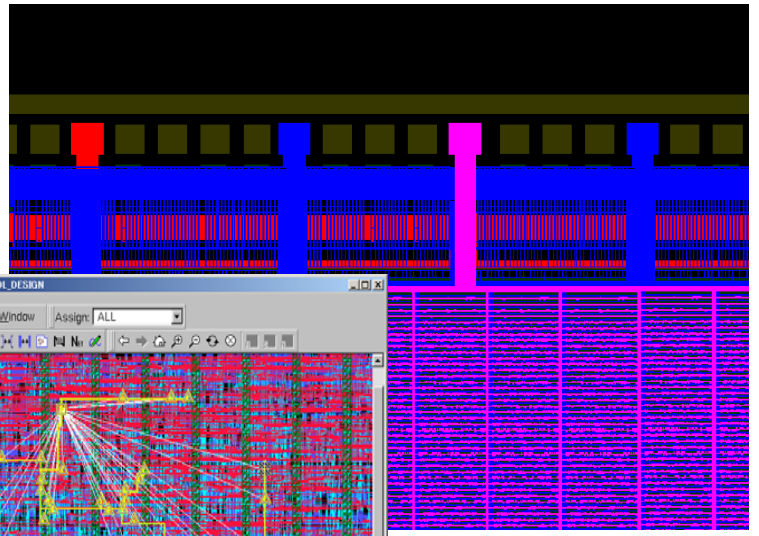


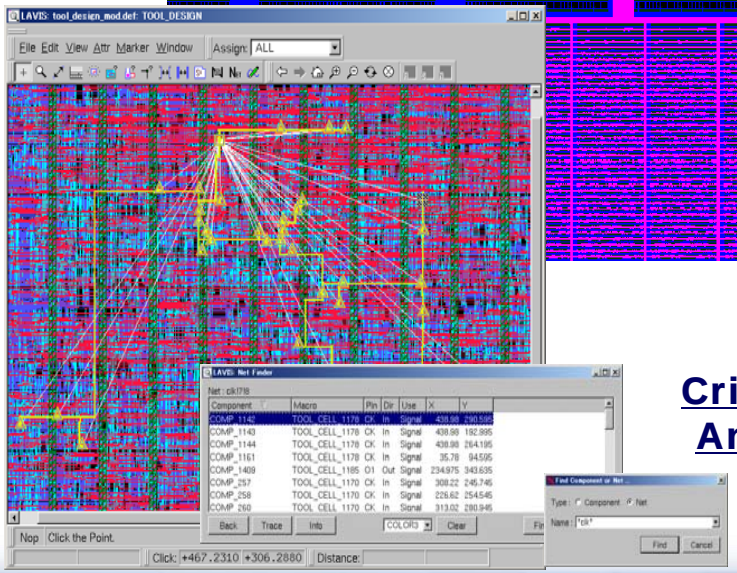
Chip level



Quick look at error distribution

power lines check





Critical path Analysis on Layout

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Simple Rule Checking

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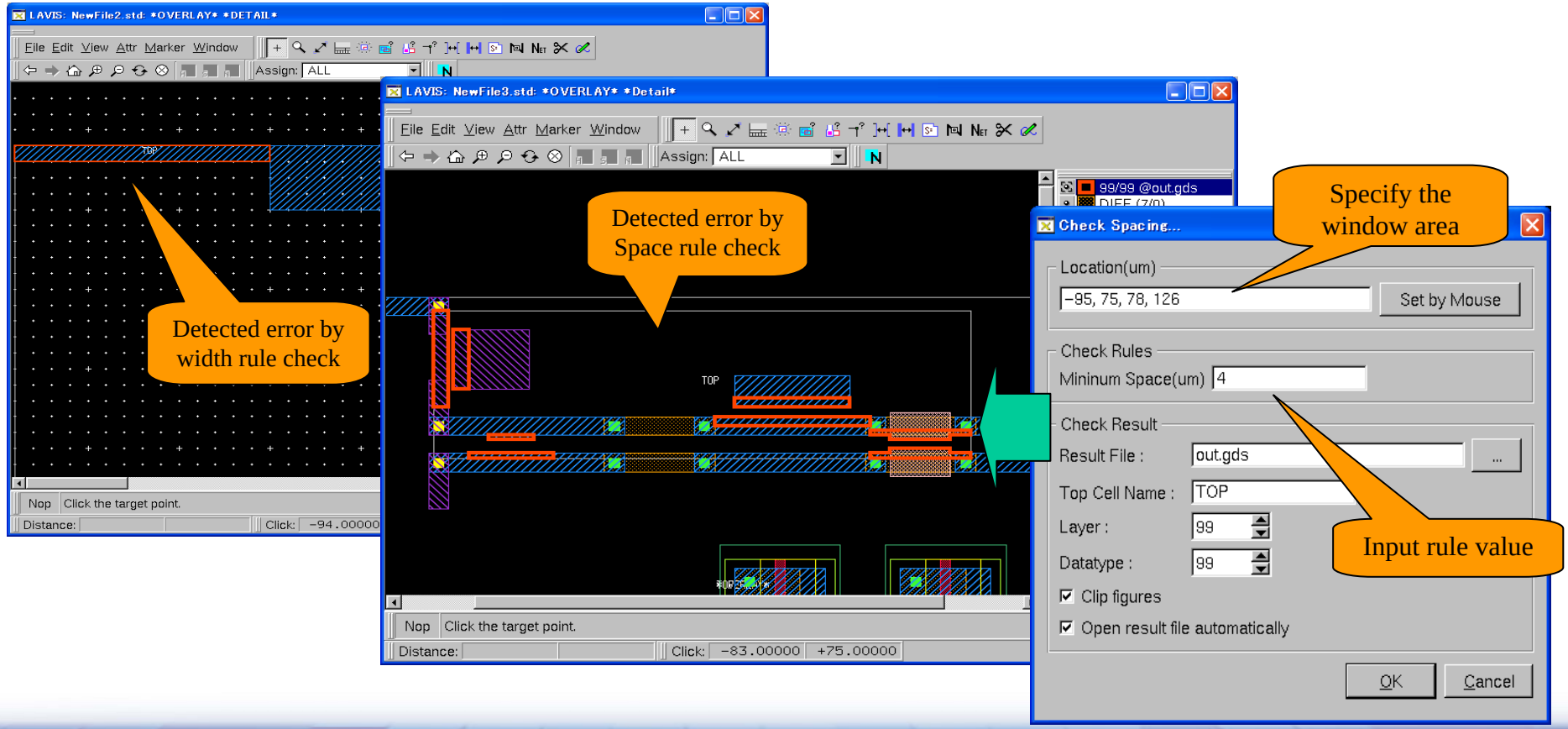
Area Specified Rule Check (1)

New Minimum Width/Space Check

> Minimum width/space check within the specified window area is available



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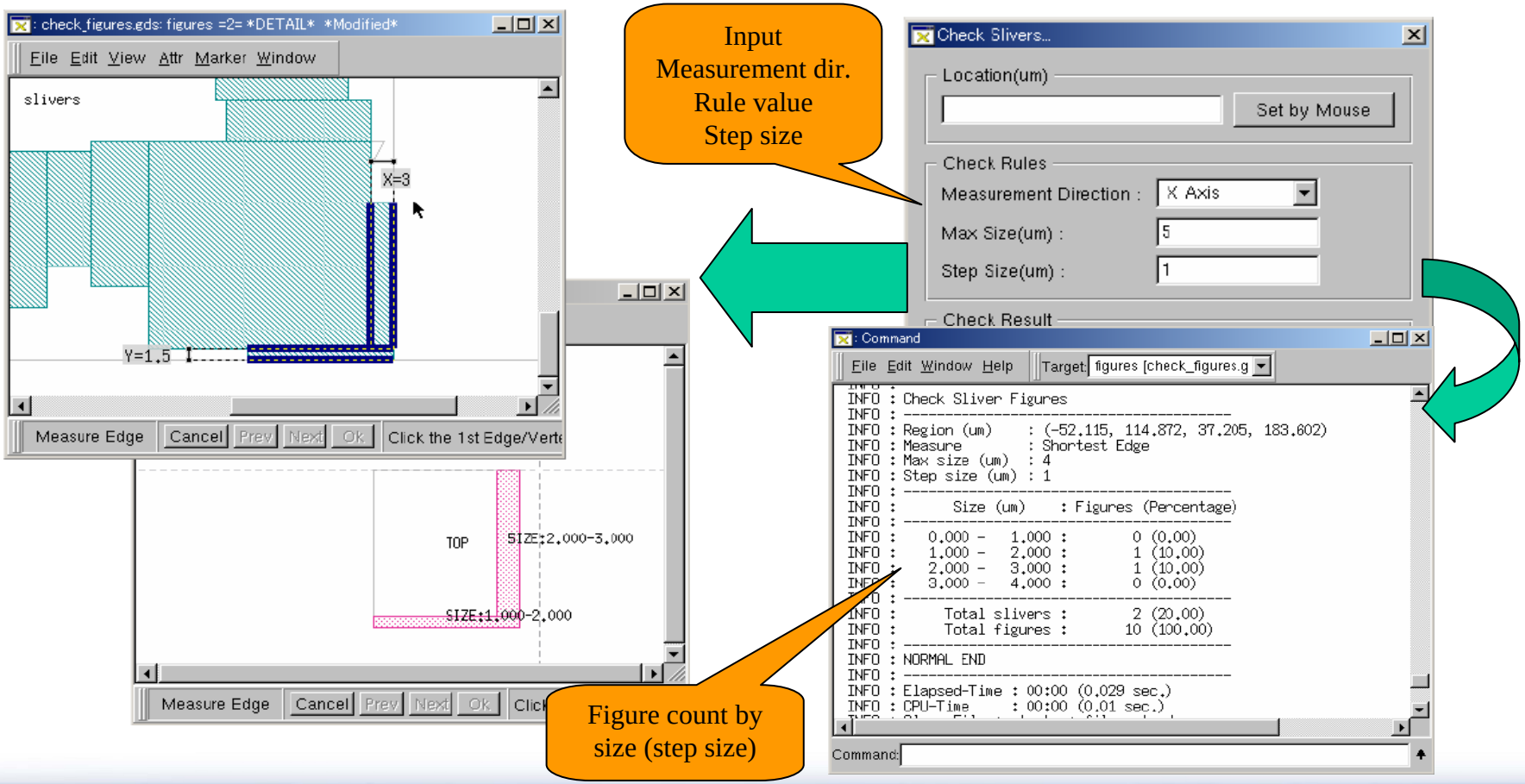
Area Specified Rule Check (2)

New Sliver Check

> Sliver check within the specified window area is available



Area Specified Rule Check (3)

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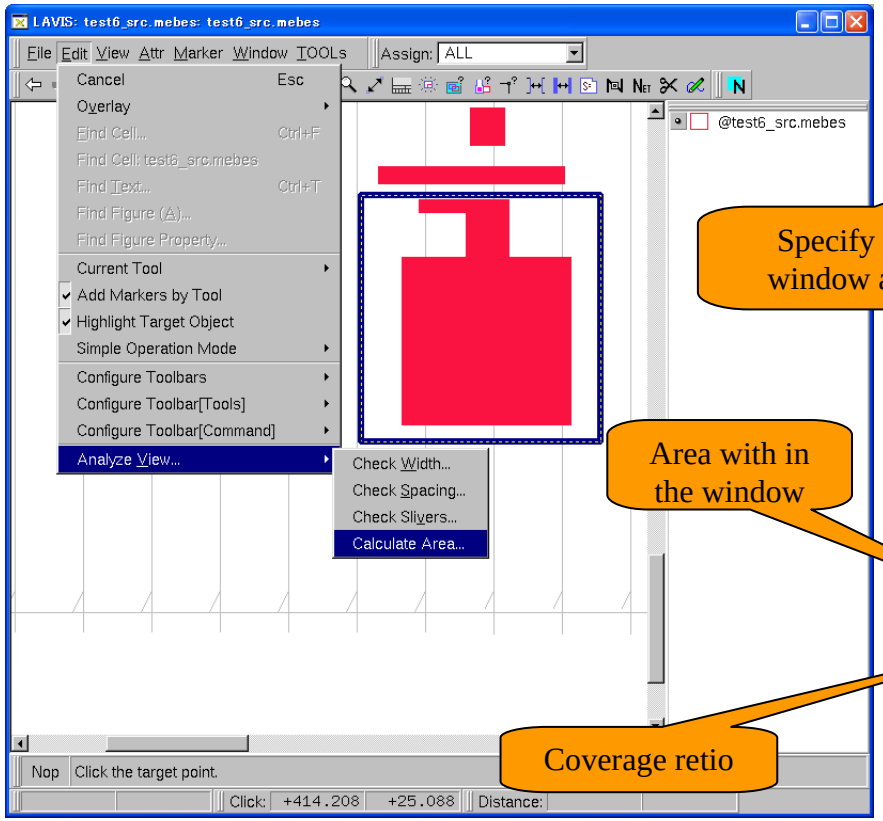
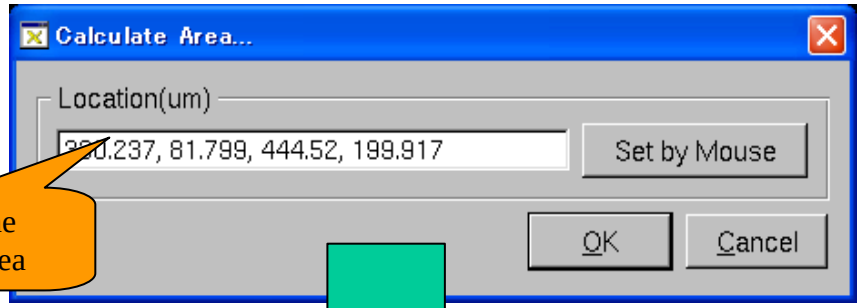
New Area Calculation within the specified window

> Enable to calculate Area / Coverage within the specified window area

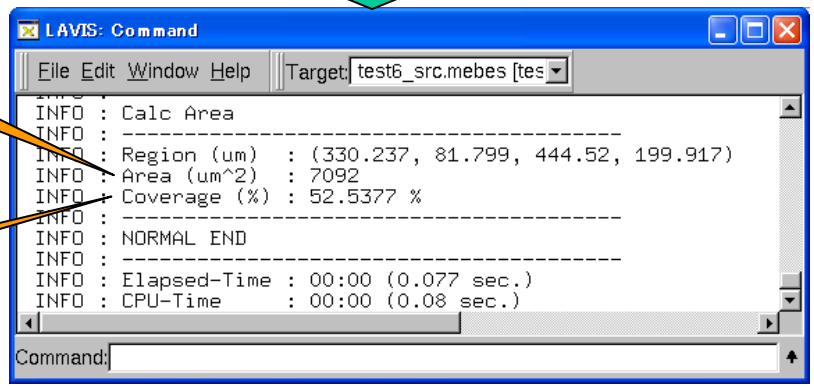




Specify the window area

Area with in the window

Coverage retio



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Node Checking on GDS

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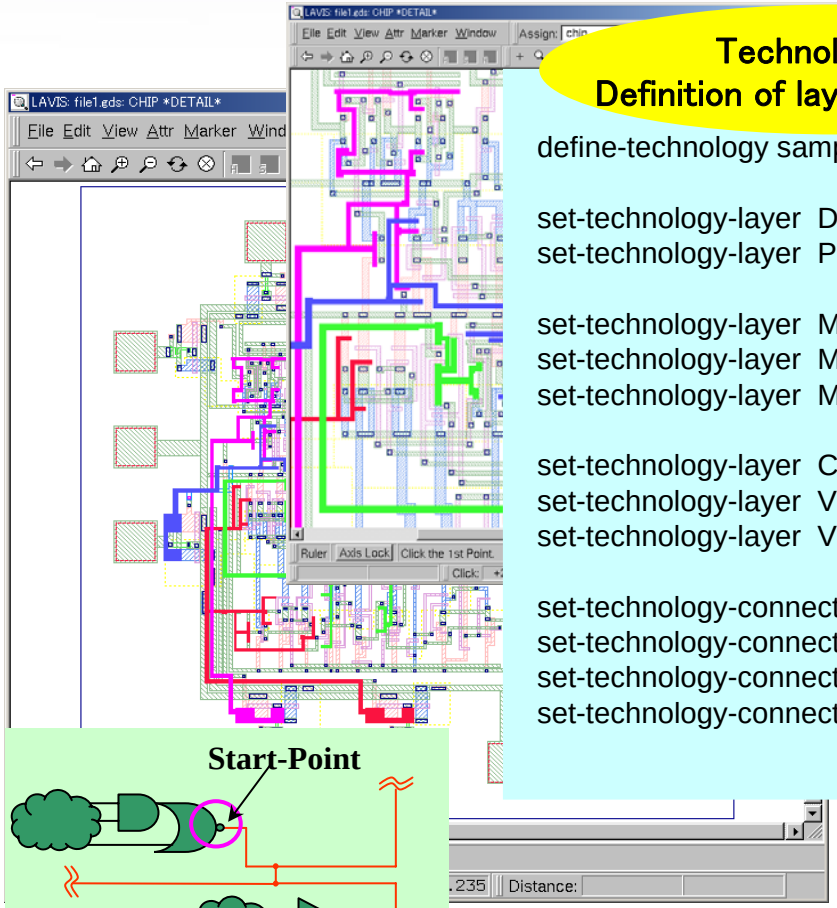
Tracing Node and Short

Easy to start node-trace analysis



Technology File
Definition of layer's connection

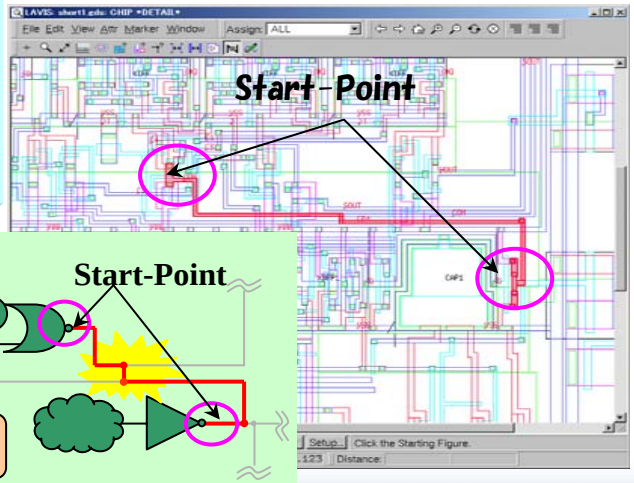
```
define-technology sample

set-technology-layer  Diff       DIFF   1
set-technology-layer  Poly       POLY   2,3

set-technology-layer  Metal1     WIRE   11
set-technology-layer  Metal2     WIRE   13
set-technology-layer  Metal3     WIRE   15

set-technology-layer  Contact    VIA     7
set-technology-layer  Via1       VIA    12
set-technology-layer  Via2       VIA    14

set-technology-connection  Diff    Contact Metal1
set-technology-connection  Poly    Contact Metal1
set-technology-connection  Metal1 Via1     Metal2
set-technology-connection  Metal2 Via2     Metal3
```

Short Trace

- **Only GDS is needed**
- **Simple Tech. File**
- **Trace & Highlight of the same nodes**
- **Trace the shortest connection of 2 points**
- **Detect a location of electrical short.**

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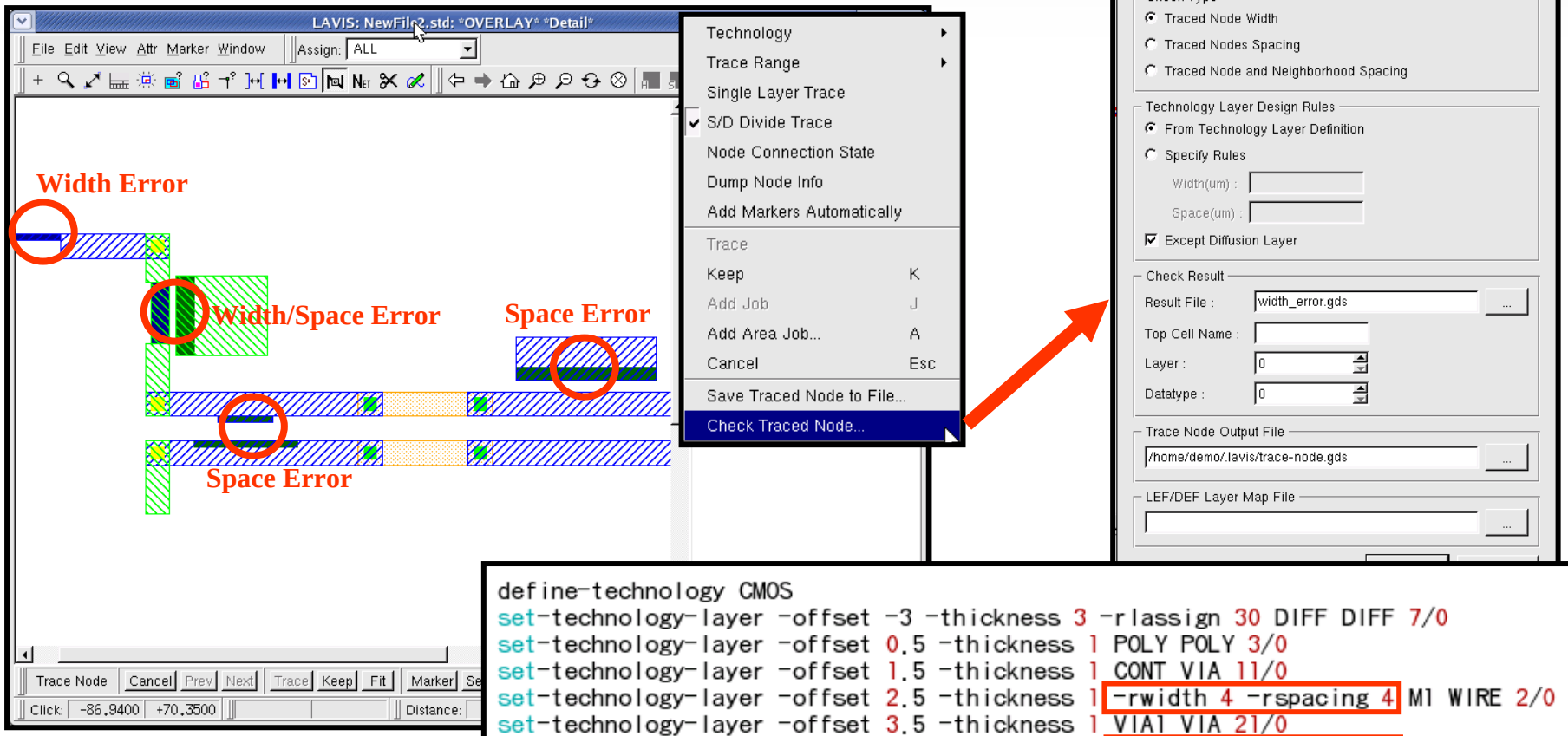
Intelligent Node-Trace (1)

-- X-Talk checking --

■Simple rule check for nearby figures to the traced node




```
define-technology CMOS
set-technology-layer -offset -3 -thickness 3 -rlassign 30 DIFF DIFF 7/0
set-technology-layer -offset 0.5 -thickness 1 POLY POLY 3/0
set-technology-layer -offset 1.5 -thickness 1 CONT VIA 11/0
set-technology-layer -offset 2.5 -thickness 1 -rwidth 4 -rspacing 4 M1 WIRE 2/0
set-technology-layer -offset 3.5 -thickness 1 VIA1 VIA 21/0
set-technology-layer -offset 4.5 -thickness 1 -rwidth 4 -rspacing 4 M2 WIRE 22/0
set-technology-connection DIFF CONT M1
set-technology-connection POLY CONT M1
set-technology-connection M1 VIA1 M2
```

[Technology Definitions]

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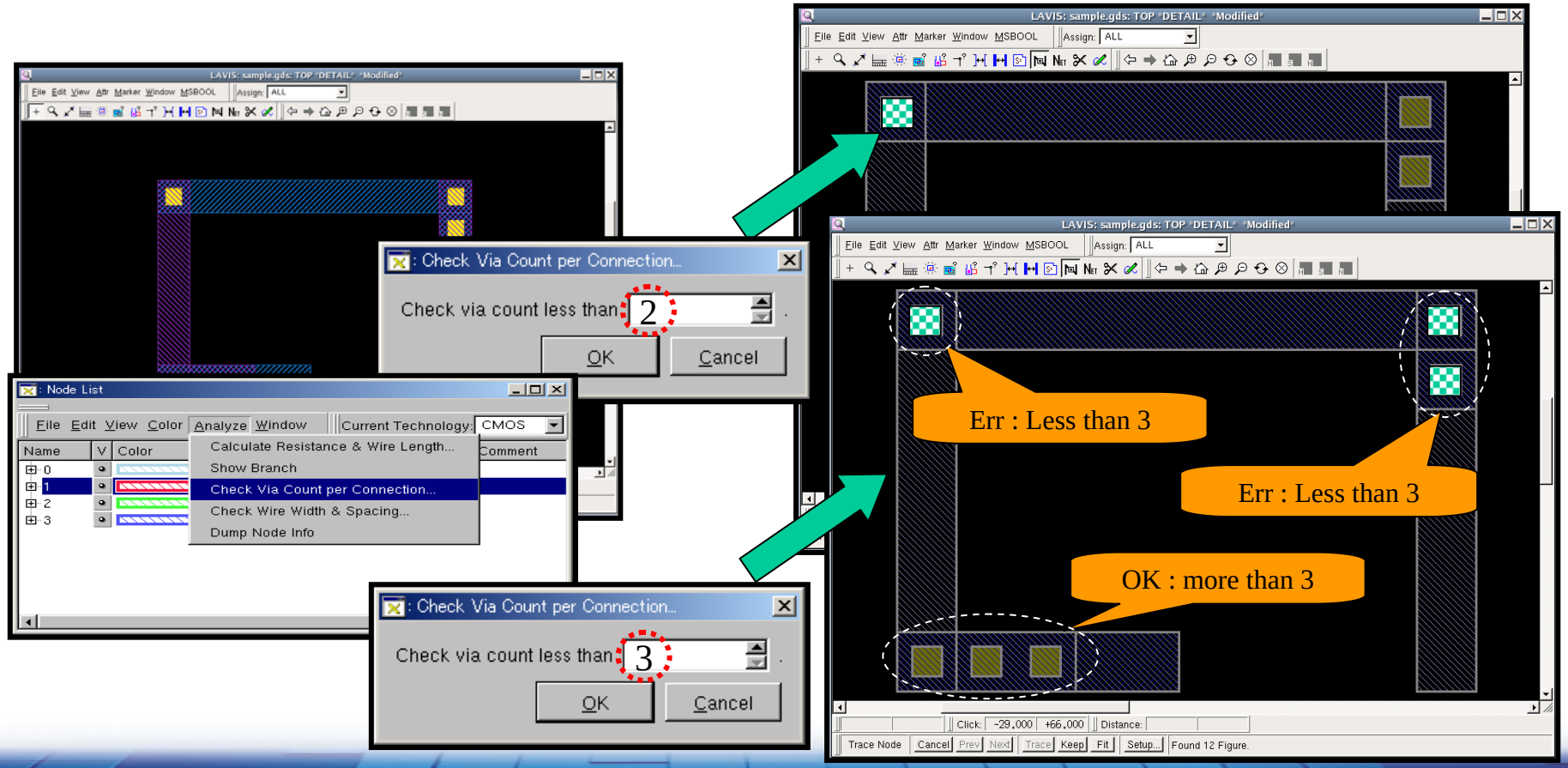
Intelligent Node-Trace (2)

-- Redundant Via Check --

Node–Trace Additional Function (3)

=>Redundant Via rule check:
Check Via Count per Connections



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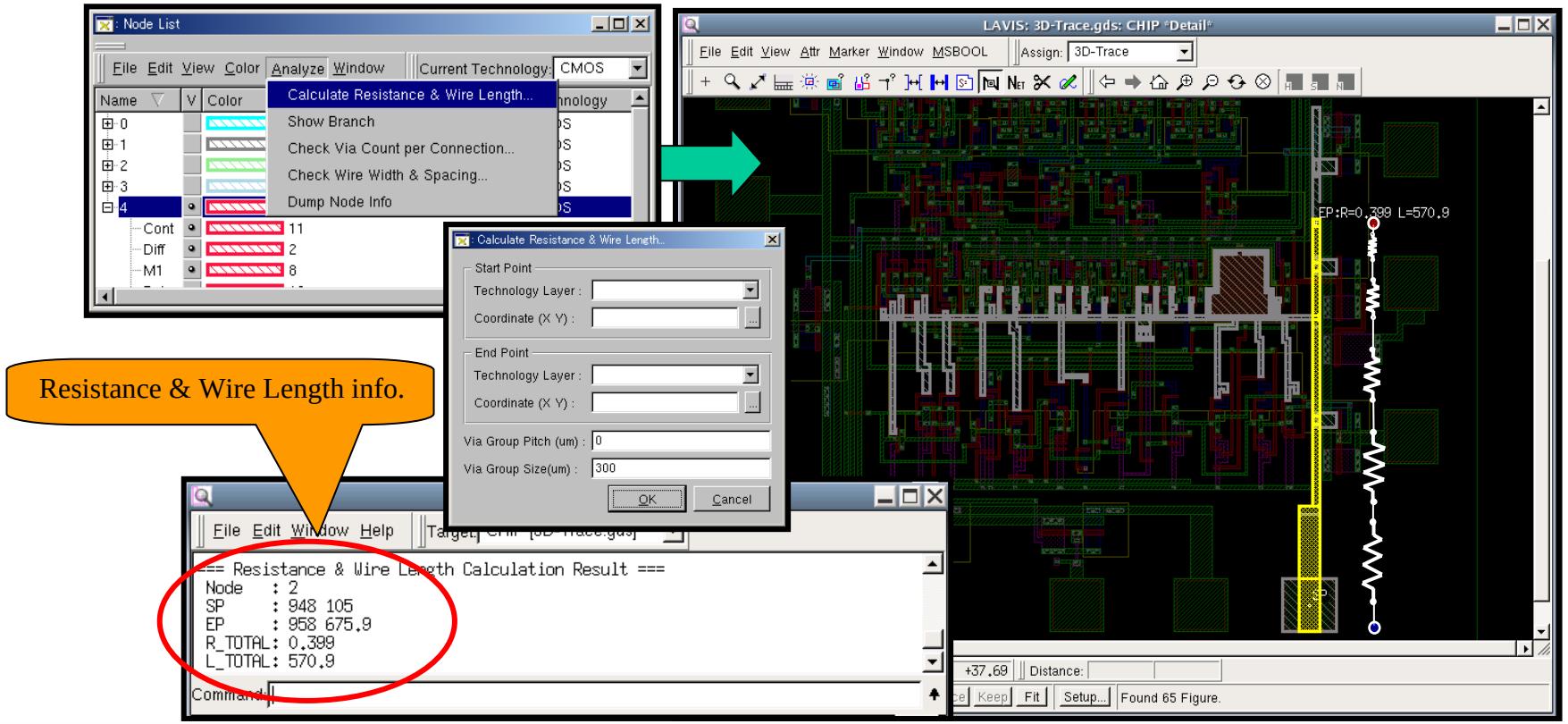
Intelligent Node-Trace (3)

-- Resistance & Wire Length info --

Node–Trace Additional Function

=> Resistance and Wire Length can be calculated and displayed



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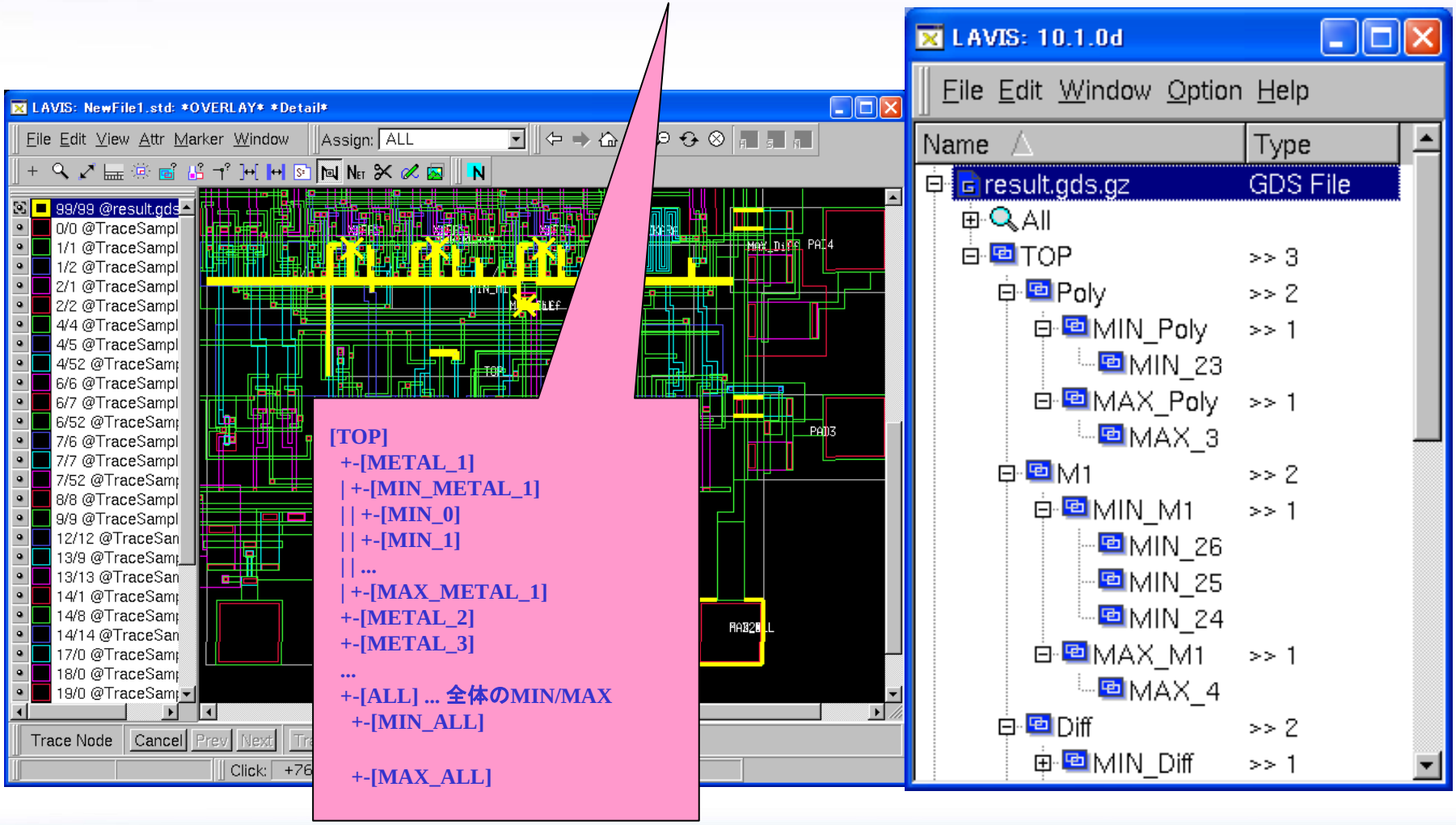
MinMax Wire Width by each tech. layer

=> Display Min/Max by each technology layer



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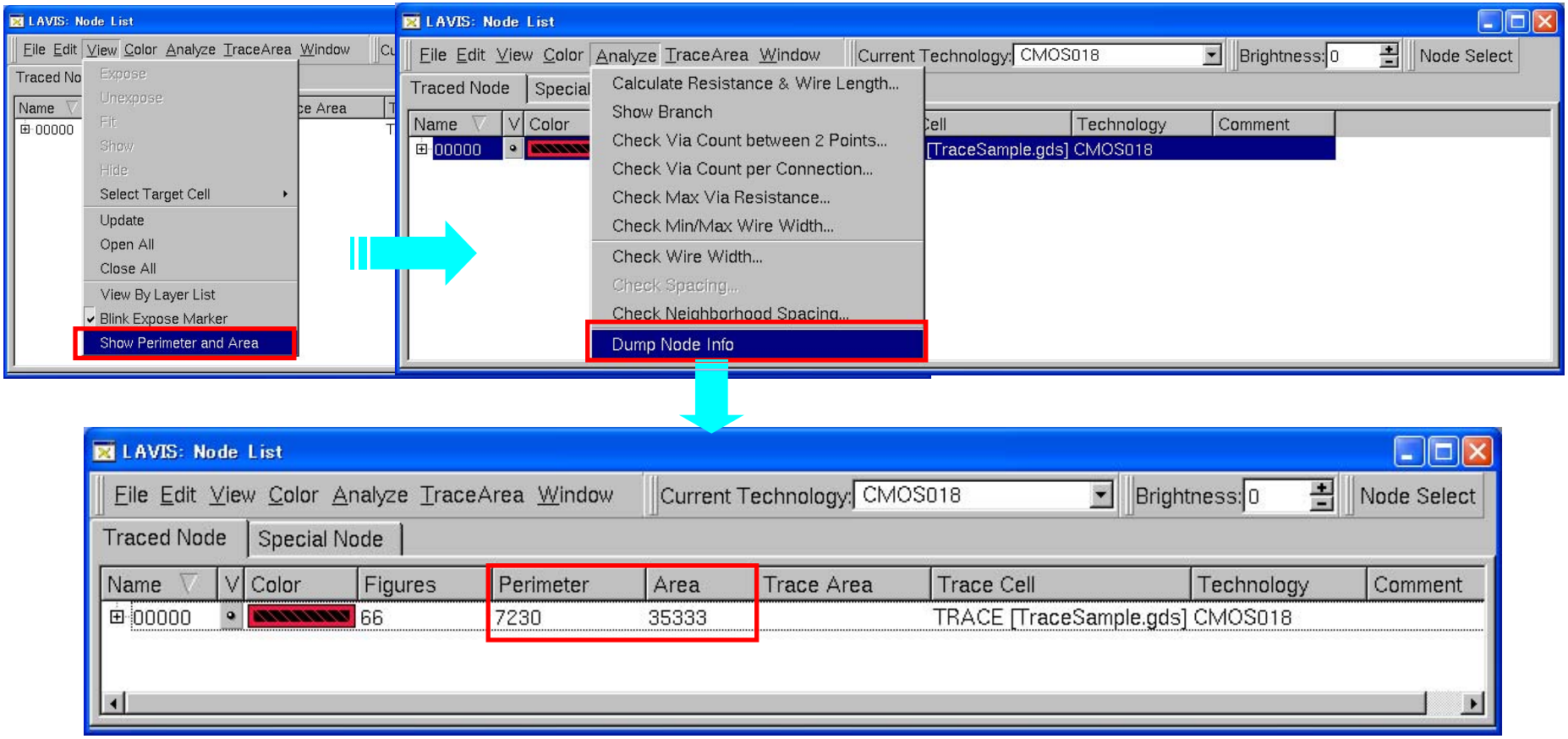
Area and perimeter of Traced Node

=> Node List can display an area and a perimeter information of traced node



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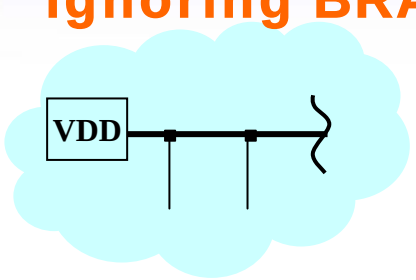
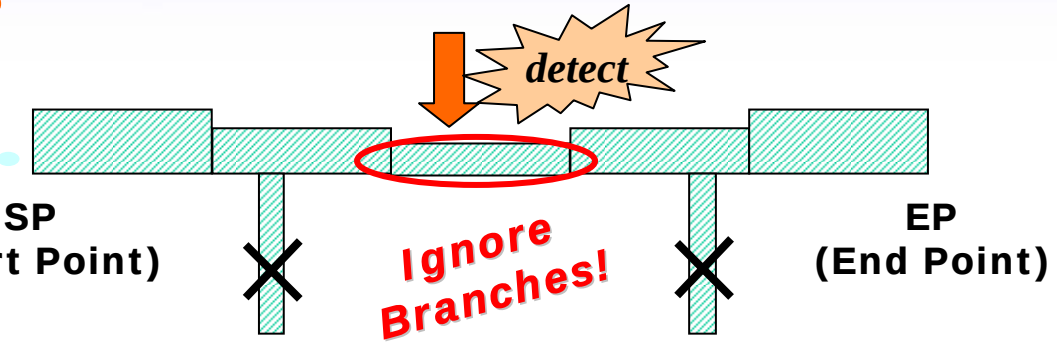
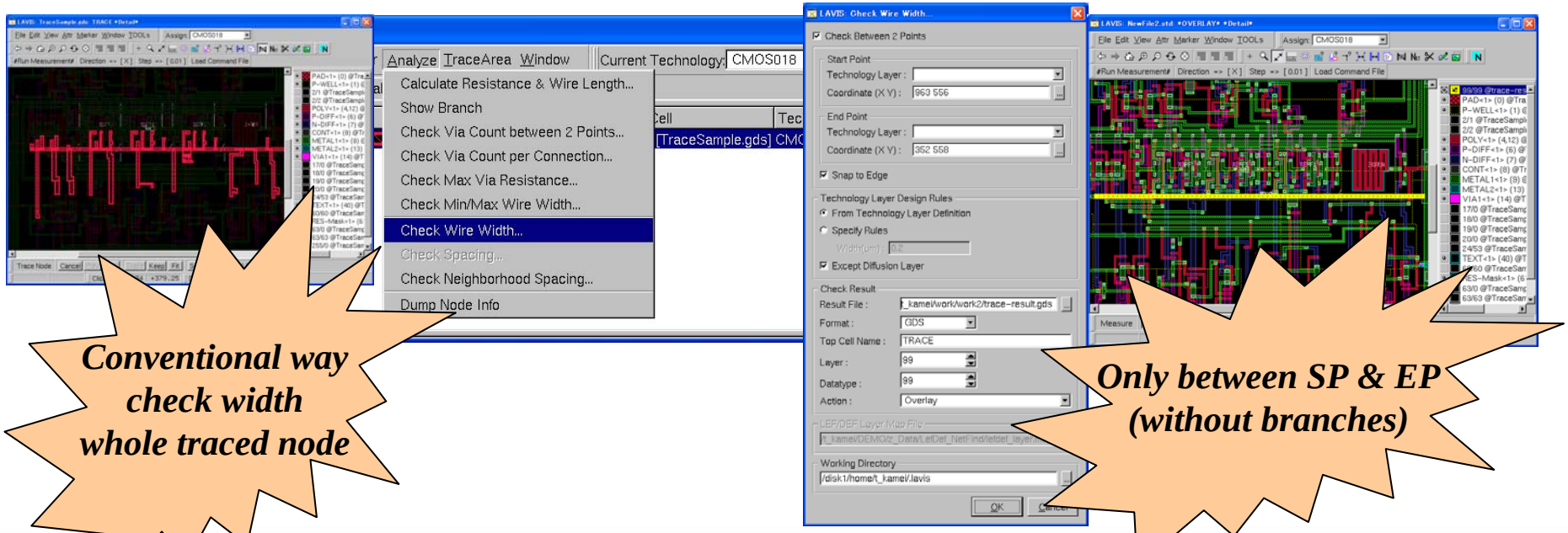
Check wire width between 2 points

- **Check Wire Width between the specified SP & EP points ignoring BRANCHES**







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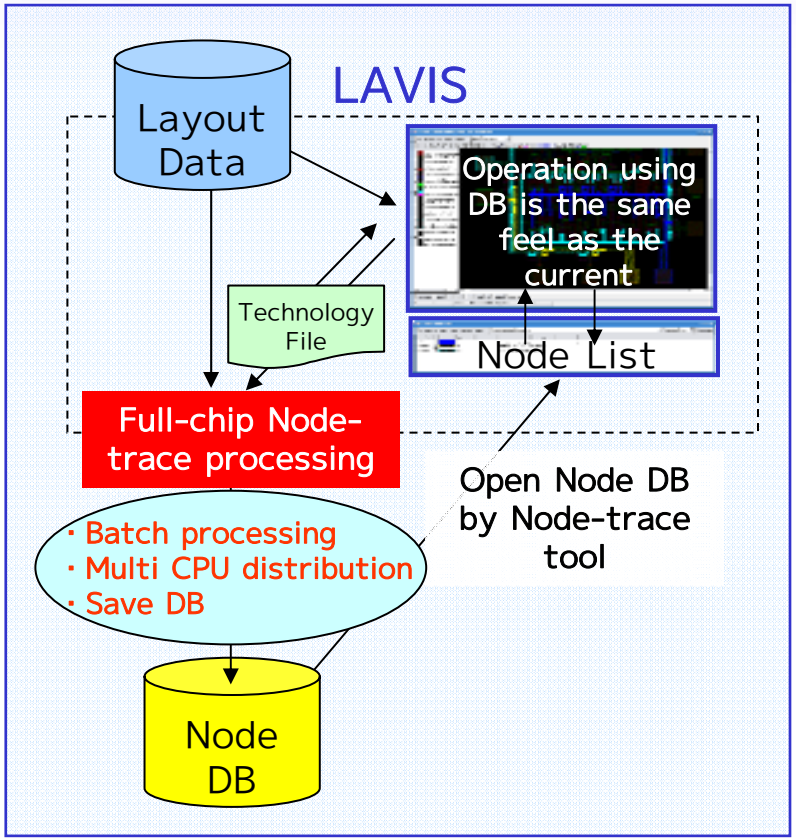
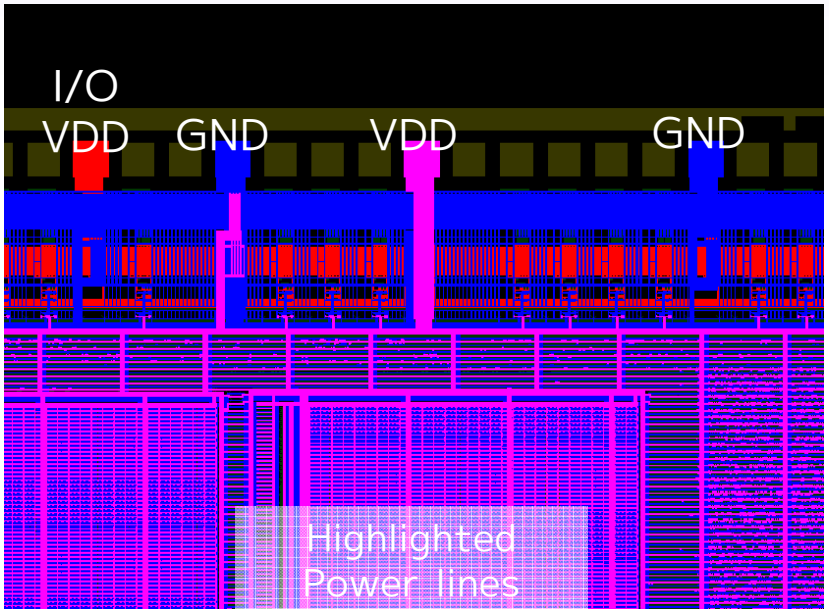
High performance node tracing
- Node Trace Data Base (NT-DB) -

■Batch process Node-trace flow



◇Batch process node-trace flow

All nodes extracted at chip level once are saved as a node DB



◇Case of power lines tracing

Enables to check easily wires of huge net with many figures, and multi power lines running at chip level using a node DB

10s~100s times faster than interactive mode!

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Layout Comparing Check

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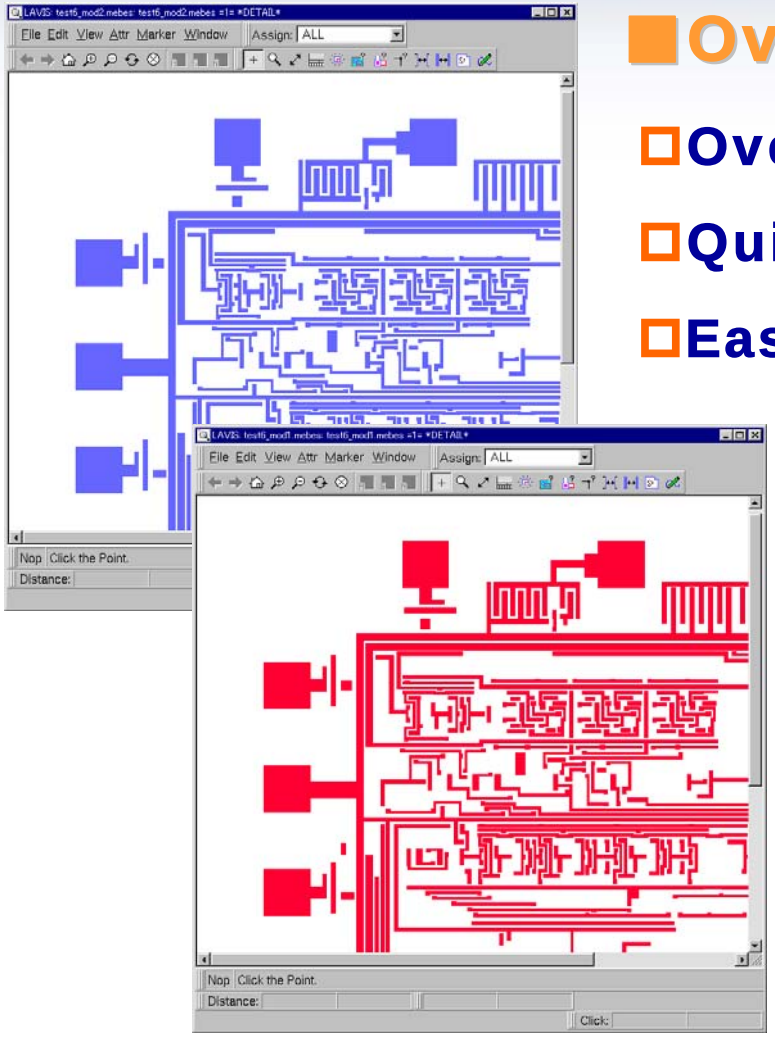
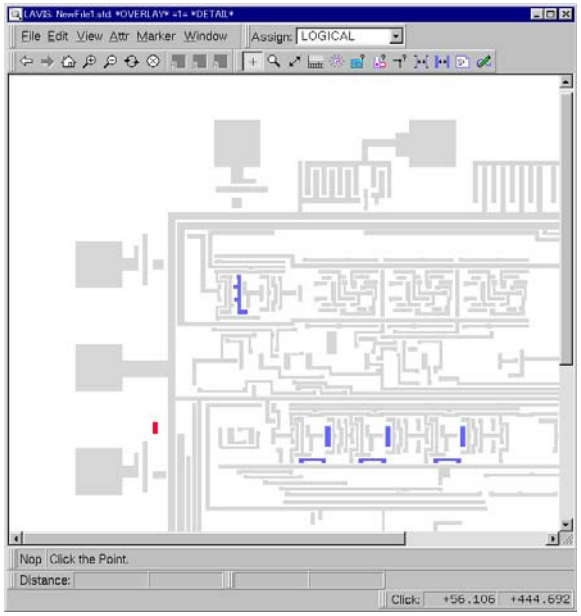
ECO Check & Compare



Overlay & Image Data Paste

- Overlay Display - GDS / LEFDEF / EBs
- Quick Comparison & Difference Check
- Easy to set - Scale / Origin / Rotation



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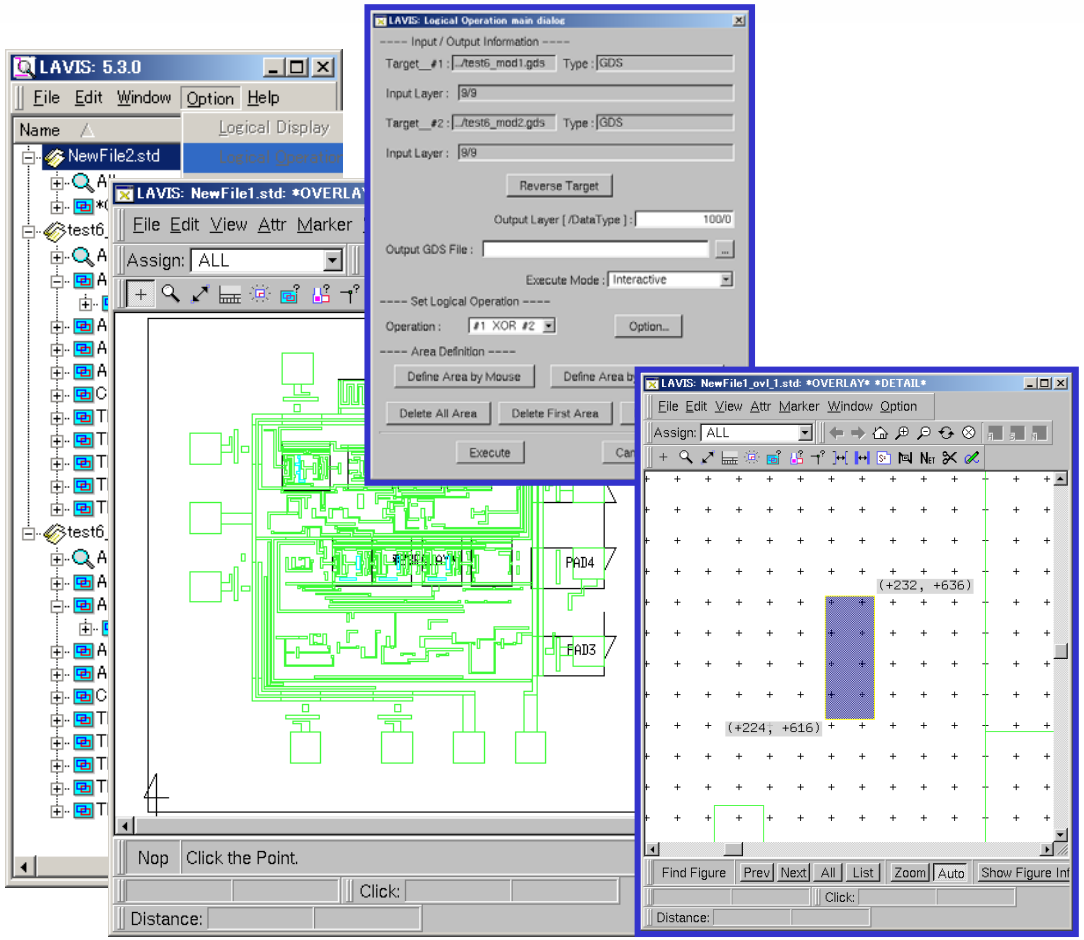
ECO Check & Compare (2)

Boolean Operation & Display



- **Boolean Operation of overlaid data**
  - XOR
  - AND
  - OR
  - SUB
- **Display the result in GDSII**
- **List up the results**
- **Enable to navigate all geometries by selecting the line in the checklist**

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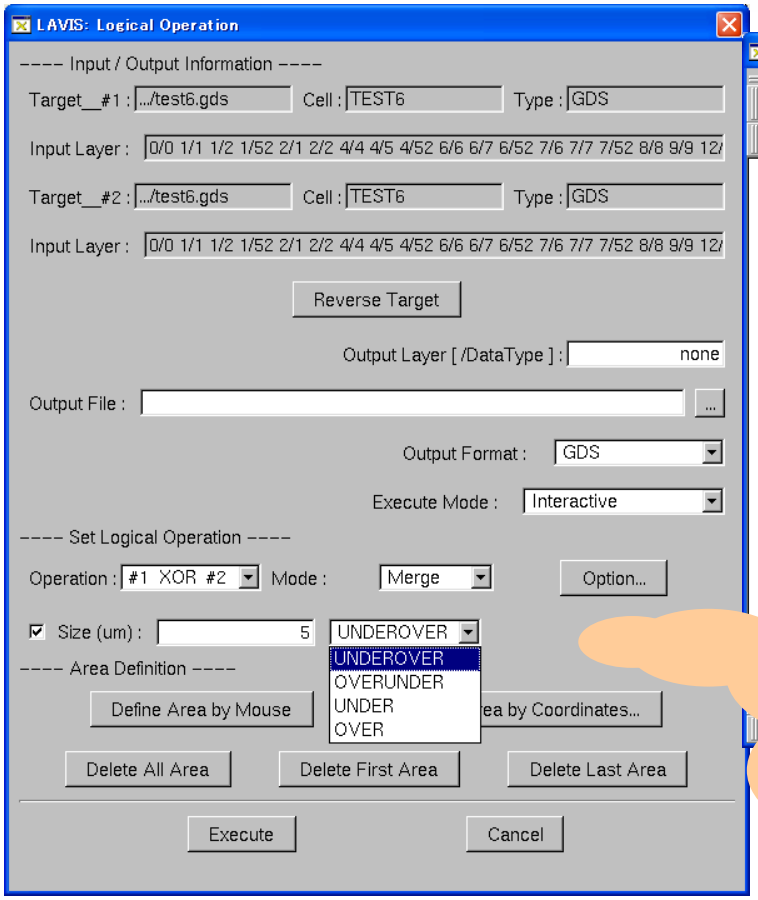
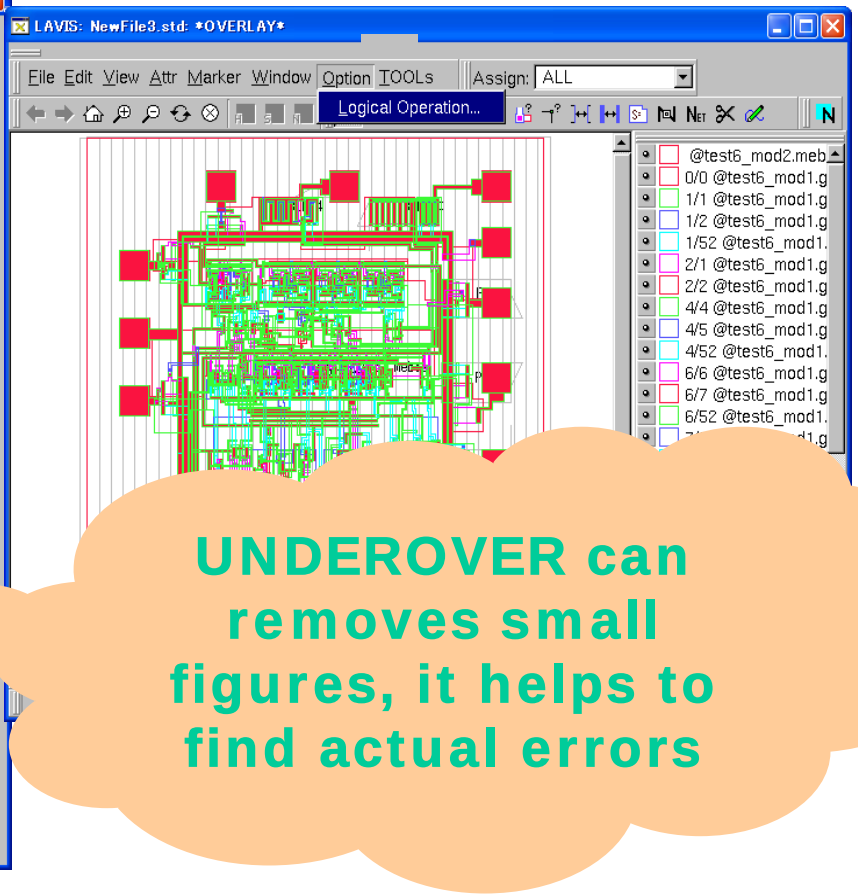
Logical Operation / lvlogic has Resize Function

=>LogicalOperation/lvlogic, resize(underover, etc) operation after boolean operation.





UNDEROVER can removes small figures, it helps to find actual errors

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I/F with Sign-off DRC/LVS Tools

Layout Verification Error Analysis and Layout Revision

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Layout Verification

Error DB

lverrdb2gds

GDSII
(error data only)

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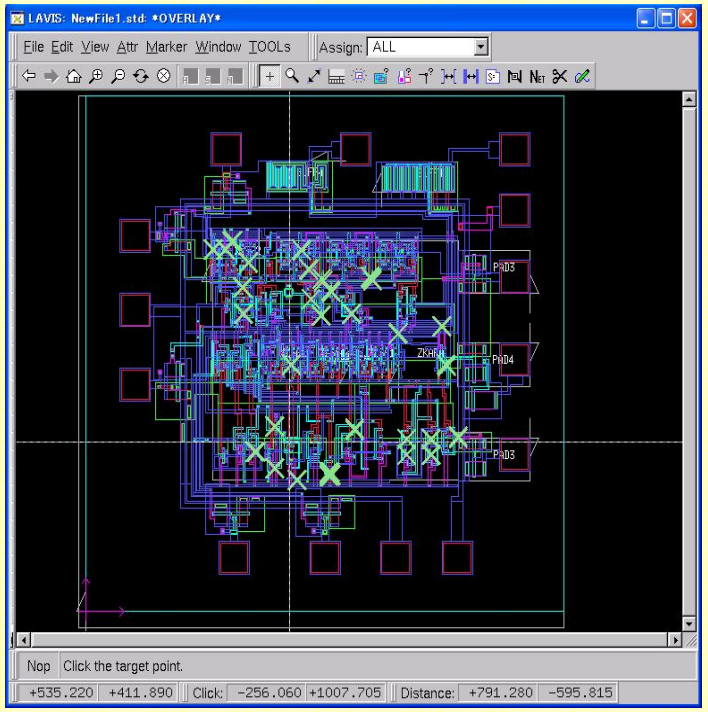
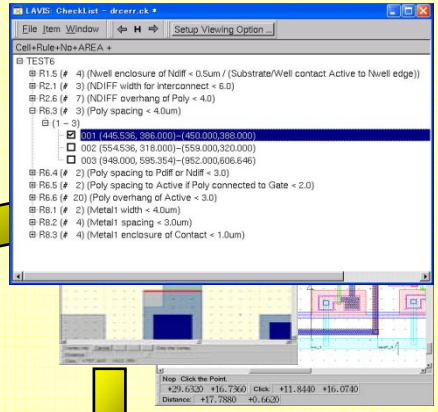
Quick look at entire error distribution



one-by-one review & revision

Check List



custom layout capable editor

Out of capacity

Simple Edit

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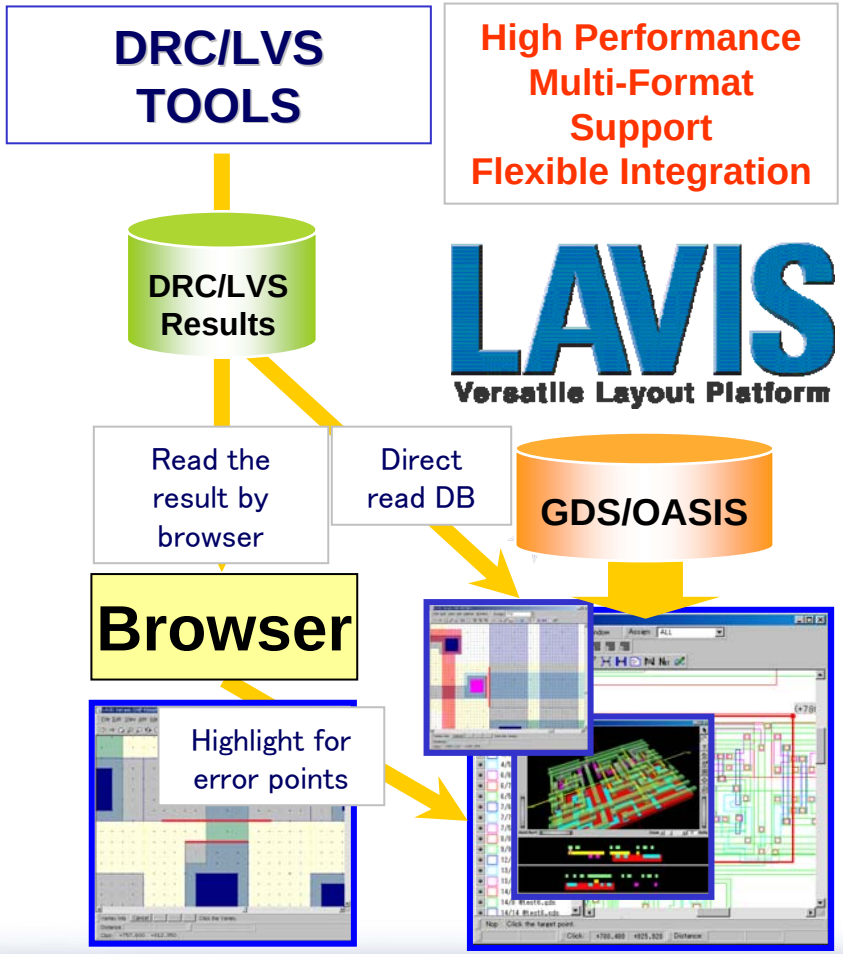
Assist for DRC/LVS analysis

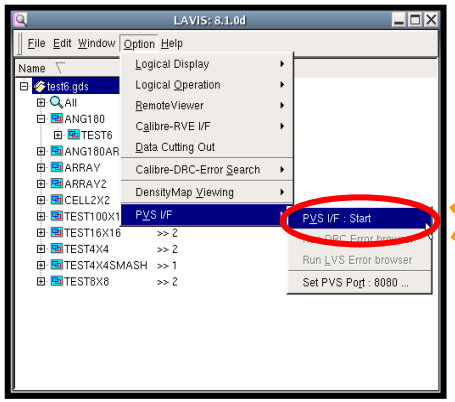
- I/F with 3rd party tools -

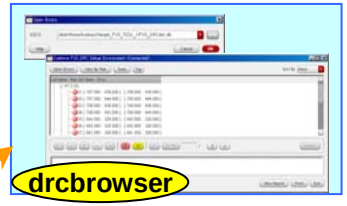
Interface with 3rd party tools

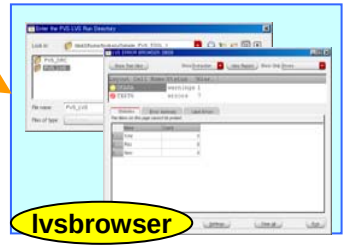


- Calibre-I/F of Mentor
- PVS-IF of Cadence

(ex) Cadence PVS-I/F







Benefit

⇨ **Easy and Flexible interface using Remote Viewing Environment**

⇨ **Direct read for DRC Error ASCII DB output by CalibreDRC**

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ECO & Hot fixing
On GDS/OASIS

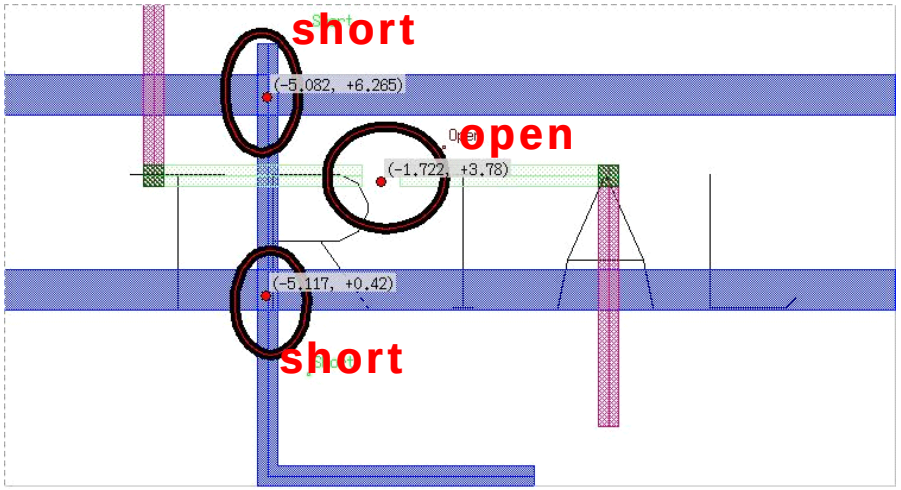
Simple Edit on GDS/OASIS

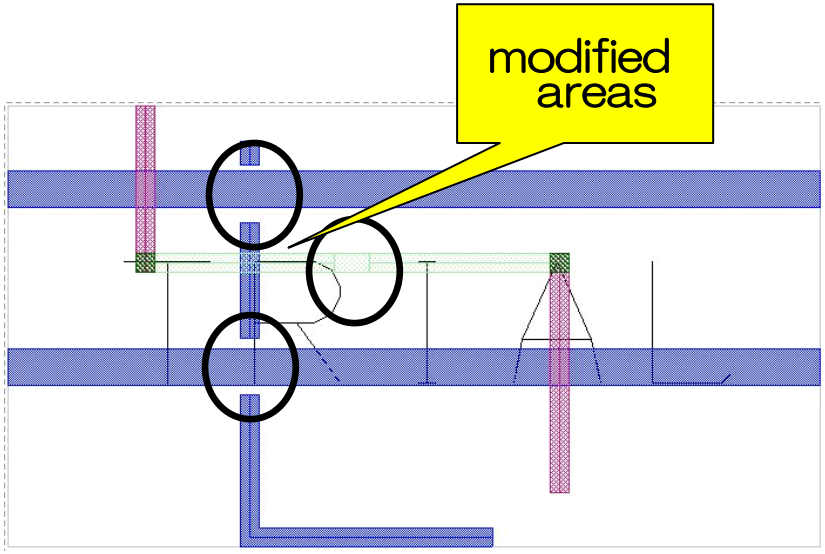
-- Assist for DRC/LVS analysis --

Hot Fix for Layout Verification

- Quick layout modification - add/delete/move text, elements & cell
- Create new GDS/OASIS data

For fixing a tiny bit of errors to get the short free data





⇨ *Fix the DRC/LVS errors in the early phase of design flow, feedback to the original data, and shorten the total verification TAT*

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GDS Simple Edit Functions

Items	Functions				
File Handling	Create File				
Cell Handling	Create Cell	Copy Cell	Delete Cell		
Figure, Cell Input	Input Boundary	Input PATH	Input TEXT	Input Cell (SREF)	Input Array Cell (AREF)
Figure, Cell Selection	Select Figure & Cell	Select Side of Figure	Select Vertex of Figure	Select Multi-Figure	
Selected Figure, Cell Editing	Move Selected Figure & Cell	Copy Selected Figure & Cell	Delete Selected Figure & Cell	Change Parameter of Selected BOUNDARY	Change Parameter of Selected PATH
	Change Parameter of Selected TEXT	Change Parameter of Selected Cell (SREF)	Change Parameter of Selected Array Cell (SREF)	Rotate Selected Figure & Cell	Mirror Selected Figure & Cell
	Add Sequential Figure	Divide Figure	Move Selected Figure & Side	Move Vertex of Selected Figure	Resize Figure
	Figure Logical Operation	Selected Figure & Cell Instantiation	Selected Array Cell Expansion	Selected Cell Expansion	Selected TEXT Expansion
Others	UNDO, REDO	Incorrect Figure Prohibition Mode	Resume Function for Abend	QUIT Editing Cell Information	QUIT All Editing Information

Available Not available

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LEF/DEF Interface

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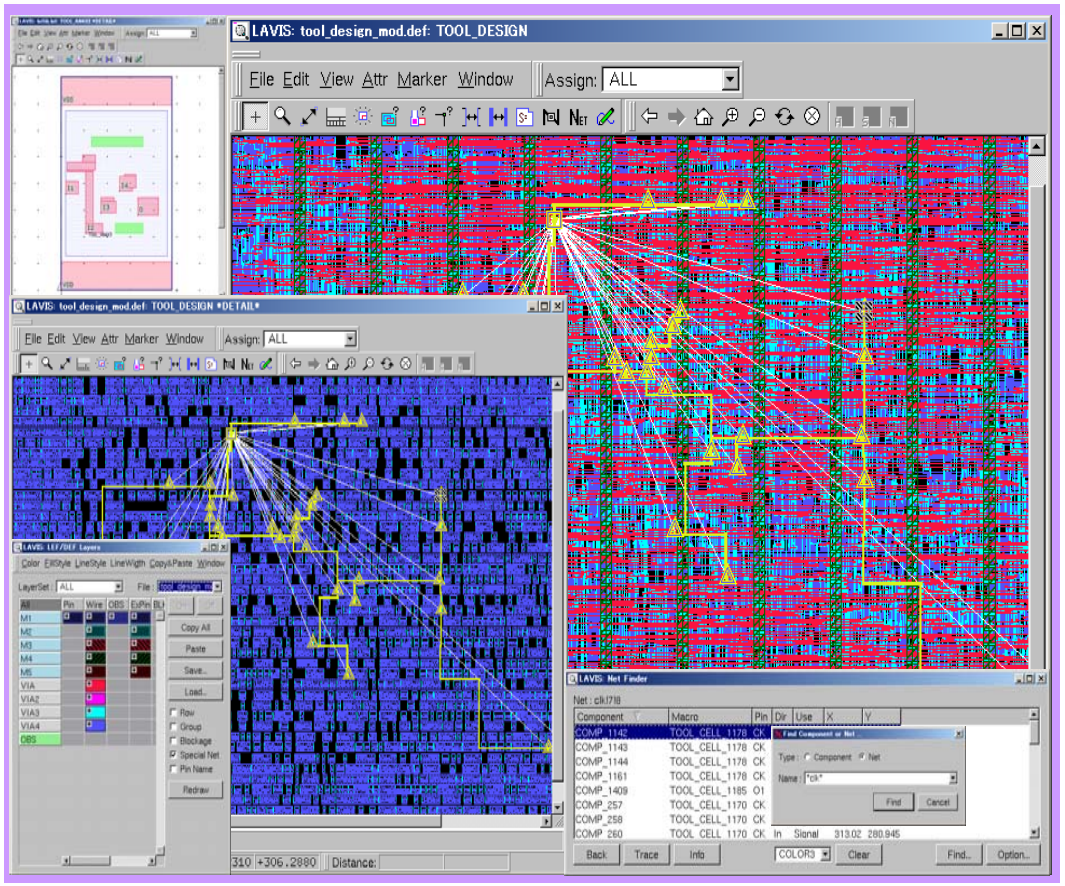
Pursuing wire connection and Critical / CLK Path

■ Trace net & component on LEF/DEF display



- ■ Trace / Find Net & Component
- ■ Visual Track / Check of CLK Tree
- ■ Visual Track / Check of Critical Path by TA
- ■ Scan Path check, etc.
- ■ Overlay LEF vs GDSII
  - ■ Check Cell / IP ports & Obstacles

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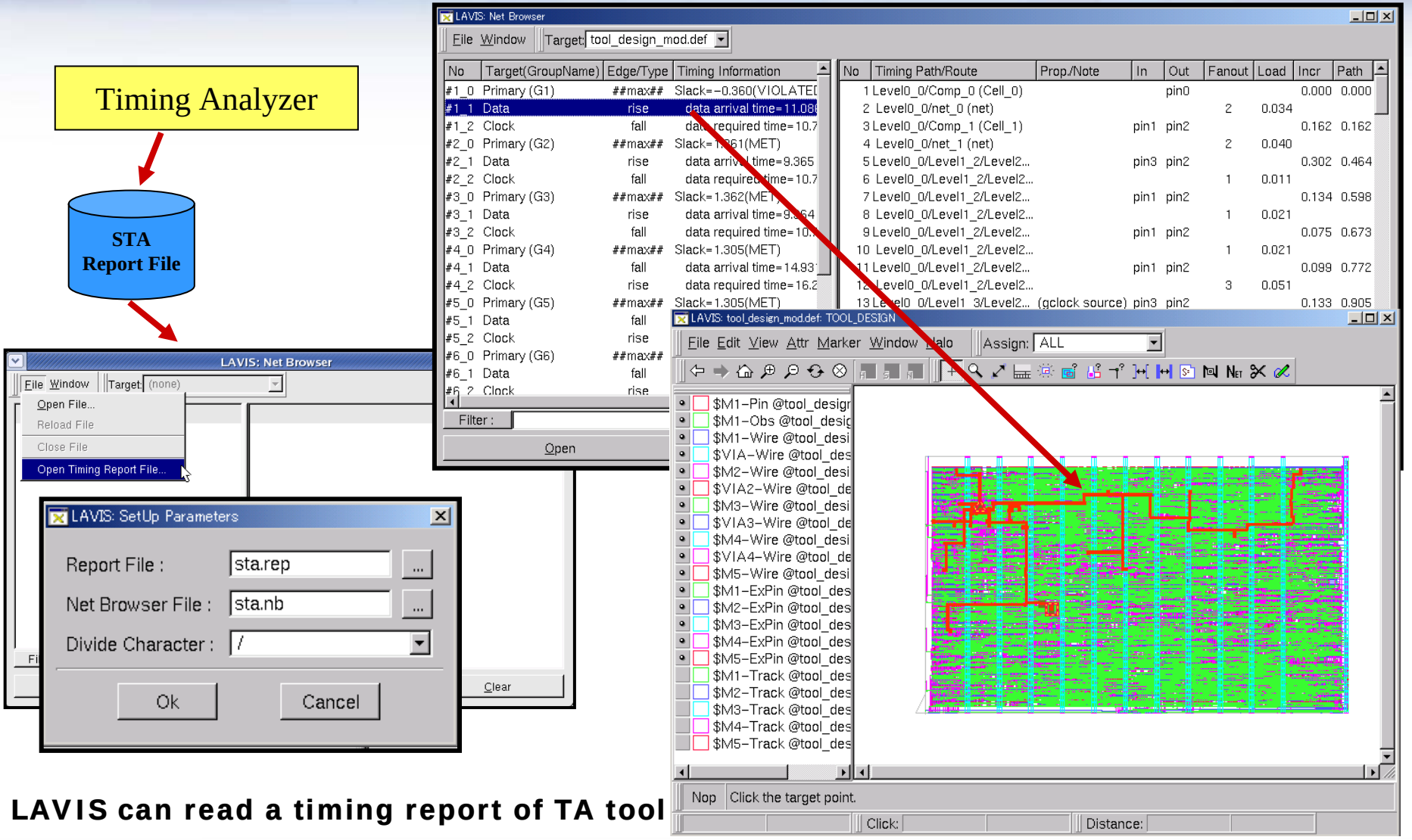
STA Critical Path Display

Timing Analyzer

STA Report File



LAVIS can read a timing report of TA tool

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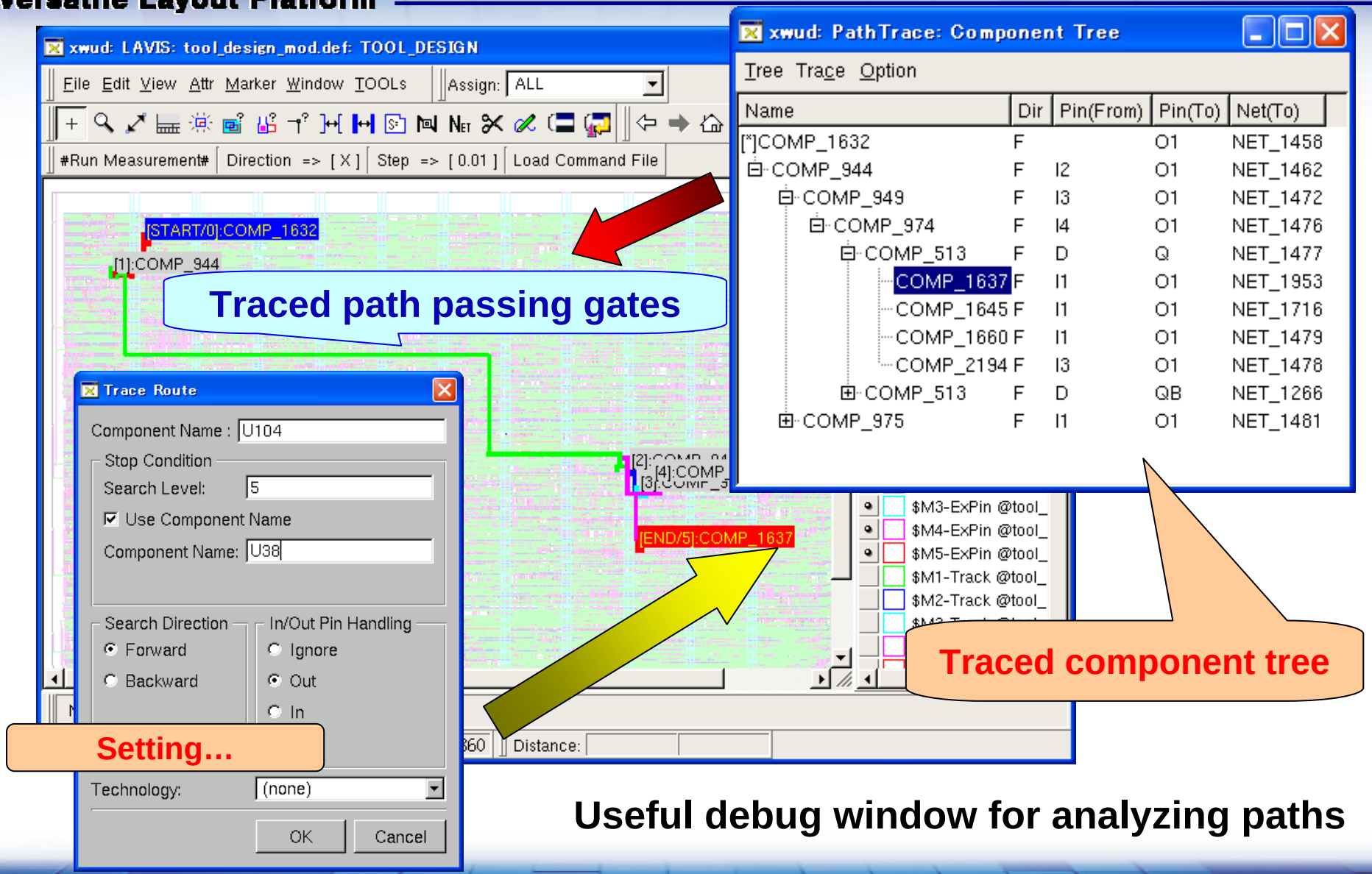
Gate-pass Route Trace
- LEFDEF I/F -



Useful debug window for analyzing paths

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Other Features

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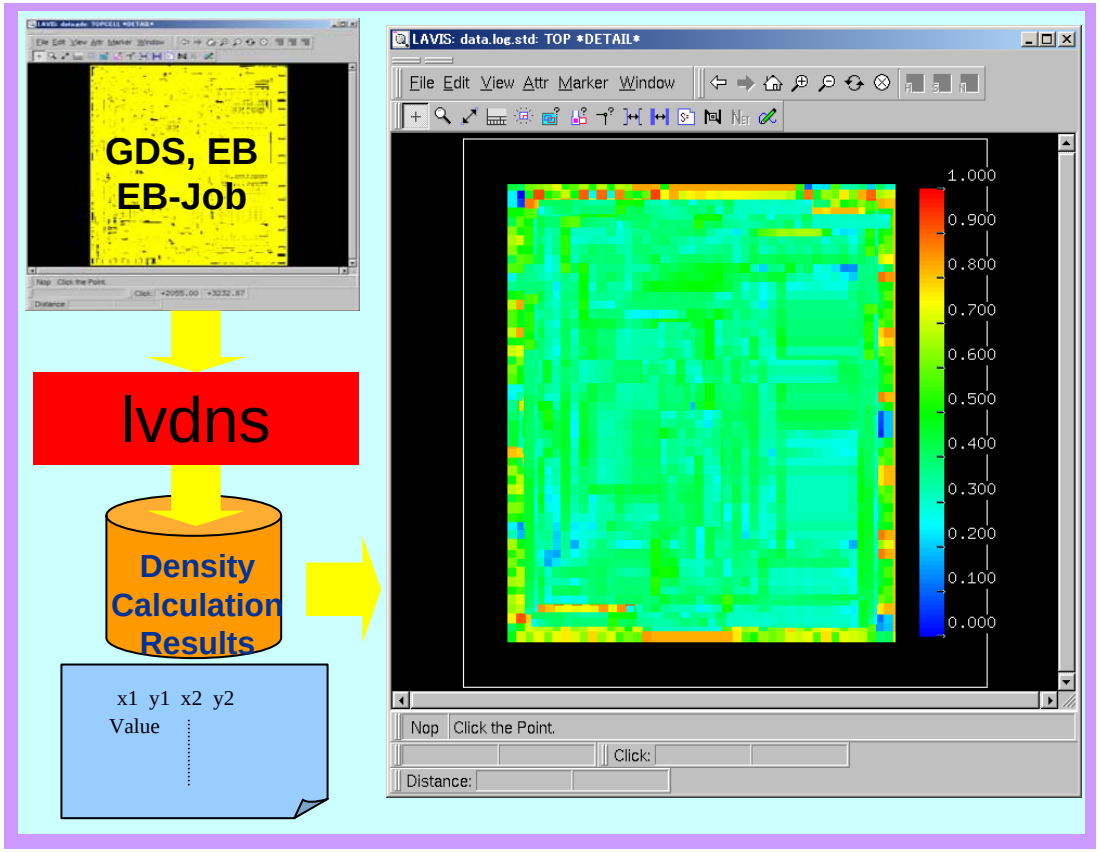
Density Calculation & Map Display!

- Displaying a color map for an analytical calculation result



- Geometry-based (Layout patterns) density calculation result
- Voltage drop calculation
- The density calculation utility is bundled in LAVIS

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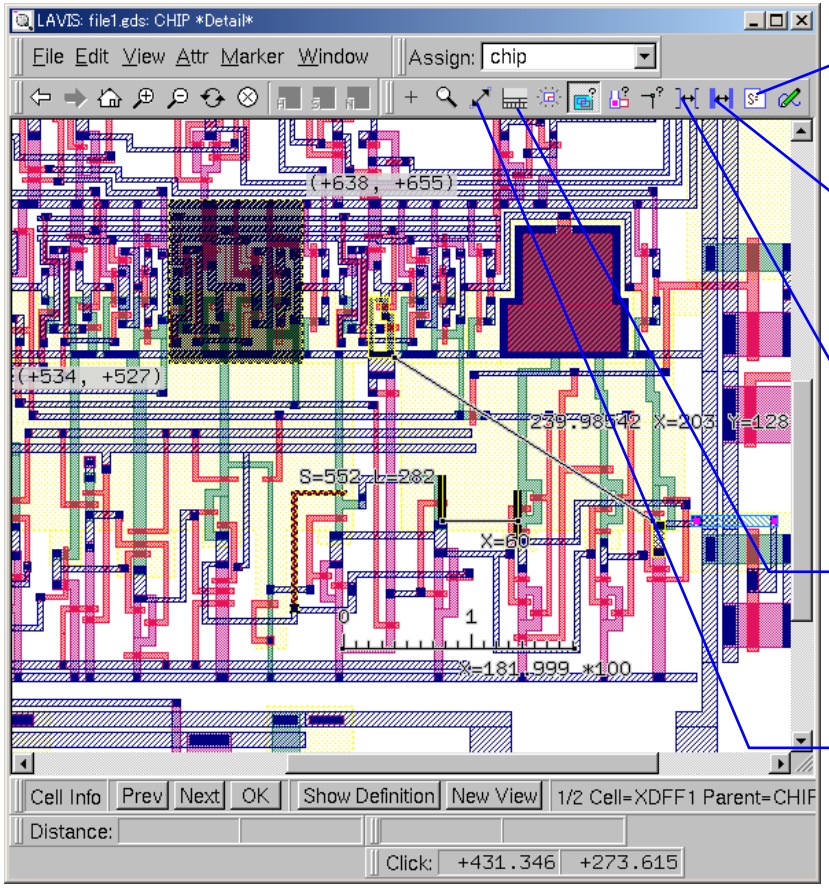
Measurement

Providing various types of measurement tools



Measure Area Tool
Area / Perimeter

Measure Figure Tool
2-figure interval

Measure Edge Tool
2-sided space / width

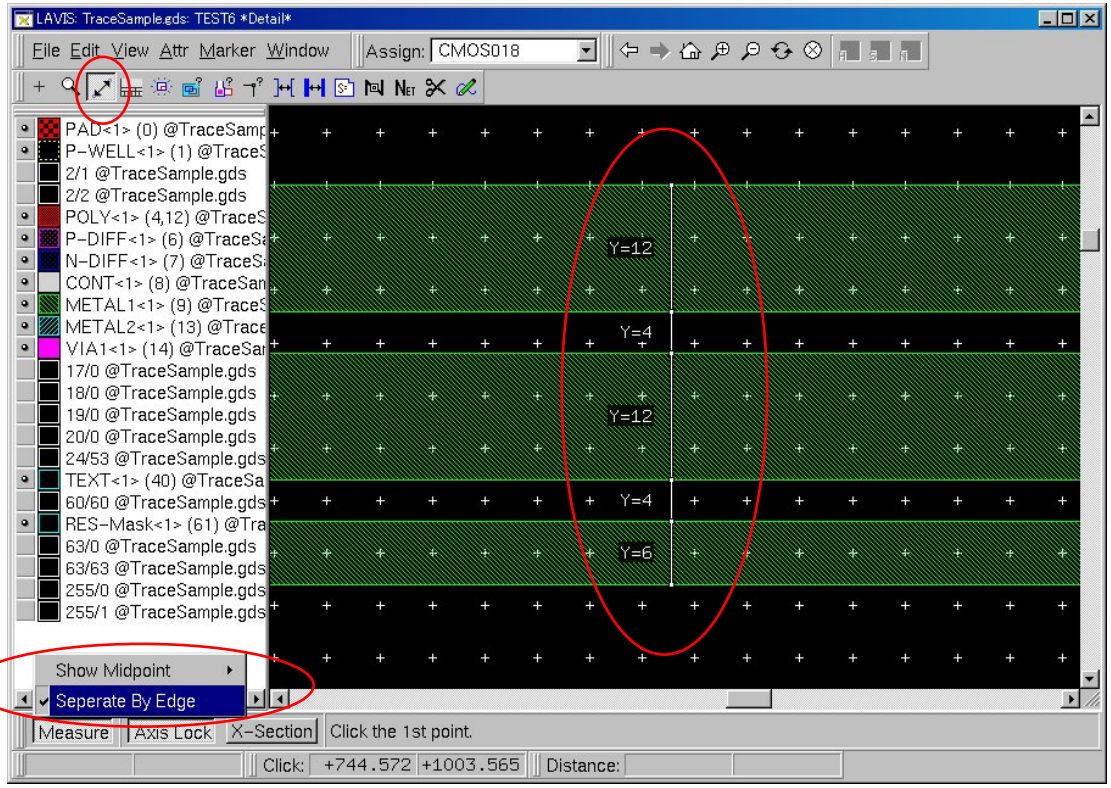
Ruler Tool (Scale)
2-point distance

Measure Tool
2-point distance

Line & Space measurement

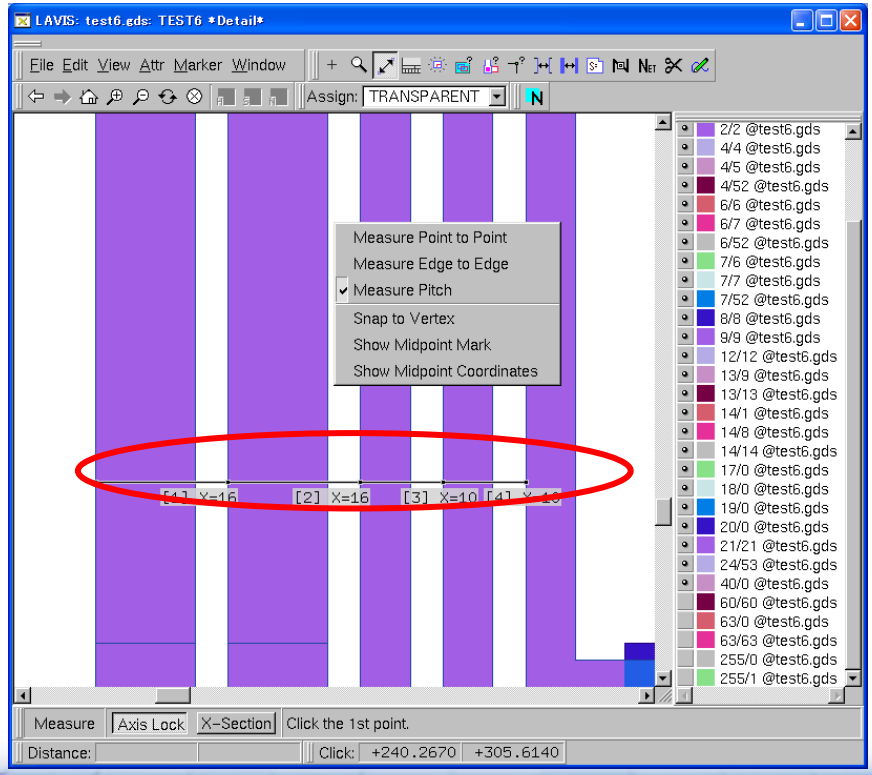
Measurement Tool has the new option

=> Line&Space can be measured at a time



03. Pitch measurement for line & space

=> MeasureTool has pitch measurement function for L/S (detect the same side edge)
Also it says the number which stands for how many pitch(es) from the end



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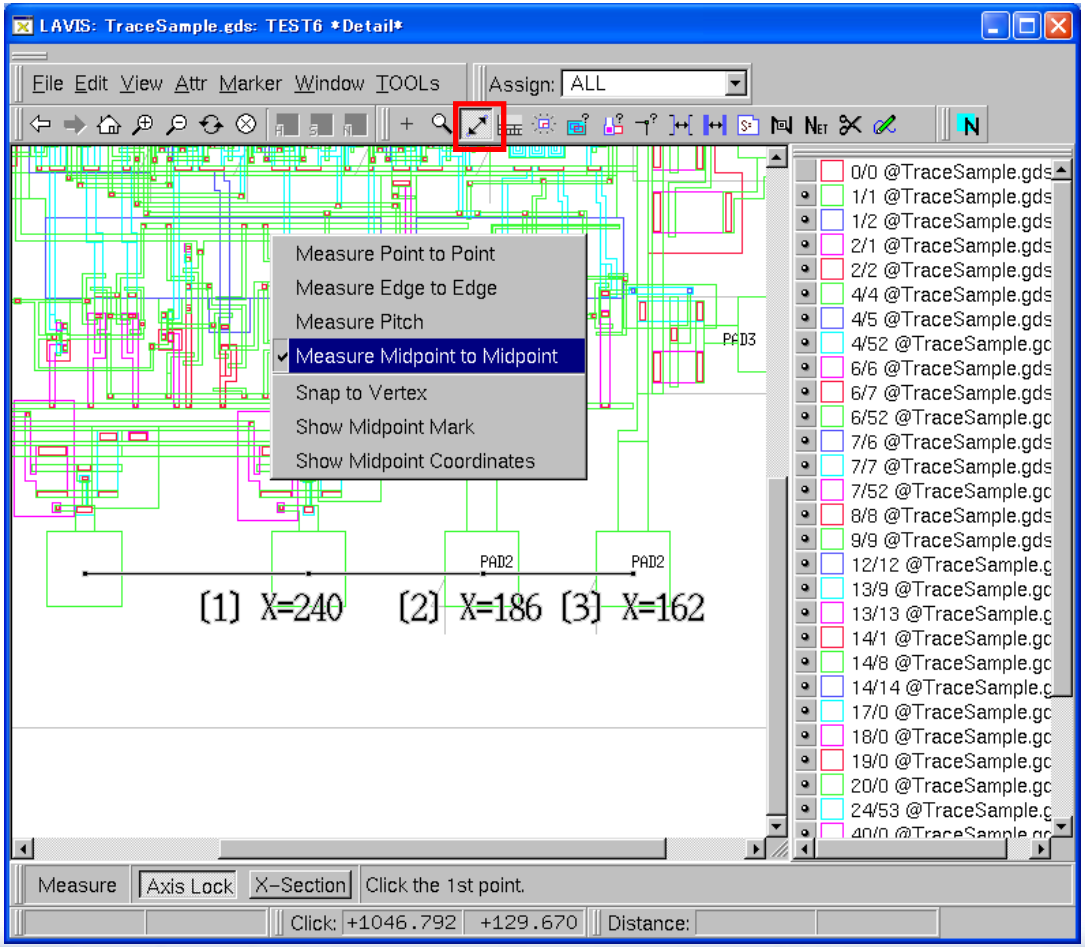
Measure between 2 midpoints

=> “Measure Midpoint to Midpoint” can be available on MeasureTool



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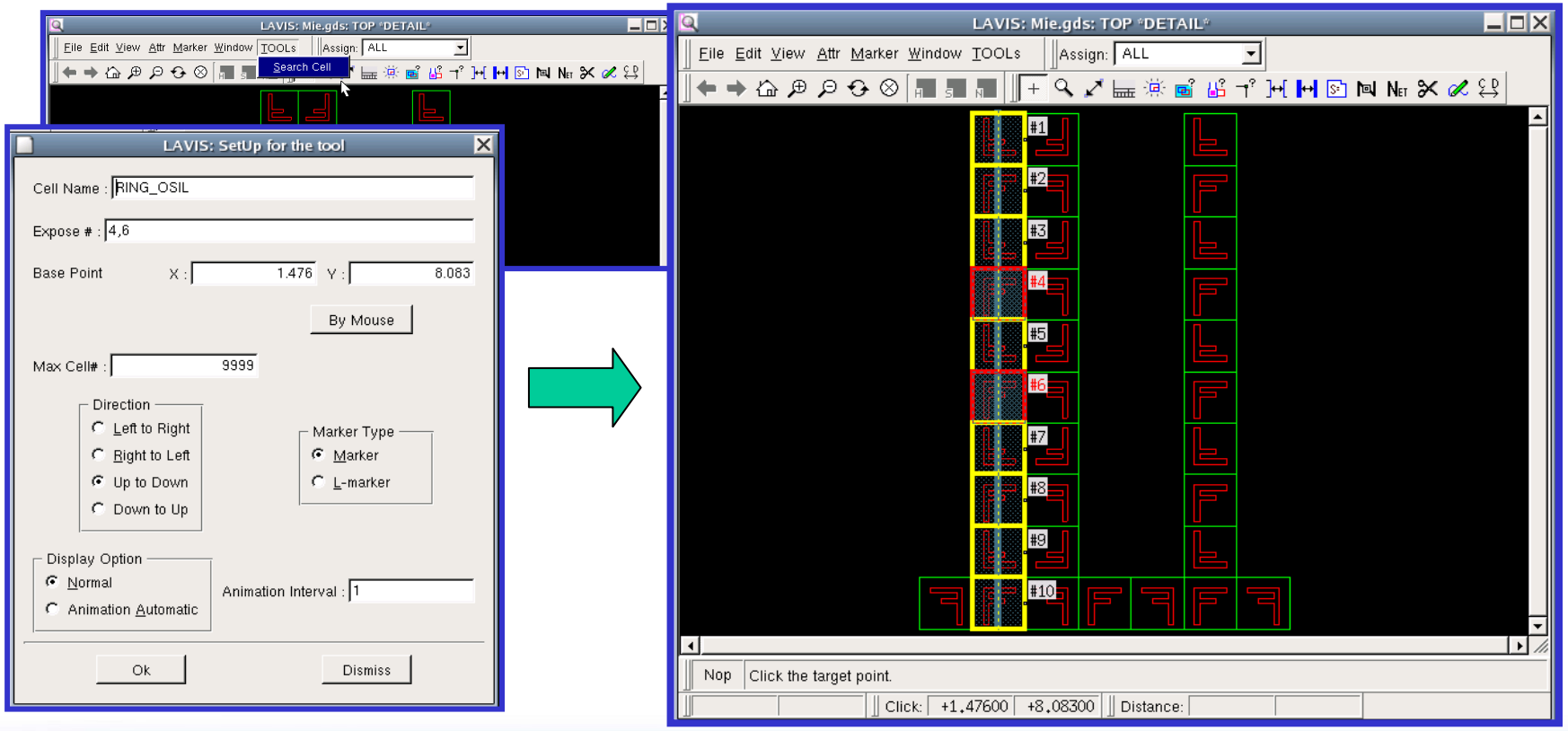
Searching Cells

< >Feature: SerchCell

Easy finding cell for the specified view area and showing order number automatically



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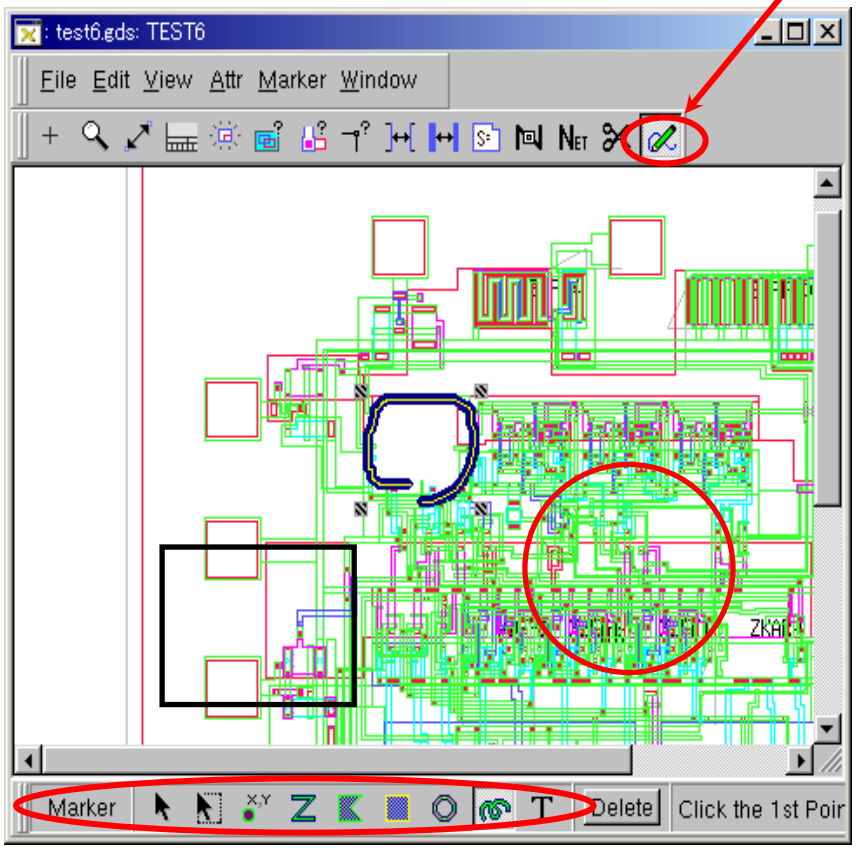
Markers



Enable to set & save various types of Marker

- Line
- Rectangle
- Polygon
- Circle
- Freehand
- Text
- Bitmap,etc …

More Easy to do check and revision of layout data

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High Cost-Performance

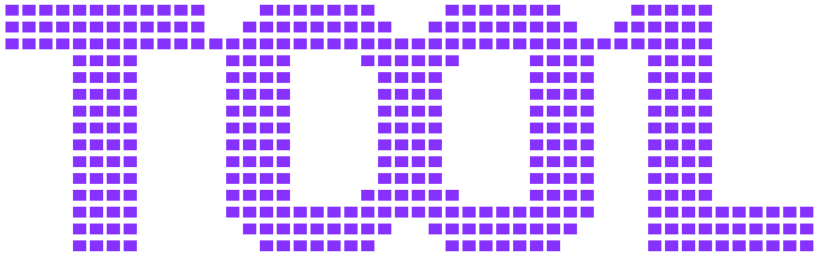
By taking advantage of

LAVIS *High-performance Multi-use Layout Analyzer*

- **Super high-speed & huge data display**
- **Powerful layout check and debug capabilities**
- **Abundant interfaces with popular EDA tools**

for the physical design and verification flow

LAVIS can shorten Turn Around Time
& provide the High Cost-Performance



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