Test & Debug with JTAG finally made easy

Product Overview

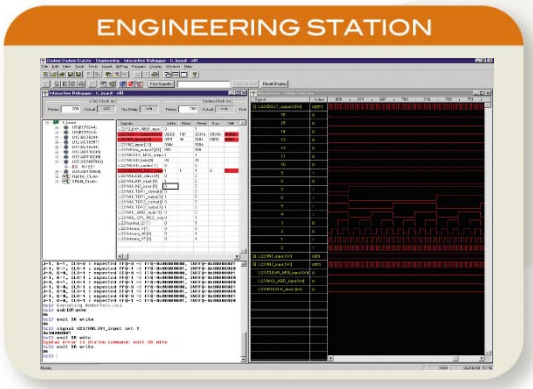
DiaTem Studio has been designed to answer the challenge of testing and debugging complex boards and systems throughout the product life cycle. You can use the same platform to operate your test environment with the highest quality standards.

The core of the platform is DiaTem Engineering Station which is the first efficient JTAG Tool dedicated to board designers.

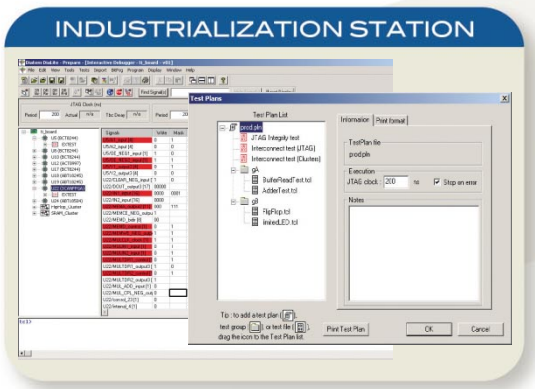
Both scalable and flexible, this platform has been customized for use in four main phases of the product life cycle:

- Engineering
- Industrialization
- Production
- Repair and Maintenance

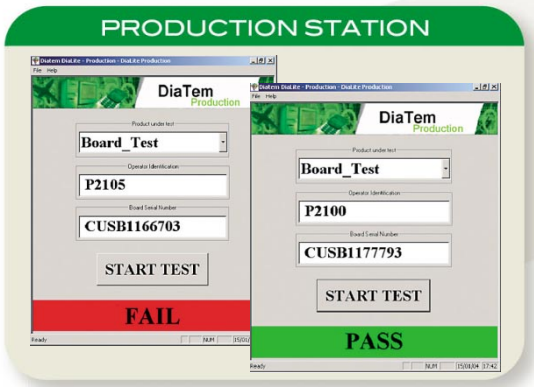
One integrated platform for all activities, from engineering to production



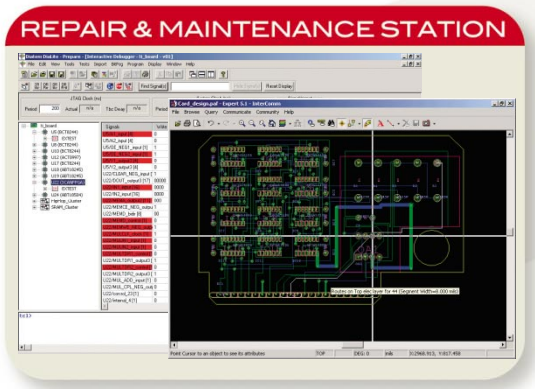
1 Test Development



2 Test Plan



3 Test Execution

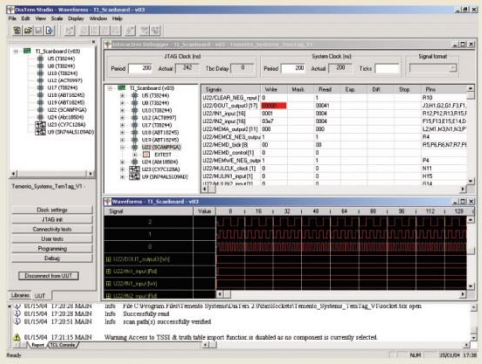


4 Test Probe

DiaTem® STUDIO

FOUR STATIONS COVER THE ENTIRE PRODUCT LIFE CYCLE

1 ENGINEERING STATION



HIGHLIGHTS

- Test coverage analysis
- BSDL components checking
- Infrastructure diagnostics (scan chain integrity)
- Automatic Test Pattern Generator (ATPG) for Interconnection, clusters and memories
- Interactive debugger
- Support of more than 90 netlist formats
- Custom test development though TCL language
- Display of results as a waveform or state table
- Fault detection on devices or boards through Interactive Access
- Interactive control and observation of signals at the register, bus or pin level
- In System programming solution option (IPSO) for Flash memory and Programmable Logic Devices (PLD)
- SVF File format export
- TemCable parallel port interface controller
- TemTag PCI and TemTag USB hardware controllers

Engineering Station allows designers and test engineers to verify and to debug boards and systems using the full potential of the benefits brought by Boundary Scan and the JTAG (IEEE 1149.1) standard.
It includes all the functionality you need to: define Unit Under Test (UUT), check BSDL, verify scan chain integrity (infrastructure tests), perform interconnect tests, create complex functional tests using TCL language and to perform diagnostics on nets and signals. This Station allows you to declare your board and build a debugging project in less than two days, which leaves you more time for your debugging!
One of the key advantages of DiaTem Studio is that it provides you with a static analysis of Test Coverage and the ability to check testability during the design process. This analysis is linked to a Net Navigator that quickly leverages your understanding of what can be improved in the JTAG testability. The benefit is that you can be sure that your DfT is optimised before manufacturing the boards. Release 2.2 adds many important features and also more flexibility, control and enhanced performance. Interconnection tests take advantage of extended configuration possibilities (tracks, clusters, algorithms) along with an average execution time that is four times faster!

ENGINEERING STATION PACKAGE INCLUDES:

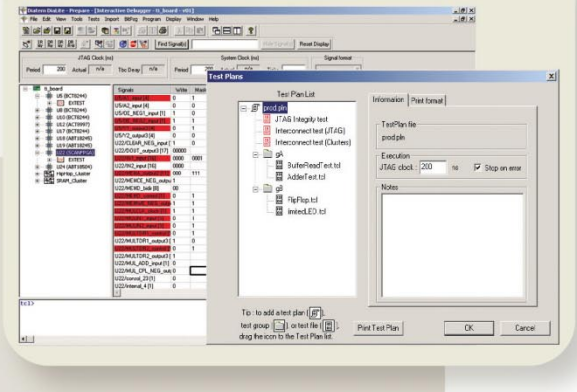
Modules	*Functional Description*
System Builder	Enables components, boards and systems description, EDIF netlist import and cluster definition
Toolbox	Advanced Debugging Functions enable individual verification of TMS, TCK, TDI, TDO and TRST signals
BSDL Checker	Checks BSDL conformity with IEEE 1149.1 Standard
Interactive Debugger	DiaTem Interactive Debugger enables the user to diagnose the system to isolate faults or failed devices
ATPG Type 1 Infrastructure	Checks that the scan chain is functional and corresponds to the design specifications
ATPG Type 2 Interconnect	Automatically tests the interconnections between testable pins
ATPG Type 3 Memory clusters	Automatically tests the interconnections between SRAM, SDRAM, DDR2, FLASH, NAND FLASH (Multiplexed), Asynchronous FIFO and SPI Serial Flash
Test Development	TCL Test Development allows engineers to create custom test applications for advanced diagnostics
FPGA / CPLD Loader	Enables programming any kind of CPLD and FPGA while debugging or testing without needing to change tools or hardware
Flash Programmer (option)	Enables programming any kind of flash memory, from installing debug subroutines, to loading boot-straps for finished boards
Netlist Merger (option)	Automates building system-level netlists for test pattern generation on multi-board assemblies
Run Time generation	Allows the export of entire databases to other DiaTem stations
Net Navigator	Displays cross-reference tables between nets, pins and JTAG cells. Allows search by type, name and cells
API DiaTem Server (option)	Enables users to integrate DiaTem in any industrial framework such as Windows CVI or Labview and bring JTAG test capabilities to their bench.
SVF Export (option)	Allows the export of DiaTem main commands (Interconnect test, FPGA programming, Flash programming) using commented SVF file format

PREVIEW AND VALIDATE YOUR "DESIGN FOR TEST" BEFORE PRODUCTION RELEASE

Temento systems

FOUR STATIONS COVER THE ENTIRE PRODUCT LIFE CYCLE

2 INDUSTRIALIZATION STATION



HIGHLIGHTS

- Re-use previously created test vectors in a manufacturing environment
- Organize and manage test data according to your needs
- Run and execute test sequences
- Generate programs for test and ISP components
- Define batch test sequences
- Export test sequences when moving to production station

Industrialization Station allows manufacturing engineers to define test sequences to be applied in a production mode.

This station enables the production and preparation of the test and programming operations to be performed on the board. Compatible with most common CAD formats to import test data, it is flexible enough to insure compatibility with engineering teams tools and Production Stations.

A powerful Test Plan Manager authorizes the definition of test and programming sequences. Test Plans can then be easily exported to another Production Station as a single directory.

DiaTem Studio now provides the opportunity to export commands and tests using the standardized Serial Vector Format (SVF is a vendor independent format representing JTAG test patterns in ASCII text files). When the SVF option is enabled, all the JTAG transactions performed are computed and registered by DiaTem using SVF format. Using this DiaTem option, the test engineer is able to produce a standardized test file for other testing platforms and to improve communication between test environments.

INDUSTRIALIZATION STATION PACKAGE INCLUDES:

Modules	*Functional Description*
System Builder	Enables components, boards and systems description, EDIF netlist import and cluster definition
Toolbox	Advanced Debugging Functions enable individual verification of TMS, TCK, TDI, TDO and TRST signals
BSDL Checker	Checks BSDL conformity with IEEE 1149.1 Standard
Interactive Debugger	DiaTem Interactive Debugger enables the user to diagnose the system to isolate faults or failed devices
ATPG Type 1 Infrastructure	Checks that the scan chain is functional and corresponds to the design specifications
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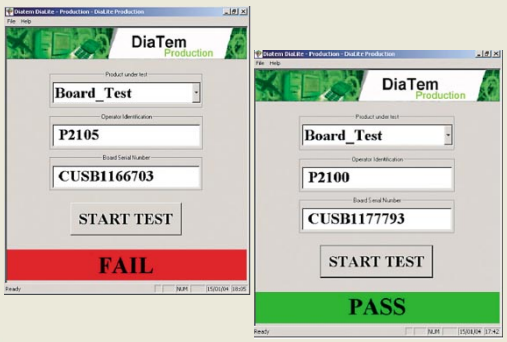
ATPG Type 3 Memory clusters	Automatically tests the interconnections between SRAM, SDRAM, DDR2, FLASH, NAND FLASH (Multiplexed), Asynchronous FIFO and SPI Serial Flash
Test Development	TCL Test Development allows engineers to create custom test applications for advanced diagnostics
FPGA / CPLD Loader	Enables programming any kind of CPLD and FPGA while debugging or testing, without needing to change tools or hardware
Flash Programmer (option)	Enables programming any kind of flash memory, from installing debugging subroutines, to loading boot-straps for finished boards
Netlist Merger (option)	Automates building system-level netlists for test pattern generation on multi-board assemblies
Test Plan Manager	Allows the organisation of all the preceding test sequences automatically in a pre-defined order for production
Run Time generation	Allows the export of entire databases to other DiaTem stations
Fault Ticket Edition	Provides reports from a simple fault ticket (pass/fail) to ones with more details including instructions for repair operators
Net Navigator	Displays cross-reference tables between nets, pins and JTAG cells. Allows search by type, name and cells
API DiaTem Server	Enables the user to integrate DiaTem in any industrial framework such as Windows CVI or Labview and bring JTAG test capabilities to their bench.
Production Test Execution	Includes all the necessary features to enable a Test Plan execution provided by the DTS Industrialization Station. This module can execute the entire test Plan including Test of integrity of the scan chain and components ID codes, Test of all interconnect types, Functional Test sequences and FPGA/CPLD loader

SVF FILE FORMAT EXPORT FEATURE BRINGS YOU A NEW WAY TOUNLEASH THE POWER OF JTAG

FOUR STATIONS COVER THE ENTIRE PRODUCT LIFE CYCLE

3

PRODUCTION STATION



HIGHLIGHTS

- Reuse previously generated test plans
- Apply automated test programs to the UUT
- Execute automatic test and ISP programs
- Monitor operator or supervisor priority levels
- Deliver operations reports and fault tickets

Production Station allows test operators to automatically run and to execute test plans and test sequences on a production line.

This station is dedicated to board-testing in a production environment. It allows the selection and execution of a test plan previously created on an Industrialization Station.

The Supervisor level module allows the definition of test sequence settings, and the selection of a test plan to set up the best test strategy. The Operator level module allows working in a standardized environment and running production tests.

Access to Test Plans has been improved with a dedicated tab in the User Test dialog box.

PRODUCTION STATION PACKAGE INCLUDES:

Modules	*Functional Description*
FPGA / CPLD Loader	Enables programming any kind of CPLD and FPGA while debugging or testing without needing to change tools or hardware
Flash Programmer (option)	Enables programming any kind of flash memory, from installing debug subroutines, to loading boot-straps for finished boards
Fault Ticket Edition	Provides reports from a simple fault ticket (pass/fail) to ones with more details including instructions for repair operators
API DiaTem Server	Enables the user to integrate DiaTem in any industrial framework such as Windows CVI or Labview and bring JTAG test capabilities to their bench.
Production Test Execution	Includes all the necessary features to enable a Test Plan execution provided by the DTS Industrialization Station. This module can execute the entire test Plan including the following types of tests: • Test of integrity of the scan chain • Verification of components ID codes • Test of all interconnect types (ATPG 1, 2 & 3) • Functional Test sequences execution • FPGA/CPLD bitstream loader • FLASH programmation
Bar Code Reader	UUT and Operator identification capability
Operator Control Panel	Enables an un-trained operator to select the board type to test, enter the serial number, launch the test, and read the PASS/FAIL result
Supervisor Control Panel	Enables a Test Plan definition for each board type that will be usable by the operator. Allows the supervisor to modify the Test Plan or the test sequence settings and verify JTAG cable and signal integrity before releasing a production run

RUN YOUR SELECTED TEST PLANS AND AUTOMATE YOUR PRODUCTION IN GO/NO GO MODE

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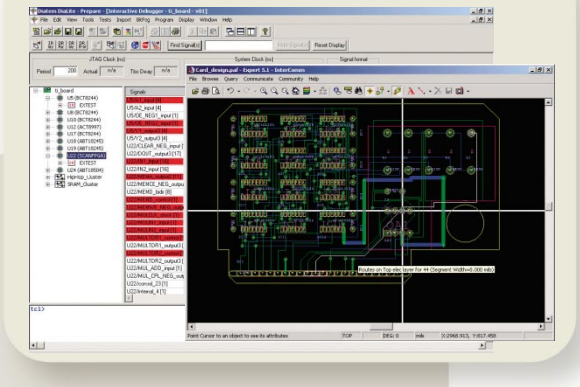
FOUR STATIONS COVER THE ENTIRE PRODUCT LIFE CYCLE

4

REPAIR & MAINTENANCE STATION



HIGHLIGHTS

- View design data in lay-out mode (Option)
- Highlight faulty nets with specific color assignments
- Localize defects
- Run and execute test sequences
- Export statistical data
- Write specific tests

Repair and maintenance Station is used by production engineers to make easy diagnostics and to perform quick repair on failing boards coming from the production station or from the field.

This platform provides assistance for defective board repair, highlighting the faults in the design and/or lay-out files. Based on the diagnostic results from the production station, the operator can get an instant view of the different nets or pins which are faulty and see all the related connectivity.

Net Viewer module allows to quickly localize the defective net. A guided probe helps determine which part of the net is faulty, to verify the diagnostic and leads to a fast and effective repair.

REPAIR AND MAINTENANCE STATION PACKAGE INCLUDES:

Modules	*Functional Description*
Toolbox	Advanced Debugging Functions enable individual verification of TMS, TCK, TDI, TDO and TRST signals
Interactive Debugger	DiaTem Interactive Debugger enables the user to diagnose the system to isolate faults or failed devices
Test Development	TCL Test Development for engineers to create custom test applications for advanced diagnostics
FPGA / CPLD Loader	Enables programming any kind of CPLD and FPGA while debugging or testing without needing to change tools or hardware
Flash Programmer (option)	Enables programming any kind of flash memory, from installing debug subroutines, to loading boot-straps for finished boards
Fault Ticket Edition	Provides reports from a simple fault ticket (pass/fail) to ones with more details including instructions for repair operators
Net Navigator	Displays cross-reference tables between nets, pins and JTAG cells. Allows search by type, name and cells
PCB Trace Viewer (option)	Displays board layout data, highlighting those nets implicated in a fault found by the tester; which helps the operator to locate faults
Production Test Execution	Includes all the necessary features to enable a Test Plan execution provided by the DTS Industrialization Station. This module can execute the entire test Plan including the following types of tests: • Test of integrity of the scan chain • Verification of components ID codes • Test of all interconnect types (ATPG 1, 2 & 3) • Functional Test sequences execution • FPGA/CPLD bitstream loader

LET THE STATION GUIDE YOU THROUGH EASY FAULT-LOCATION TO FAST AND EFFECTIVE REPAIR

Temento systems

What's new in Rev 2.2 ?

- Interconnection tests take advantage of extended configuration features with selection of tracks, clusters, algorithms along with an average execution time that is four times faster !
- New Memory Cluster ATPG support :
  - DDR2-SDRAM
  - NAND FLASH (Multiplexed)
  - Asynchronous FIFO (Ring Addressing scheme)
  - Flash SPI and Flash programming through I2C bus
- Improved FLASH protocol window : commands are gathered by tabs
- The largest list of CAD Netlist file support which includes Accel EDA, Cadence Allegro, Cadstar, CV 4X, Encore, Genrad, Mentor, Orcad, PADS PowerPCB, PCAD, Protel, Veribest, Viewlogic. Visula and others
- Improved JTAG component creation (automatic BSDL import during creation)
- LVDS testability: this release adds a LVDS transmission-line model which allows you to declare the pair of signals and detect the 1149.1 testable faults
- Improved SVF export allows you to split the file per type of test. This feature is required by some production testers, like Teradyne, and leads to enhanced diagnostics when a fault is detected
- The ability to erase a Flash memory sector by sector
- Ability to associate a cluster signal to 2 cells: one for Read, one for Write
- A new USB driver supporting the TRST signal on pin 5
- Improved access to test plans with a dedicated tab in User Test dialog box

For pricing and availability, please contact our sales network
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For technical info, please contact our customer service
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For more info on Temento Systems solutions, please visit our web site http://www.temento.com/

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