



Make it easy

- Company Overview
- Dialite Products
- Competitive Analysis
- Customers
- Distribution Channels



Temento Company History

Temento History

- 
- 1995 Company founded
 - 1996 Test Services
 - 1997 1 patent granted
 - 2001 DiaTem Product Release
 - 2003 DiaLite Product Release
 - 2004 Sales Channel Formation
 - 2005 Sales Ramp-up
 - 2006 2 more patents granted
 - 2007 DiaLite Power Edge
 - 2008 DiaTem 3 release
 - 2009 DiaLite 4.7 release

Temento Confidential

- Focus on the debug and verification of complex FPGA, SoC, and PCB designs
- 100 consumers and communications electronics customers worldwide
- Headquartered in Grenoble France, with sixteen, predominantly R&D, employees
- Unique core technology, three patents
- Two successful, mature product lines



DiaTem[®]

The test and debug of complex PCBs



DiaLite
INSTRUMENTATION

The verification and debug of FPGAs and SoCs post fabrication

PATENTED TECHNOLOGY





Diatem Overview

Diatem Lab is composed of 4 stations to test electronics boards throughout the product life cycle



1
Test Development



2
Test Plan



3
Test Execution



4
Test Probe

A WorkStation running DiaTem

A Hardware
JTAG
Controller

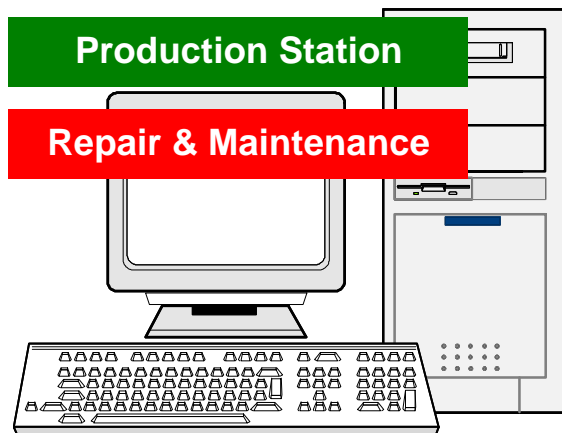
Your Units
Under Test

Engineering Station

Industrialization Station

Production Station

Repair & Maintenance



UUT 1

UUT 2

UUT 3

UUT 4



Make it easy

Traditional Logic methods Replaced With In system Debug Solutions

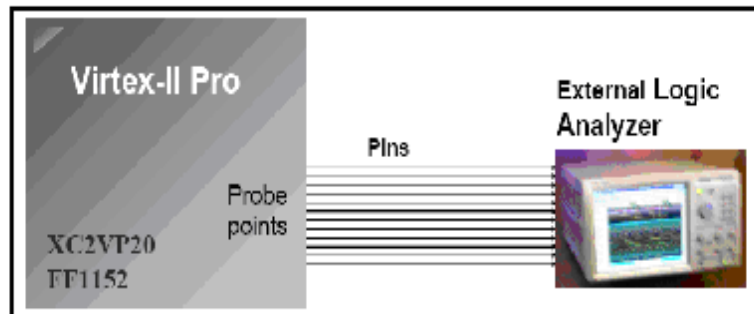
AFTER DFT TECHNOLOGY ADOPTION



INSTRUMENTATION IS MOVING ON CHIP

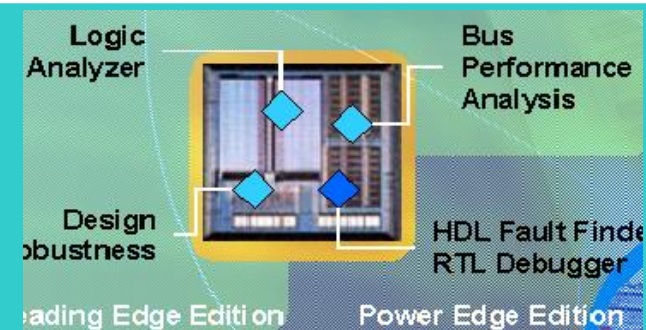
Traditional Logic Analysis Method

Dedicated pins connected to logic analyzer



- Requires extensive dedicated I/O for debug
 - Driving signals to external I/O introduces additional problems
- Inflexible solution
 - Difficult or impossible to add additional debug pins if needed
- Limited visibility to on-chip activity

In System Debug Solution



Integrate a logic analyzer in the FPGA GIVES:

- Access to the complete data bus
- Access to all internal design nodes.
- Operates at the full system speed
- synchronous the the design clock

Verification Needs Visibility

- **FPGAS ARE GETTING BIGGER, FASTER, EMBED LARGE BUSSES, DSP CORES, LOGIC ETC.. MAKES SIGNALS EXTRACTION INFEASIBLE!!**

BOTTLENECK

- **PACKAGES ARE GETTING SMALLER WITH MORE PINS, DO NOT HAVE EXPOSED LEADS THAT CAN BE PHYSICALLY PROBED!**

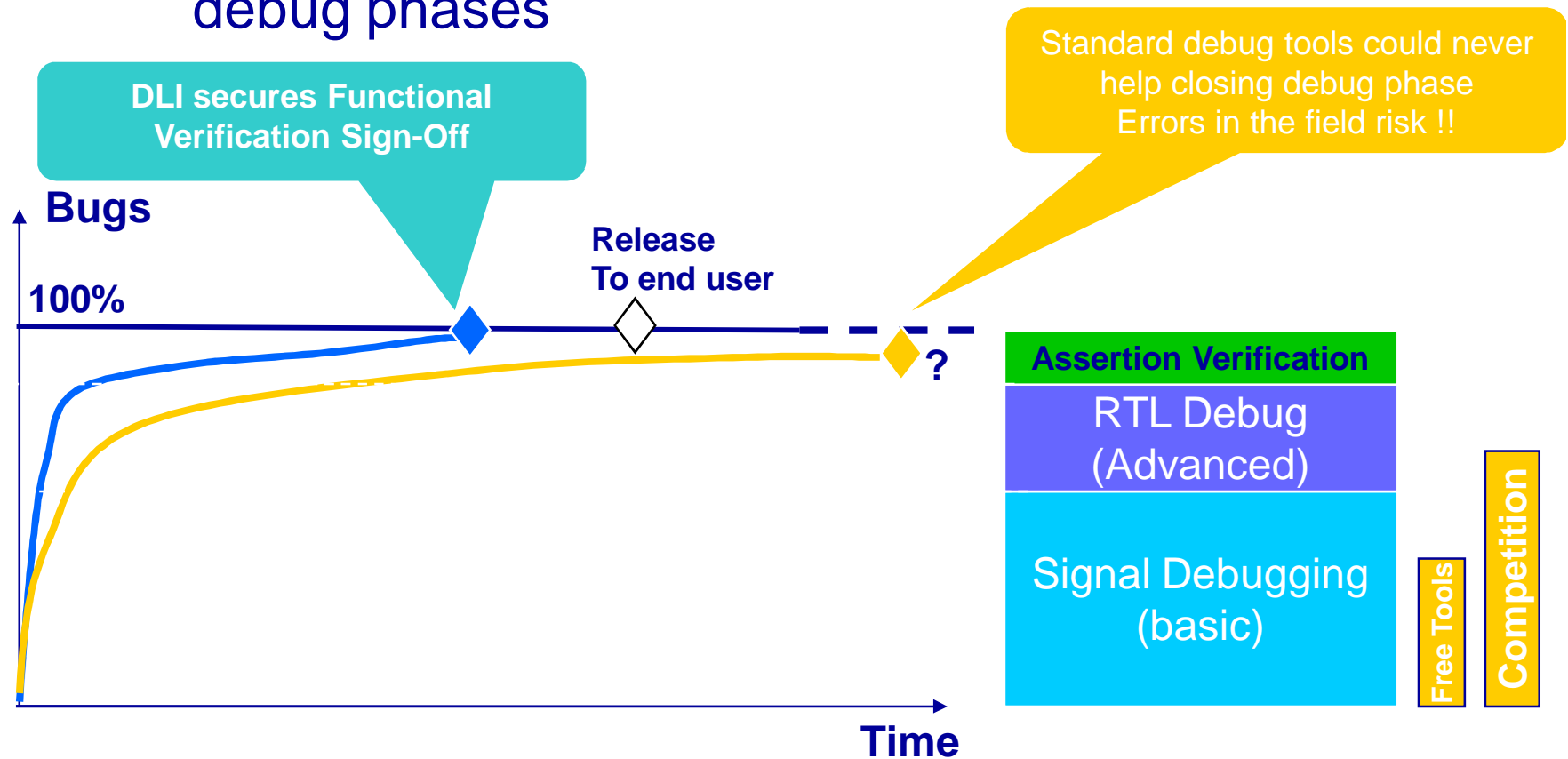
BOTTLENECK

- **BOARDS ARE GETTING SMALLER WITH MORE LAYERS. TRACES ARE OFTEN BURIED INSIDE MULTI-LAYER PRINTED CIRCUIT BOARDS**

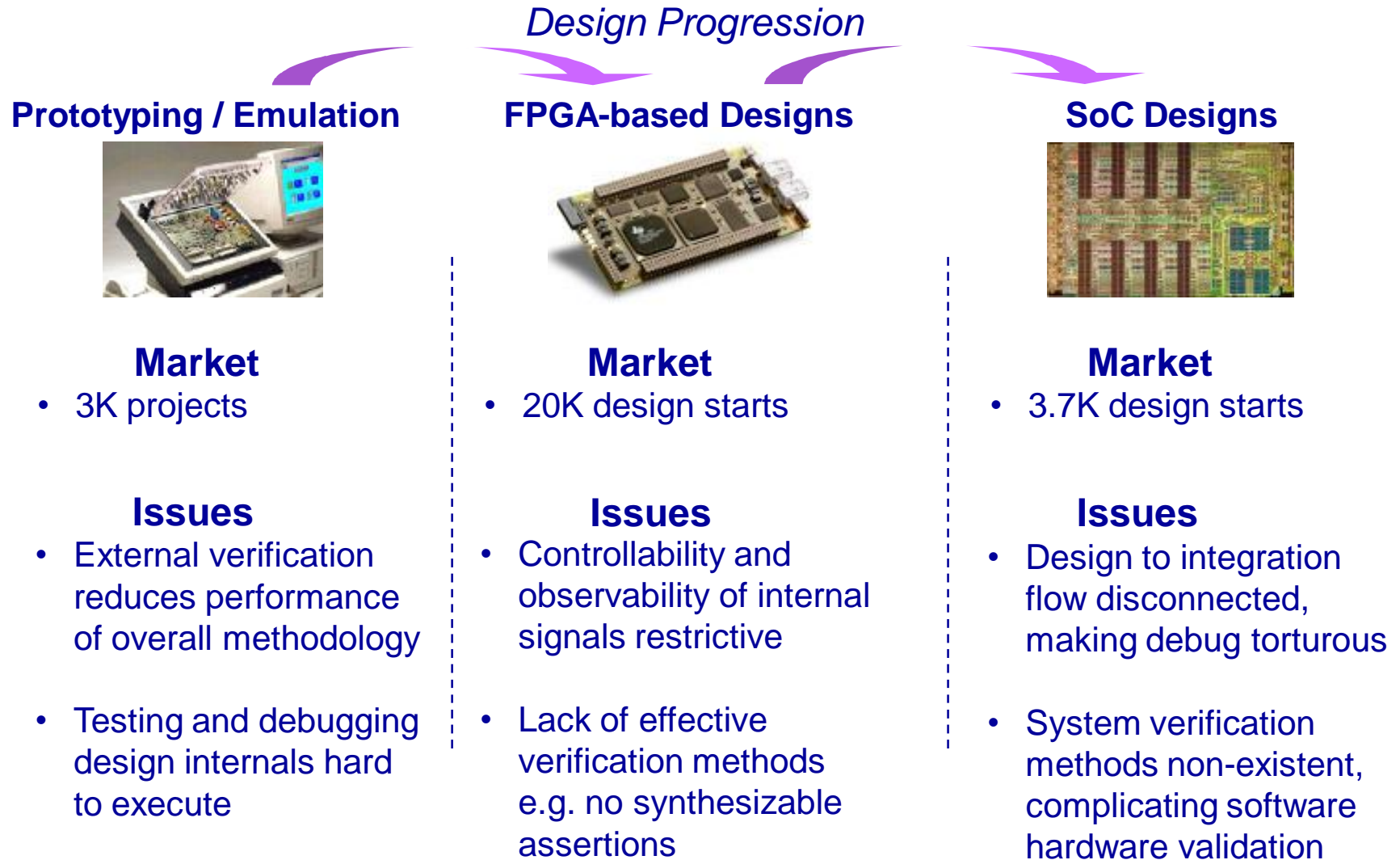
**TRADITIONAL METHODS RUN OUT OF STEAM
NO TECHNIQUES ON THE MARKET AVAILABLE TO COVER ALL CORNER CASES YOU
MISSED IN SIMULATION/EMULATIONNON-CHIP VERIFICATION & DEBUGGING TOOL**

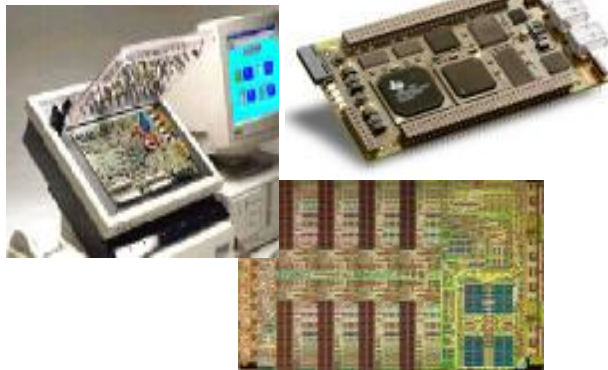
Dialite Key Benefit

- Endless debug loop threatens time-to-market
- Dialite is the only commercial tool supporting all debug phases



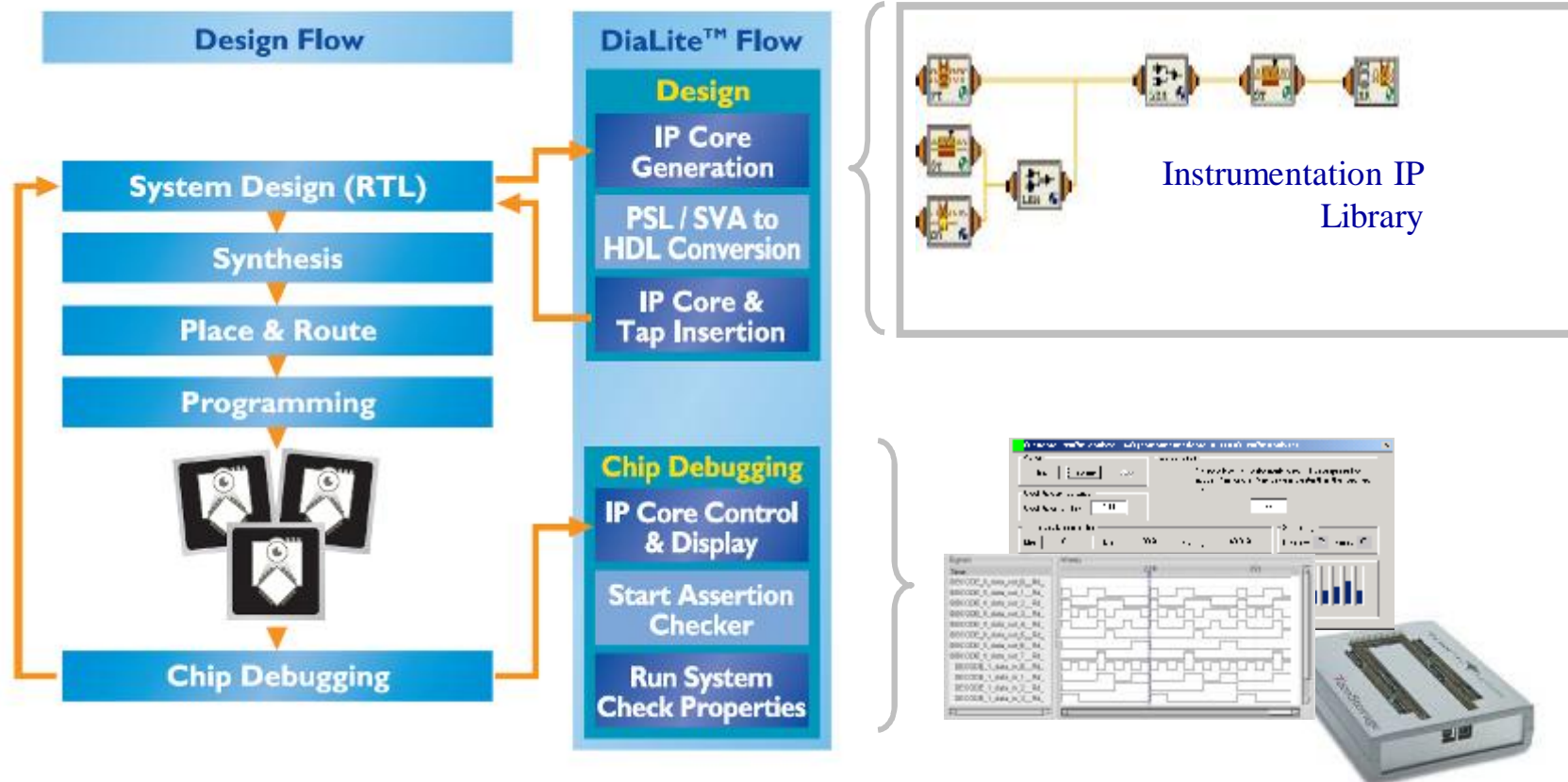
DiaLite Opportunity Throughout Platform Flow





DiaLite Design Flow

IP instrumentation cores are inserted at the RTL level.



User Friendly Interface

§ Create your Debug Project with graphic tools in just few clicks !

The screenshot displays the Temento systems User Friendly Interface for creating a debug project. The interface is divided into several panes and sections:

- Design Project Hierarchical levels and source files:** A tree view on the left shows the project hierarchy, including "Workspace - DU_DEMO_STRATIX_45_1", "DU_DEMO_STRATIX", "Instruments", and "Sources".
- Instrumentation:** A central pane displays the "DU_DEMO_STRATIX - BRIDGE_ASSERTION_I" and "DU_DEMO_STRATIX - BRIDGE_ASSERTIC" views, showing data input and output signals.
- Signals to be instrumented:** A list of signals is shown, including "IRQ_TRIGGER", "BRIDGE_DATA", "PWM_ST", "PWM_HR_2", "PWM_COMMAND", "PWM_PRG", "MEMORY_TRIGGER", "MEMORY_LEM", "ADDRESS_BUS_CHECKER", "MEMORY_TRANSACTIONS", "PWM_TA", "BRIDGE_TA", "BRIDGE_DEBUG", "PWM_ULM", and "PWM_ULM".
- Messages logging:** A bottom pane displays messages, including "Loading file C:\DLI_DEMO_STRATIX_b45029_NEWDLI_DEMO_STRATIX\HDL\TempSource\PWM.vhd", "STRATIX_b45029_NEWDLI_DEMO_STRATIX\HDL\Ref\PWM_ULM_Regul_Monitoring.vhd", "STRATIX_b45029_NEWDLI_DEMO_STRATIX\HDL\RefAck_counter.v", "STRATIX_b45029_NEWDLI_DEMO_STRATIX\HDL\RefBRIDGE_ASSERTION_CHECKER_Bridge_assertions.vhd", and "Loading file C:\DLI_DEMO_STRATIX_b45029_NEWDLI_DEMO_STRATIX\HDL\Ref\OR.vhd".
- Signals of instruments:** A right pane displays a grid of instrument icons, including "PWM_TA", "BRIDGE_TA", "ULM", "PWM_HR", "ST", "PWM_HR_2", "BRIDGE...", "ACK_COU...", "PROCESS", "PWM_COM...", "PRG", "PWM_PRO", "BRIDGE...", "ULM", "OR", and "BRIDGE...".

The interface also includes a "Connect" button, a "Disconnect" button, and a "Disconnect all" button. The status bar at the bottom shows "Watch point : 34 Line, column".

Dialite Instruments Portfolio

A Collection of 14 Debug IPS

Triggers



Parallel



Serial



**Glitch
Detector**

Combinatory Logic



**Logic
Equation
Module**



**User
Logical
Module**

Pattern Generators



**Switch &
Leds**



**Pseudo
Random
Generator**

Analzers/Bus Monitoring



**Traffic
Analyzer**



**Bus
Range
Checker**



**AMBA
Bus Tracer**

Recorders



**History
Register**

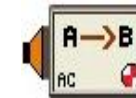


**Transaction
Register**

Verification Code Debug



**HDL Fault
Finder**



**Assertion
Checker**

An Instrument for each Issue

§ *Traffic density on a bus, throughput measurements, statistics issues ?*

► Use the Traffic Analyzer !

§ *Design robustness checking issue ?*

► Use the Pseudo Random Generator !

§ *Synchronism test of sensitive signals (like IRQ) issue ?*

► Use the Glitch Detector !

§ *Dedicated instruments needs ?*

► DLI provides the User Logical Module !

The screenshot shows the 'Traffic Analyzer' IP core configuration window. It includes controls for 'Init', 'Resume', and 'Stop'. The 'Output Level' is set to 80%. The 'Traffic analyzer statistics' section shows 'Min: 0%', 'Max: 100%', and 'Average: 48.0%'. A bar chart displays the 'Last thirty current value'.

The screenshot shows the 'Pseudo Random Generator' IP core configuration window. It includes a 'Name' field set to 'pseudorandom_generator'. The 'Clock Settings' are set to 'Rising' and 'Clock Edge'. The 'Cycle Length' is set to 1. The 'Action' section has 'Init', 'Start', and 'Stop' buttons.

The screenshot shows the 'Glitch detector' IP core configuration window. It includes 'Start' and 'Stop' buttons. The 'Searching' section has a refresh button and 'Occurence' set to 0. The 'Signals' table lists several signals with their status.

Signals	Radix	Status	Don't care
PWM_command[6:0]	Hexa	glitch	00
PWM_command_6	Hexa	no glitch	0
PWM_command_5	Hexa	no glitch	0
PWM_command_4	Hexa	no glitch	0
PWM_command_3	Hexa	no glitch	0
PWM_command_2	Hexa	glitch	0

The screenshot shows the 'User Logical Module' IP core configuration window. It includes 'Update', 'Stop', 'Uploading', and 'View Load and Switch' buttons. The 'Signals' table lists several signals with their status.

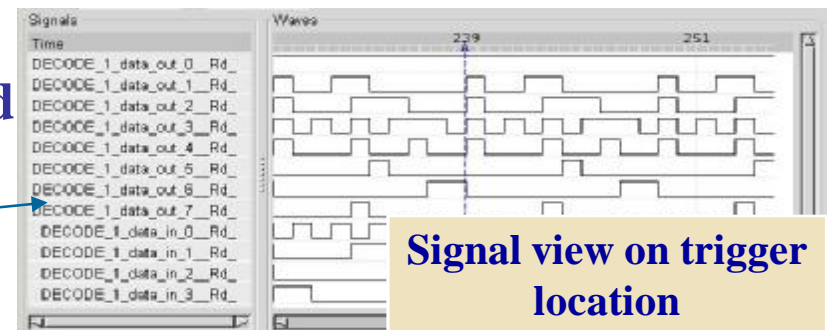
Signals	Radix	Unaltered Value	Mode	Value
regul[6:0]	Hexa	5B	Observe	5B
input1[6:0]	Hexa	5B	Observe	5B
output1	Hexa	0	Observe	0

DiaLite Power Edge & the HDL FF

§ HDL Fault Finder expands debug productivity by providing a bridge between signals on silicon and RTL code!

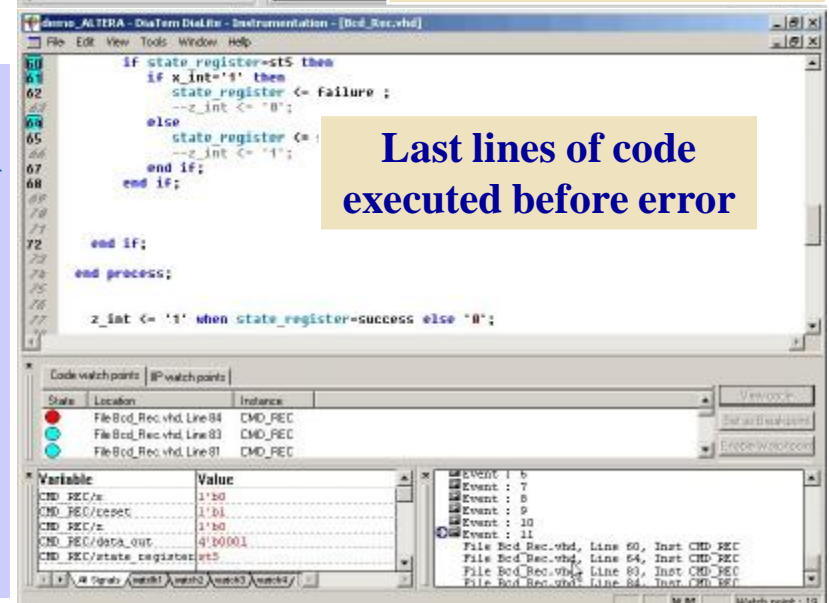
► When a trigger condition happens, it becomes easy to find error into HDL code

► Using HDL FF, you're directly pointed to the error :



```
60 if state_register=st5 then
61   if x_int='1' then
62     state_register <= failure ;
63     --z_int <= '0';
64   else
65     state_register <= success;
66     --z_int
67   end if;
68 end if;
69
70
71
72 end if;
73
74 end process;
75
76
77 z_int <= '1' when state_register=success else '0';
```

Use a Trigger as a
Hardware
Breakpoint in the
HDL FF



Last lines of code
executed before error

State	Location	Instance
●	File Bcd_Rec.vhd, Line 84	CMD_REC
●	File Bcd_Rec.vhd, Line 83	CMD_REC
●	File Bcd_Rec.vhd, Line 81	CMD_REC

Variable	Value
CMD_REC/z	1'b0
CMD_REC/reset	1'b1
CMD_REC/z	1'b0
CMD_REC/data_out	4'b0001
CMD_REC/state_register	st5

Event 1: 5
Event 7
Event 8
Event 9
Event 10
Event 11
File Bcd_Rec.vhd, Line 60, Inst CMD_REC
File Bcd_Rec.vhd, Line 64, Inst CMD_REC
File Bcd_Rec.vhd, Line 69, Inst CMD_REC
File Bcd_Rec.vhd, Line 84, Inst CMD_REC

DiaLite Power Edge & the HDL FF

The screenshot displays the DiaLite software interface with several key components:

- HDL Code:** A window showing Verilog code for `Bcd_Rec.vhd`. The code includes a process for `state_register` and `z_int`.
- Waves:** A window showing a timing diagram with signals like `cmd_rec_data_out` and `cmd_rec_state_reg`.
- Code watch points / IP watch points:** A table listing watchpoints for `CMD_REC` at various lines in `Bcd_Rec.vhd`.
- Variable:** A table showing the current values of variables like `CMD_REC/x`, `CMD_REC/reset`, and `CMD_REC/data_out`.
- Events:** A list of events (1-11) with their corresponding file locations and instances.
- Watch Point Insertion:** A dialog box for inserting watchpoints, showing a tree view of the design and a list of statements.

Annotations on the screenshot include:

- HDL Code** (pointing to the code window)
- Manage your IP Flow, Check the waves** (pointing to the waves window)
- User Defined Variables** (pointing to the variable table)
- Events** (pointing to the events list)
- Insert Watchpoints in manual or automatic mode** (pointing to the watch point insertion dialog)
- And Check in correlation...** (pointing to the watch point insertion dialog)

Hard/Soft Co-Debug

§ Hard/Soft Co-Debug is easily performed using DiaLite dedicated TAP option :

- ▶ Leave the native TAP to Soft Debug tools
- ▶ Use dedicated TAP (Altera, Xilinx) for DiaLite Instrumentation

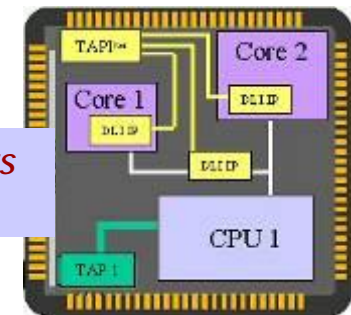
Set up HW Trigger on CPU IT with DiaLite

§ Link your C code to an HDL Debugger

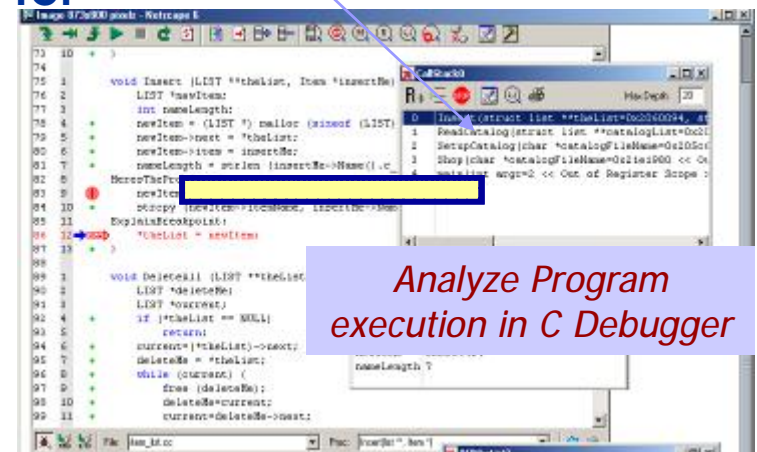
§ Increase performance of instrumentation monitoring

§ Leave instruments in the production chip for acceptance or maintenance

HW Trigger halts CPU execution



Analyze Program execution in C Debugger



DiaLite Platform & the AC

Definition: An Assertion is the execution of a Property, which itself can be seen as a fragment of an executable specification

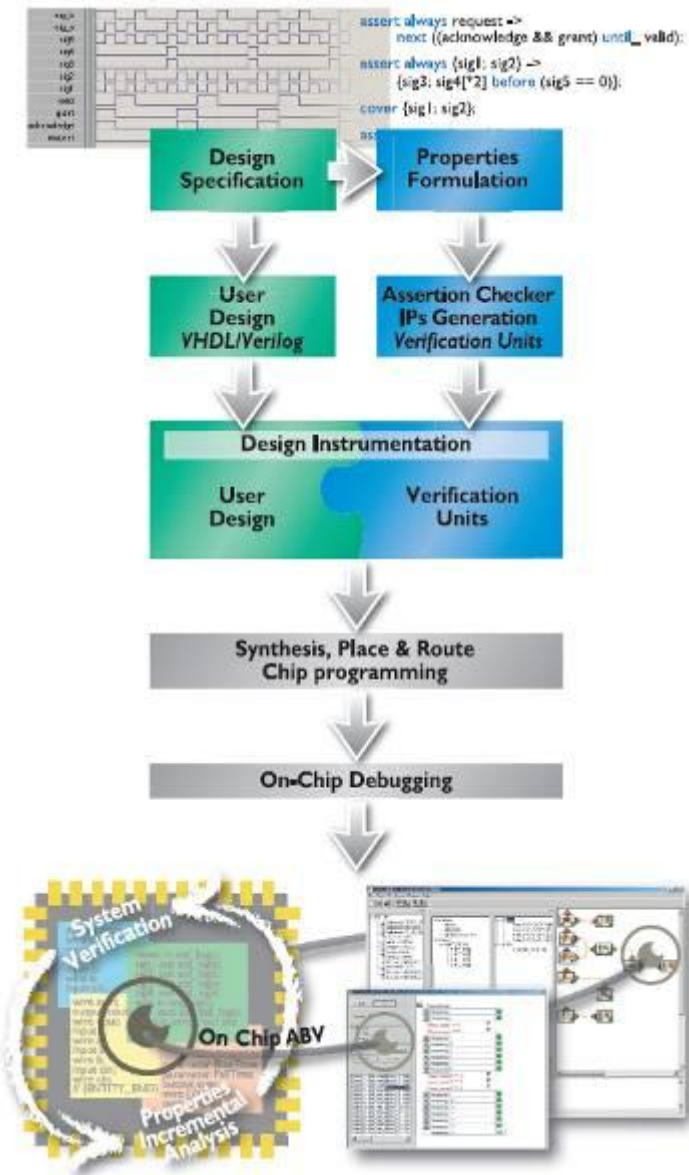
§ The Assertion Checker (AC) IP imports the assertions & embeds them into your chip

§ DiaLite Platform is the ONLY one to use your formal properties written during System Specification and to :

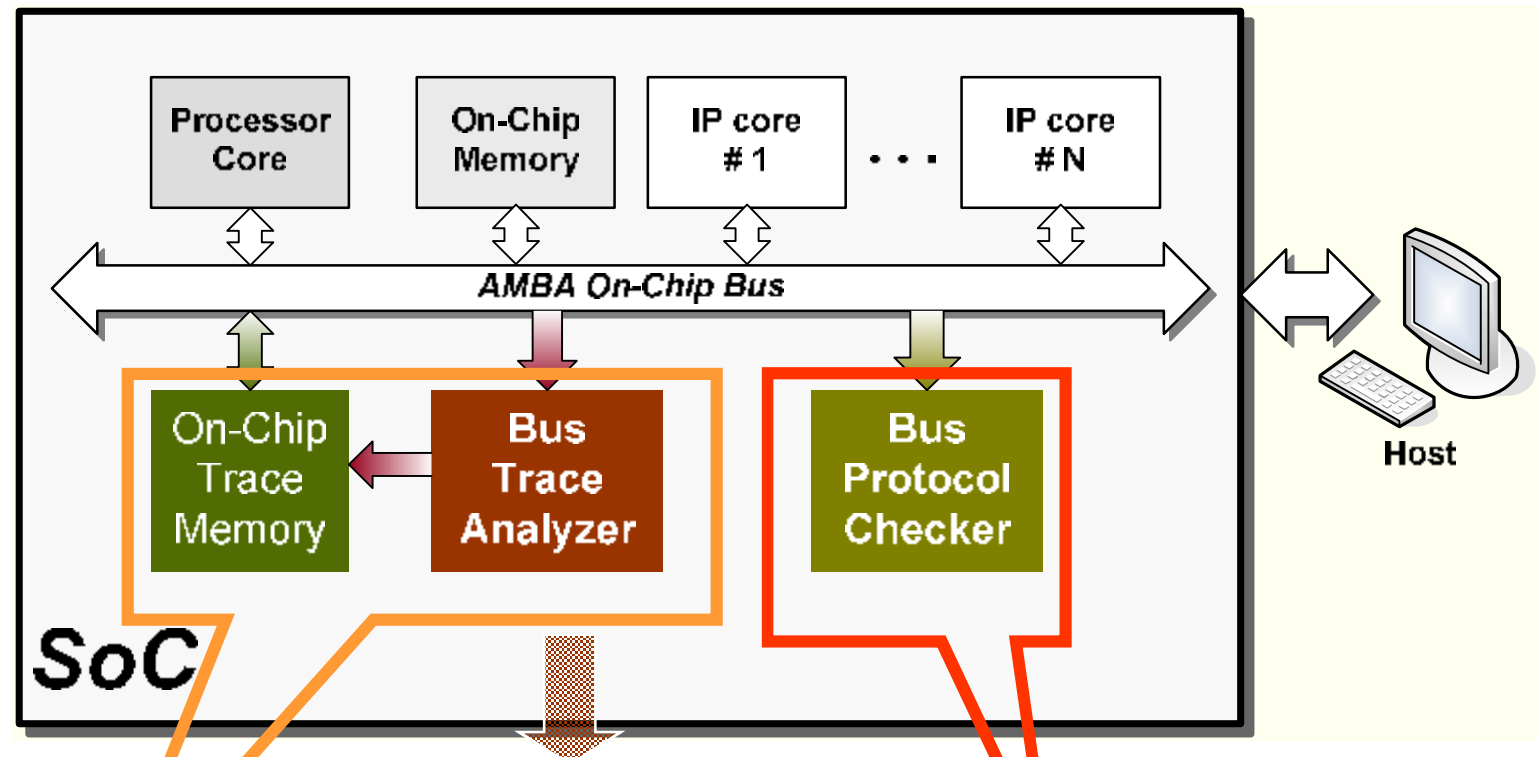
§ Run them On Silicon

§ Run them At Speed

§ Get Real-Time feedback & coverage



Instrumentation for bus analysis and debug

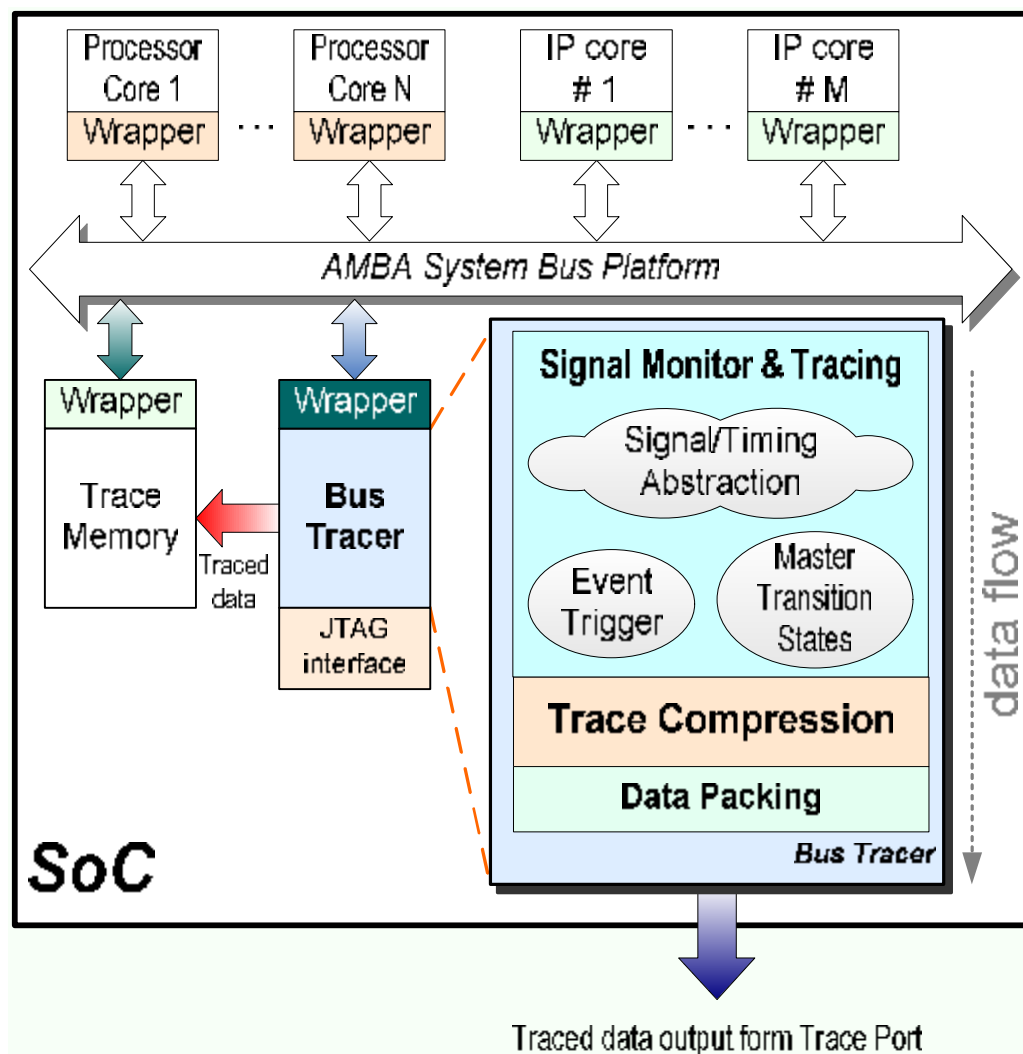


Bus Trace Analyzer

Bus Protocol Checker ⁽¹⁾



INTEGRATED TRACE AND ANALYSIS SOLUTIONS FOR EMBEDDED PROCESSORS

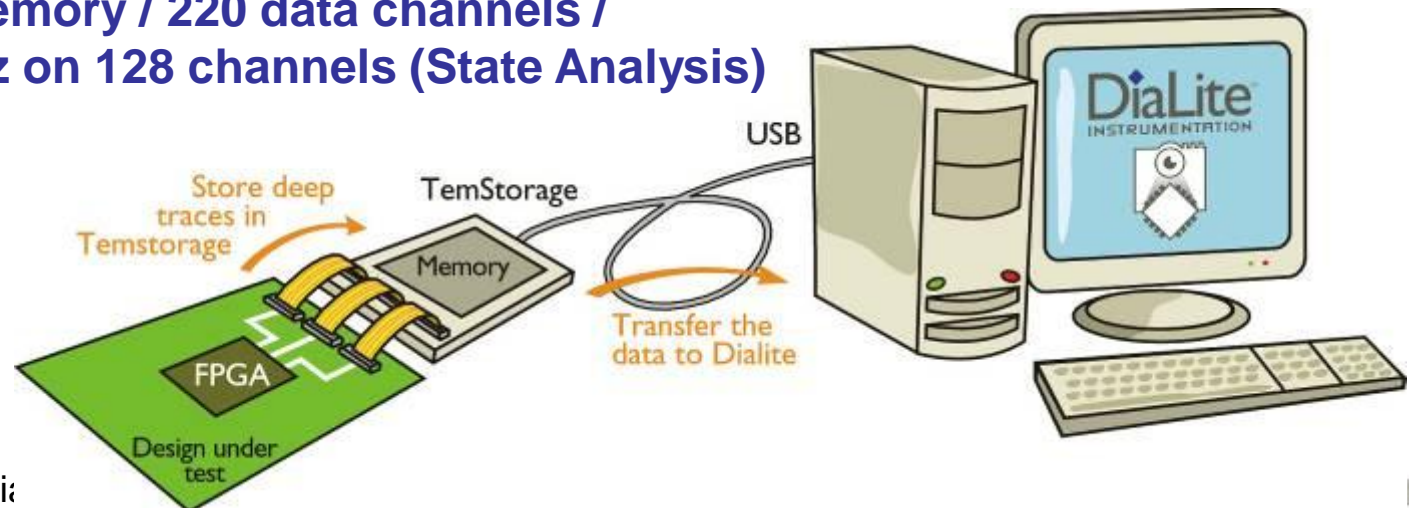


- **JTAG Interface**
 - user can setup the tracer through JTAG port
- **Signal Monitor & Tracing (Signal/Timing Abstraction)**
 - to determine when and which signals should be monitored
- **Trace Compression**
 - to compress the trace size generated from timing/signals abstraction module
- **Data Packing**
 - packs the trace data generated from the data compression module and buffer the output data
- **Trace Output**
 - transfers the trace data to host (PC)
 - Stored in/out on-chip memory

TemStorage & Off-Chip Data Record


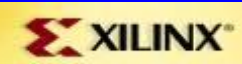


§ TemStorage frees the FPGA resources of your Debug project !

- ▶ Store large amount of Data outside your DUT and stream them to the Host PC through USB
- ▶ Seen in DLI as a Memory device for Test IPs working with RAM or Registers (like History or Transaction Registers)
- ▶ TemStorage parameters can be customized from DiaLite GUI
 - ▶ 1GB Memory / 220 data channels /
 - ▶ 100 MHz on 128 channels (State Analysis)



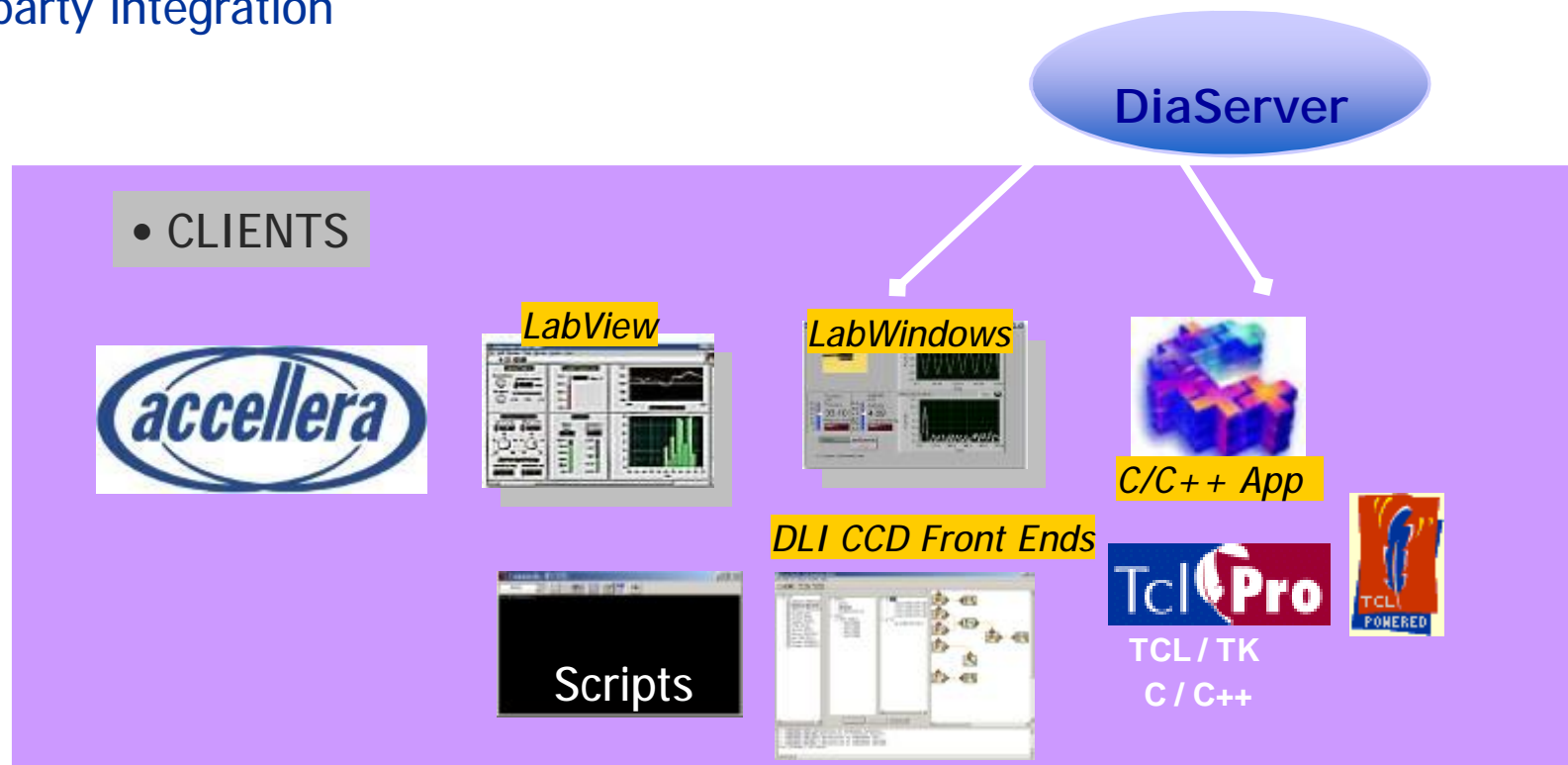
Device Independence

- § Same Debug Possibilities whatever is your FPGA Manufacturer
- § Same Debug Possibilities whatever is your Design Flow Provider
 - § Start a project with a manufacturer, move to any other !
 - § Split it between several FPGA targets, DiaLite is Multi-FPGA compatible !
 - § DiaLite can run mixed VHDL / Verilog Designs
 - § Assertions can be written in PSL or SVA
- § Possibility to use a dedicated or the native TAP of the FPGA manufacturer

	MENTOR GRAPHICS PRECISION	XILINX ISE
	LATTICE ISP LEVER	ACTEL LIBERO
	ALTERA QUARTUS	
		

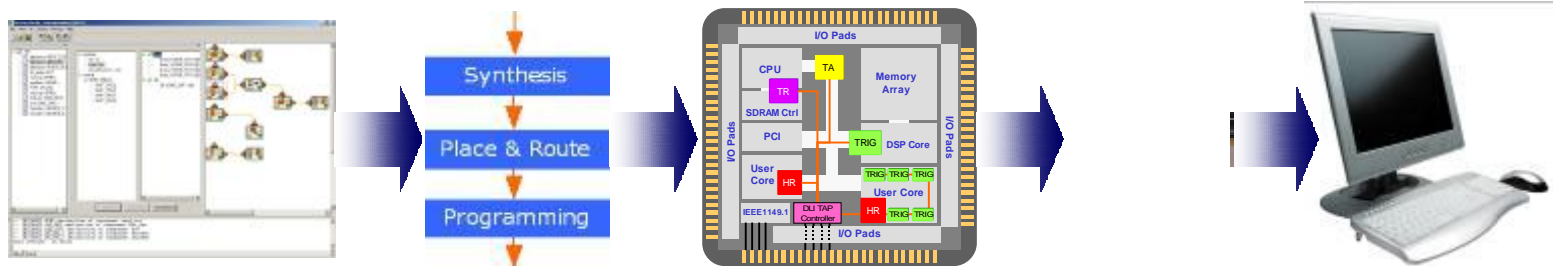
Support for Industry Standard Interfaces

- § DiaLite is based on popular Standards Verilog, VHDL, PSL, SVA, TCL, C++
- § Easy integration into any EDA environment using script and extended API
- § DCOM based client-server architecture (DiaServer), enable rapid third party integration



DiaLite Benefits & Value

- Powerful platform verification through hardware methodology
 - Complete solution of advanced techniques now available in hardware
- High performance verification fully leveraging hardware
 - No software verification environment running with emulator or prototype
- Easy to use, consistent throughout flow, debug & verification process
 - Works throughout existing flow, easy to use instrumentation and analysis



Package	Application	
DiaLite LeadingEdge	FPGA Design	
DiaLite PowerEdge	FPGA Design & SoC Prototyping	
DiaLite Platform	FPGA Design, SoC Prototyping & SoC Design	
Hardware Storage	All	

DiaLite Across Multiple Methodologies

DiaLite makes a powerful addition to multiple methodologies

FPGA Verification



Enable platform verification throughout design flow

HDL Debug Extension



Extend HDL debug into systems, hardware integration, FPGA

SoC Verification



Transform hardware software, design to integration, verification

Emulation / Rapid Prototyping Acceleration



Inline verification increases performance and functionality



Competitive Landscape

ON CHIP INSTRUMENTATION (FPGA) - COMPETITIVE MATRIX										
Competitive Matrix		Temento	Novas	Aldec	Mentor	Lattice	Altera	Xilinx	Synplificity	Actel
Validation & Verification	Assertion Checking o Hardware Assertion Instrumentation and Validation	DiaLite Platform								
Debug & Verification	Bus Analysis o ARM AHB Protocol o ARM AXI Protocol ¹ o OCP Protocol ¹ o IBM Core Connect ¹	All DiaLite	Debussy Verdi		Spiratech					
	RTL Debugger o C-Debugger Interface o State Machine Debugger	DiaLite Power Edge						Identify	Identify	Identify (AE)
Design Instrumentation	Instrumentation o Multi- Vendor FPGA Support o Multi Vendor Synthesis Support	DiaLite Leading Edge				ISP Tracy Reveal	SignalTap	ChipScope	Identify	Identify (AE)
Design Synthesis		Precision XST QUS Synplify		XST Precision Synplify	Precision	Precision Synplify	QIS	XST	Synplify	Synplify

Note 1 - Temento Development Roadmap

Multi-Vendor Support
Proprietary
Partial Solution



Temento is the only company with complete, portable solution

Customer Base

Canon

NEC

BAE SYSTEMS



Galileo Avionica



SUNPLUS

applications **pld**
Powerful Logic Design

SANYO OKI
PRINTING SOLUTIONS

AIRBUS

HITACHI
Inspire the Next

TOSHIBA

- 40 DiaLite Stations running
- Broad range of electronic segments covered
- Strong presence in Japan and Europe

Distribution Channels

