Make it easy
• Company Overview
• Dialite Products
• Competitive Analysis
• Customers
• Distribution Channels
## Temento Company History

### Temento History

<table>
<thead>
<tr>
<th>Year</th>
<th>Event</th>
</tr>
</thead>
<tbody>
<tr>
<td>1995</td>
<td>Company founded</td>
</tr>
<tr>
<td>1996</td>
<td>Test Services</td>
</tr>
<tr>
<td>1997</td>
<td>1 patent granted</td>
</tr>
<tr>
<td>2001</td>
<td>DiaTem Product Release</td>
</tr>
<tr>
<td>2003</td>
<td>DiaLite Product Release</td>
</tr>
<tr>
<td>2004</td>
<td>Sales Channel Formation</td>
</tr>
<tr>
<td>2005</td>
<td>Sales Ramp-up</td>
</tr>
<tr>
<td>2006</td>
<td>2 more patents granted</td>
</tr>
<tr>
<td>2007</td>
<td>DiaLite Power Edge</td>
</tr>
<tr>
<td>2008</td>
<td>DiaTem 3 release</td>
</tr>
<tr>
<td>2009</td>
<td>DiaLite 4.7 release</td>
</tr>
</tbody>
</table>

- Focus on the debug and verification of complex FPGA, SoC, and PCB designs
- 100 consumers and communications electronics customers worldwide
- Headquartered in Grenoble France, with sixteen, predominantly R&D, employees
- Unique core technology, three patents
- Two successful, mature product lines

**DiaTem**

The test and debug of complex PCBs

**DiaLite**

The verification and debug of FPGAs and SoCs post fabrication

**PATENTED TECHNOLOGY**
Diatem Lab is composed of 4 stations to test electronics boards throughout the product life cycle.

1. Test Development
   - Engineering Station
2. Test Plan
   - Industrialization Station
3. Test Execution
   - Production Station
4. Test Probe
   - Repair & Maintenance

A WorkStation running DiaTem
A Hardware JTAG Controller
Your Units Under Test

UUT 1
UUT 2
UUT 3
UUT 4
Traditional Logic Analysis Method

Dedicated pins connected to logic analyzer

- Requires extensive dedicated I/O for debug
  Driving signals to external I/O introduces additional problems
- Inflexible solution
  - Difficult or impossible to add additional debug pins if needed
- Limited visibility to on-chip activity

In System Debug Solution

Integrate a logic analyzer in the FPGA GIVES:
- Access to the complete data bus
- Access to all internal design nodes.
- Operates at the full system speed
- Synchronous to the design clock

AFTER DFT TECHNOLOGY ADOPTION

INSTRUMENTATION IS MOVING ON CHIP
Verification Needs Visibility

- FPGAs are getting bigger, faster, embed large busses, DSP cores, logic etc. Makes signals extraction infeasible!!

BOTTLENECK

- Packages are getting smaller with more pins, do not have exposed leads that can be physically probed!

BOTTLENECK

- Boards are getting smaller with more layers. Traces are often buried inside multi-layer printed circuit boards

Traditional methods run out of steam
No techniques on the market available to cover all corner cases you missed in simulation/emulation/on-chip verification & debugging tool
• Endless debug loop threatens time-to-market
• Dialite is the only commercial tool supporting all debug phases

DLI secures Functional Verification Sign-Off

Standard debug tools could never help closing debug phase. Errors in the field risk!!

Bugs

100%

Release
To end user

Assertion Verification
RTL Debug (Advanced)
Signal Debugging (basic)

Time

Free Tools

Competition
DiaLite Opportunity Throughout Platform Flow

**Prototyping / Emulation**
- **Market**: 3K projects
- **Issues**: External verification reduces performance of overall methodology
  - Testing and debugging design internals hard to execute

**FPGA-based Designs**
- **Market**: 20K design starts
- **Issues**: Controllability and observability of internal signals restrictive
  - Lack of effective verification methods e.g. no synthesizable assertions

**SoC Designs**
- **Market**: 3.7K design starts
- **Issues**: Design to integration flow disconnected, making debug torturous
  - System verification methods non-existent, complicating software hardware validation
IP instrumentation cores are inserted at the RTL level.
Create your Debug Project with graphic tools in just few clicks!

- Design Project Hierarchical levels and source files
- Instrumentation
- Signals to be instrumented
- Messages logging
- Signals of instruments

User Friendly Interface
A Collection of 14 Debug IPS

**Triggers**
- Parallel
- Serial
- Glitch Detector

**Pattern Generators**
- Switch & Leds
- Pseudo Random Generator

**Combinatory Logic**
- Logic Equation Module
- User Logical Module

**Analyzers/Bus Monitoring**
- Traffic Analyzer
- Bus Range Checker
- AHB Bus Tracer

**Recorders**
- History Register
- Transaction Register

**Verification Code Debug**
- HDL Fault Finder
- Assertion Checker
Traffic density on a bus, throughput measurements, statistics issues?
- Use the Traffic Analyzer!

Design robustness checking issue?
- Use the Pseudo Random Generator!

Synchronism test of sensitive signals (like IRQ) issue?
- Use the Glitch Detector!

Dedicated instruments needs?
- DLI provides the User Logical Module!

Temento Confidential
HDL Fault Finder expands debug productivity by providing a bridge between signals on silicon and RTL code!

- When a trigger condition happens, it becomes easy to find error into HDL code.

- Using HDL FF, you’re directly pointed to the error:

```
if state_register=st5 then
  if x_int='1' then
    state_register <= Failure;
    --z_int <= '0';
  else
    state_register <= success;
    --z_int <= '1';
  end if;
end if;
```

Use a Trigger as a Hardware Breakpoint in the HDL FF.
DiaLITE Power Edge & the HDL FF

Manage your IP Flow, Check the waves

Insert Watchpoints in manual or automatic mode

And Check in correlation...

HDL Code

User Defined Variables

Events
Hard/Soft Co-Debug is easily performed using DiaLite dedicated TAP option:

- Leave the native TAP to Soft Debug tools
- Use dedicated TAP (Altera, Xilinx) for DiaLite Instrumentation

- Link your C code to an HDL Debugger
- Increase performance of instrumentation monitoring
- Leave instruments in the production chip for acceptance or maintenance

Set up HW Trigger on CPU IT with DiaLite

HW Trigger halts CPU execution

Analyze Program execution in C Debugger
Definition: An Assertion is the execution of a Property, which itself can be seen as a fragment of an executable specification.

- The Assertion Checker (AC) IP imports the assertions & embeds them into your chip.
- DiaLite Platform is the ONLY one to use your formal properties written during System Specification and to:
  - Run them On Silicon
  - Run them At Speed
  - Get Real-Time feedback & coverage
Instrumentation for bus analysis and debug

SoC

Processor Core  On-Chip Memory  IP core #1  ...  IP core #N

AMBA On-Chip Bus

On-Chip Trace Memory  Bus Trace Analyzer  Bus Protocol Checker

EXTERNAL MEMORY

Bus Trace Analyzer

Host

Bus Protocol Checker (1)

Temento Confidential (1) under development
**INTEGRATED TRACE AND ANALYSIS SOLUTIONS FOR EMBEDDED PROCESSORS**

- **JTAG Interface**
  - User can setup the tracer through JTAG port

- **Signal Monitor & Tracing (Signal/Timing Abstraction)**
  - To determine when and which signals should be monitored

- **Trace Compression**
  - To compress the trace size generated from timing/signals abstraction module

- **Data Packing**
  - Packs the trace data generated from the data compression module and buffer the output data

- **Trace Output**
  - Transfers the trace data to host (PC)
  - Stored in/out on-chip memory
TemStorage frees the FPGA resources of your Debug project!

- Store large amount of Data outside your DUT and stream them to the Host PC through USB
- Seen in DLI as a Memory device for Test IPs working with RAM or Registers (like History or Transaction Registers)
- TemStorage parameters can be customized from DiaLite GUI
  - 1GB Memory / 220 data channels / 100 MHz on 128 channels (State Analysis)
Same Debug Possibilities whatever is your FPGA Manufacturer

Same Debug Possibilities whatever is your Design Flow Provider
- Start a project with a manufacturer, move to any other!
- Split it between several FPGA targets, DiaLite is Multi-FPGA compatible!
- DiaLite can run mixed VHDL / Verilog Designs
- Assertions can be written in PSL or SVA

Possibility to use a dedicated or the native TAP of the FPGA manufacturer
DiaLite is based on popular Standards Verilog, VHDL, PSL, SVA, TCL, C++

- Easy integration into any EDA environment using script and extended API
- DCOM based client-server architecture (DiaServer), enable rapid third party integration
DiaLite Benefits & Value

- Powerful platform verification through hardware methodology
  - Complete solution of advanced techniques now available in hardware
- High performance verification fully leveraging hardware
  - No software verification environment running with emulator or prototype
- Easy to use, consistent throughout flow, debug & verification process
  - Works throughout existing flow, easy to use instrumentation and analysis

<table>
<thead>
<tr>
<th>Package</th>
<th>Application</th>
</tr>
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<tbody>
<tr>
<td>DiaLite LeadingEdge</td>
<td>FPGA Design</td>
</tr>
<tr>
<td>DiaLite PowerEdge</td>
<td>FPGA Design &amp; SoC Prototyping</td>
</tr>
<tr>
<td>DiaLite Platform</td>
<td>FPGA Design, SoC Prototyping &amp; SoC Design</td>
</tr>
<tr>
<td>Hardware Storage</td>
<td>All</td>
</tr>
</tbody>
</table>
DiaLite Across Multiple Methodologies

DiaLite makes a powerful addition to multiple methodologies

FPGA Verification
Enable platform verification throughout design flow

HDL Debug Extension
Extend HDL debug into systems, hardware integration, FPGA

SoC Verification
Transform hardware software, design to integration, verification

Emulation / Rapid Prototyping Acceleration
Inline verification increases performance and functionality
## Competitive Landscape

### ON CHIP INSTRUMENTATION (FPGA) - COMPETITIVE MATRIX

<table>
<thead>
<tr>
<th>Competitive Matrix</th>
<th>Temento</th>
<th>Novas</th>
<th>Aldec</th>
<th>Mentor</th>
<th>Lattice</th>
<th>Altera</th>
<th>Xilinx</th>
<th>Synplicity</th>
<th>Actel</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Validation &amp; Verification</strong></td>
<td>Assertion Checking o Hardware Assertion Instrumentation and Validation</td>
<td>DiaLite Platform</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Debug &amp; Verification</strong></td>
<td>Bus Analysis o ARM AHB Protocol o ARM AXI Protocol o OCP Protocol o IBM Core Connect</td>
<td>All DiaLite</td>
<td>Debussy Verdi</td>
<td>Spiratech</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>RTL Debugger</strong></td>
<td>o C-Debugger Interface o State Machine Debugger</td>
<td>DiaLite Power Edge</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Design Instrumentation</strong></td>
<td>Instrumentation o Multi-Vendor FPGA Support o Multi Vendor Synthesis Support</td>
<td>DiaLite Leading Edge</td>
<td>ISPT Tracy</td>
<td>SignalTap</td>
<td>ChipScope</td>
<td>Identify</td>
<td>Identify</td>
<td>Identify (AE)</td>
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<tr>
<td><strong>Design Synthesis</strong></td>
<td>Precision XST QUS Synplify</td>
<td>XST Precision Synplify</td>
<td>Precision</td>
<td>Precision Synplify</td>
<td>QIS</td>
<td>XST</td>
<td>Synplify</td>
<td>Synplify</td>
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**Note 1 - Temento Development Roadmap**

Multi-Vendor Support
- Proprietary
- Partial Solution

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Temento is the only company with complete, portable solution
Customer Base

- 40 DiaLite Stations running
- Broad range of electronic segments covered
- Strong presence in Japan and Europe