Temento systems

DiaLite INSTRUMENTATION

Make it easy

Agenda

- Company Overview
- Dialite Products
- Competitive Analysis
- Customers
- Distribution Channels

Temento Company History

Temento History

1995	Company founded
1996	Test Services
1997	1 patent granted
2001	DiaTem Product Release
2003	DiaLite Product Release
2004	Sales Channel Formation
2005	Sales Ramp-up
2006	2 more patents granted
2007	DiaLite Power Edge
2008	DiaTem 3 release
2009	DiaLite 4.7 release

- Focus on the debug and verification of complex FPGA, SoC, and PCB designs
- 100 consumers and communications electronics customers worldwide
- Headquartered in Grenoble France, with sixteen, predominantly R&D, employees
- Unique core technology, three patents
- Two successful, mature product lines

DiaTem®

The test and debug of complex PCBs

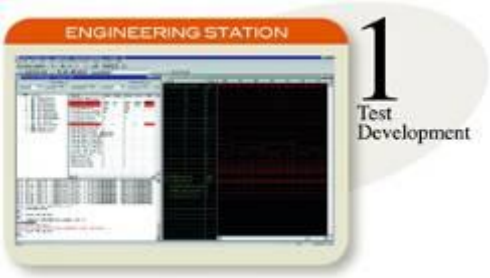
DiaLite INSTRUMENTATION

The verification and debug of FPGAs and SoCs post fabrication

PATENTED TECHNOLOGY

Diatem Overview

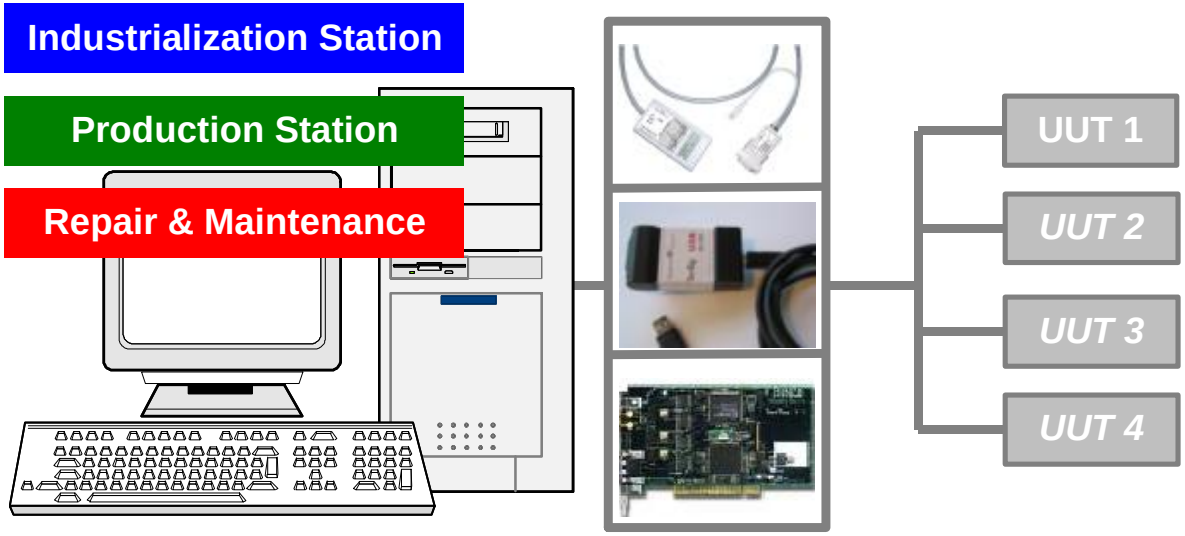
Innovative Provider of Debug and Verification Solutions



Diatem Lab is composed of 4 stations to test electronics boards throughout the product life cycle

A WorkStation running DiaTem	A Hardware JTAG Controller	Your Units Under Test

- Engineering Station
- Industrialization Station
- Production Station
- Repair & Maintenance



Temento systems

Temento systems

DiaLite INSTRUMENTATION

Make it easy

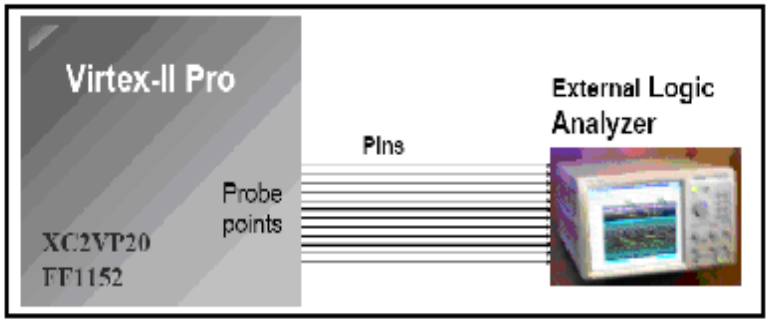
Traditional Logic methods Replaced With In system Debug Solutions

AFTER DFT TECHNOLOGY ADOPTION

INSTRUMENTATION IS MOVING ON CHIP

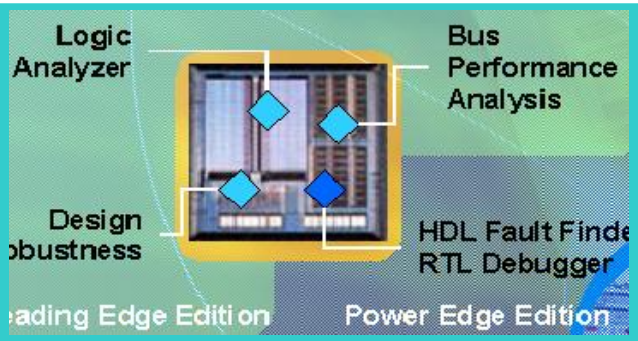
Traditional Logic Analysis Method

Dedicated pins connected to logic analyzer



- Requires extensive dedicated I/O for debug
  - Driving signals to external I/O introduces additional problems
- Inflexible solution
  - Difficult or impossible to add additional debug pins if needed
- Limited visibility to on-chip activity

In System Debug Solution



Integrate a logic analyzer in the FPGA GIVES:

- **Access to the complete data bus**
- **Access to all internal design nodes.**
- **Operates at the full system speed**
- **synchronous the the design clock**

Verification Needs Visibility

- **FPGAS ARE GETTING BIGGER, FASTER, EMBED LARGE BUSSES, DSP CORES, LOGIC ETC.. MAKES SIGNALS EXTRACTION INFEASIBLE!!**

BOTTLENECK

- **PACKAGES ARE GETTING SMALLER WITH MORE PINS, DO NOT HAVE EXPOSED LEADS THAT CAN BE PHYSICALLY PROBED!**

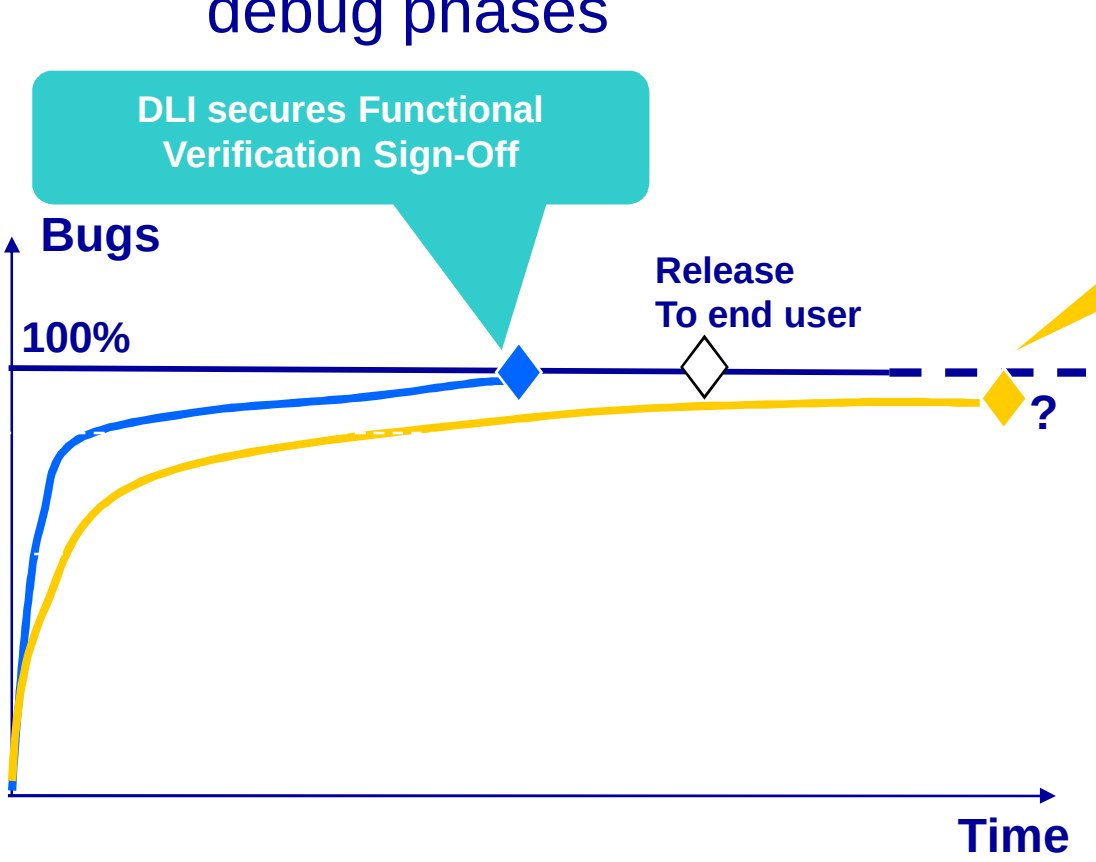
BOTTLENECK

- **BOARDS ARE GETTING SMALLER WITH MORE LAYERS. TRACES ARE OFTEN BURIED INSIDE MULTI-LAYER PRINTED CIRCUIT BOARDS**

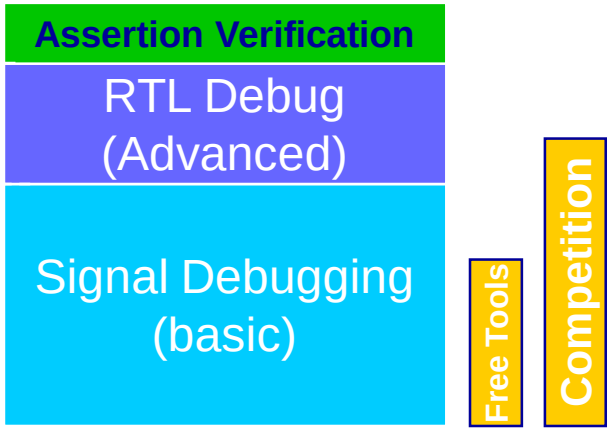
TRADITIONAL METHODS RUN OUT OF STEAM
NO TECHNIQUES ON THE MARKET AVAILABLE TO COVER ALL CORNER CASES YOU MISSED IN SIMULATION/EMULATIONON-CHIP VERIFICATION & DEBUGGING TOOL

Dialite Key Benefit

- Endless debug loop threatens time-to-market
- Dialite is the only commercial tool supporting all debug phases



Standard debug tools could never help closing debug phase Errors in the field risk !!



DiaLite Opportunity Throughout Platform Flow

Design Progression

Prototyping / Emulation

Market

- 3K projects

Issues

- External verification reduces performance of overall methodology
- Testing and debugging design internals hard to execute

FPGA-based Designs

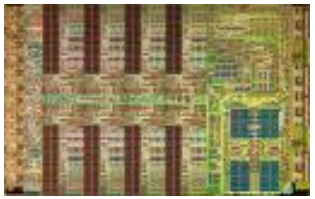
Market

- 20K design starts

Issues

- Controllability and observability of internal signals restrictive
- Lack of effective verification methods e.g. no synthesizable assertions

SoC Designs



Market

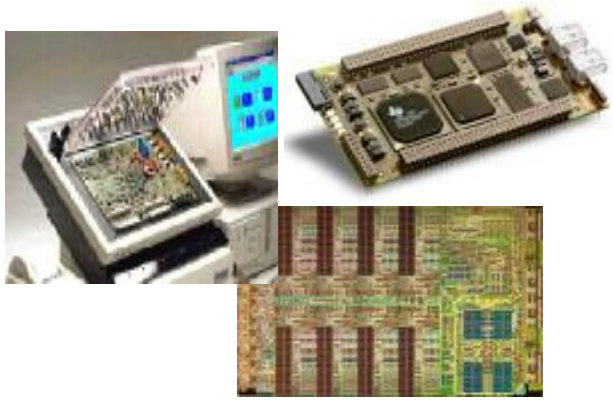
- 3.7K design starts

Issues

- Design to integration flow disconnected, making debug torturous
- System verification methods non-existent, complicating software hardware validation

Temento systems

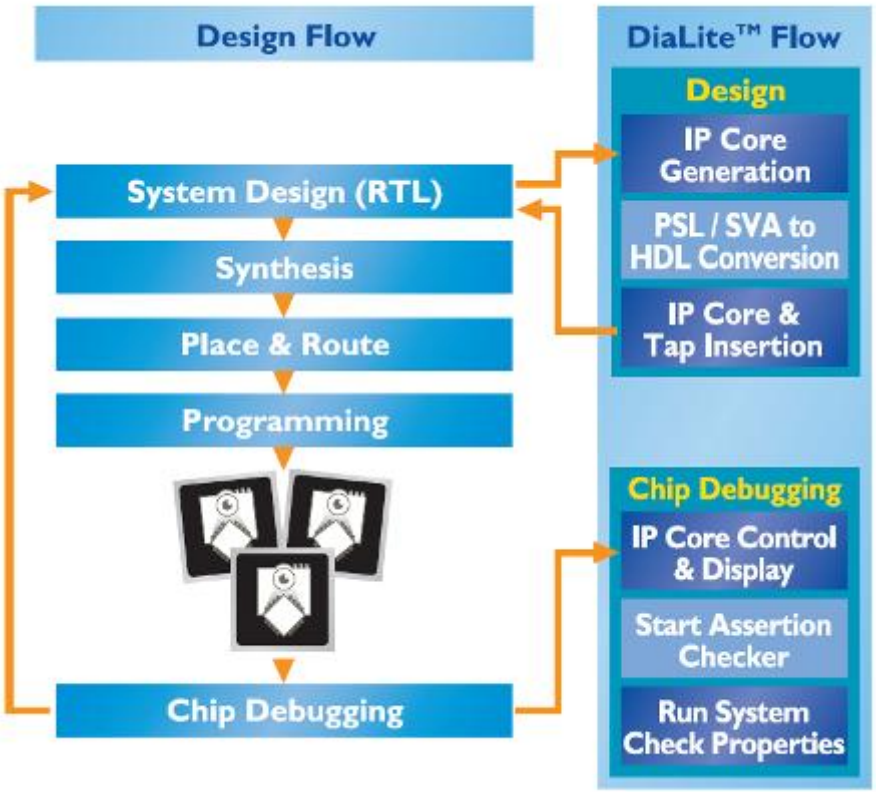
Tremento systems

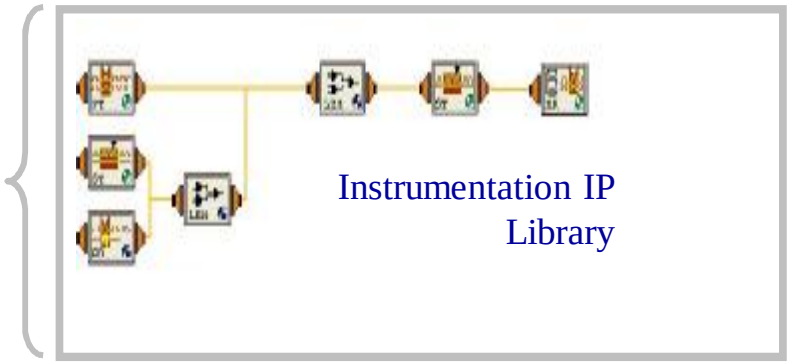


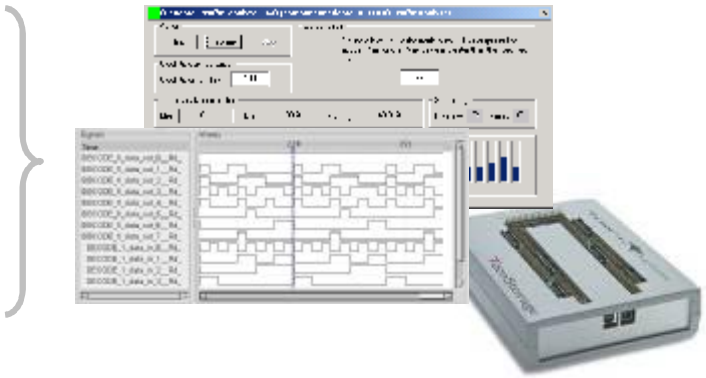
DiaLite INSTRUMENTATION

DiaLite Design Flow

IP instrumentation cores are inserted at the RTL level.

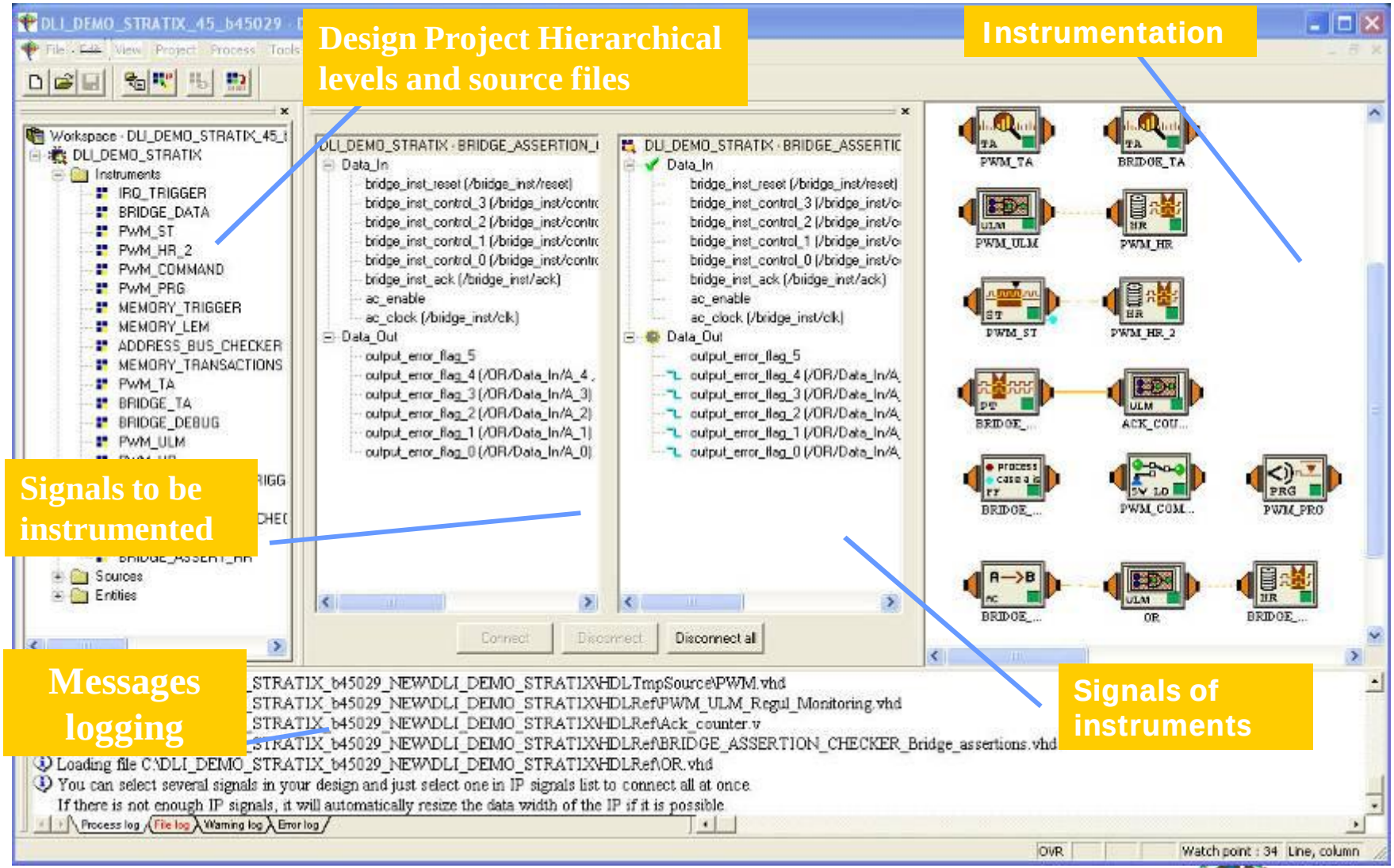






User Friendly Interface

§ Create your Debug Project with graphic tools in just few clicks !



Dialite Instruments Portfolio

Innovative Provider of Debug and Verification Solutions

A Collection of 14 Debug IPS

Triggers

Parallel

Serial

Glitch Detector

Pattern Generators

Switch & Leds

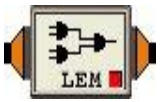
Pseudo Random Generator

Recorders

History Register

Transaction Register

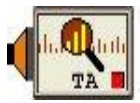
Combinatory Logic



Logic Equation Module

User Logical Module

Analyzers/Bus Monitoring



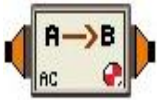
Traffic Analyzer

Bus Range Checker

AHB Bus Tracer

Verification Code Debug

HDL Fault Finder



Assertion Checker

Temento systems

An Instrument for each Issue

§ ***Traffic density on a bus, throughput measurements, statistics issues ?***

- Use the Traffic Analyzer !

§ ***Design robustness checking issue ?***

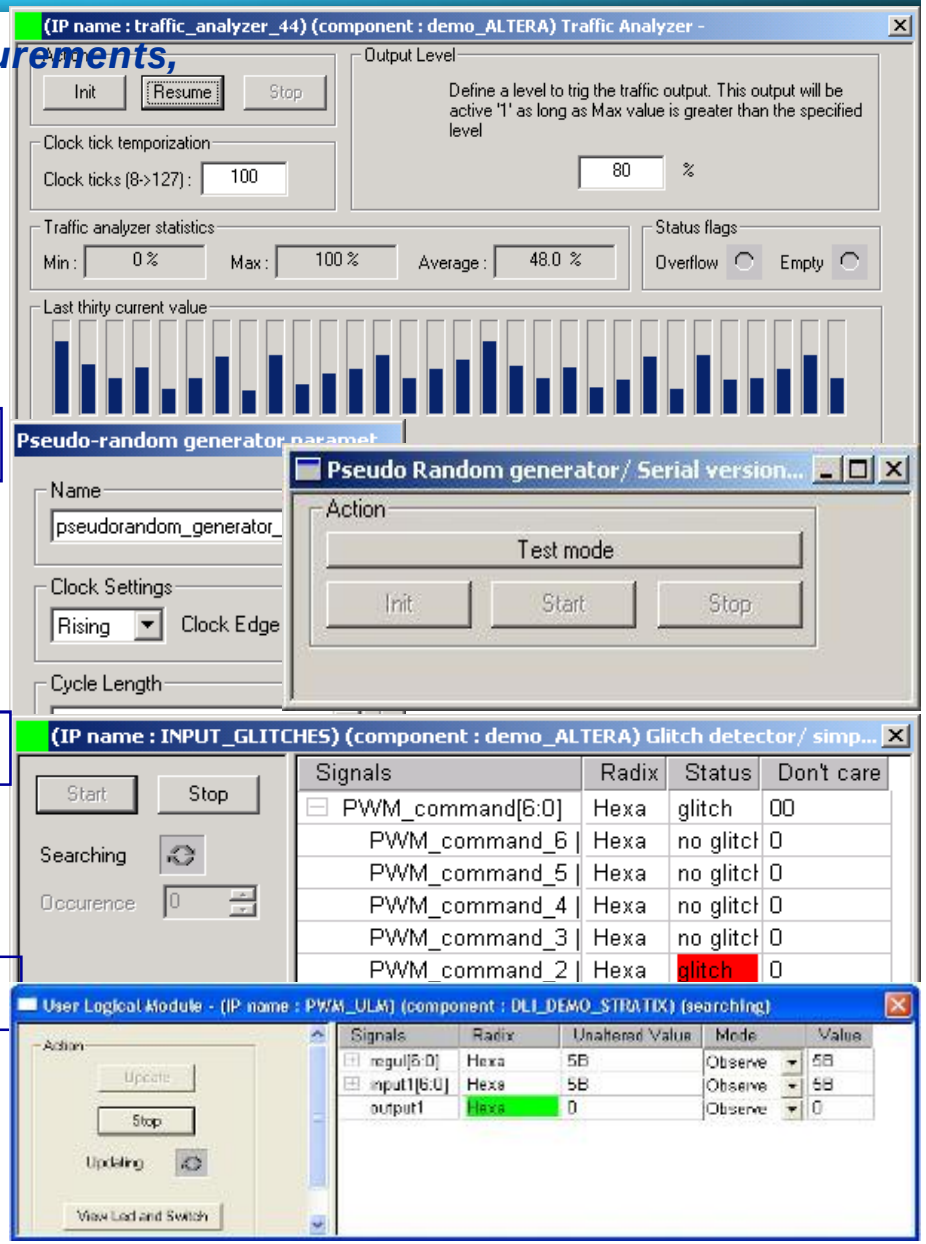
- Use the Pseudo Random Generator !

§ ***Synchronism test of sensitive signals (like IRQ) issue ?***

- Use the Glitch Detector !

§ ***Dedicated instruments needs ?***

- DLI provides the User Logical Module !

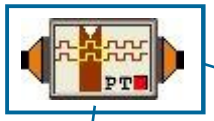


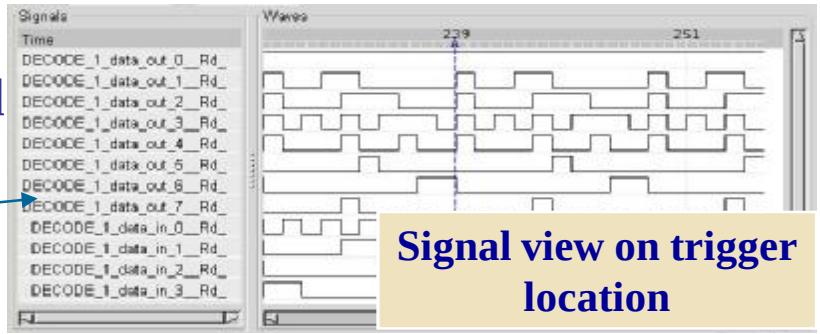
DiaLite Power Edge & the HDL FF

§ **HDL Fault Finder expands debug productivity by providing a bridge between signals on silicon and RTL code!**

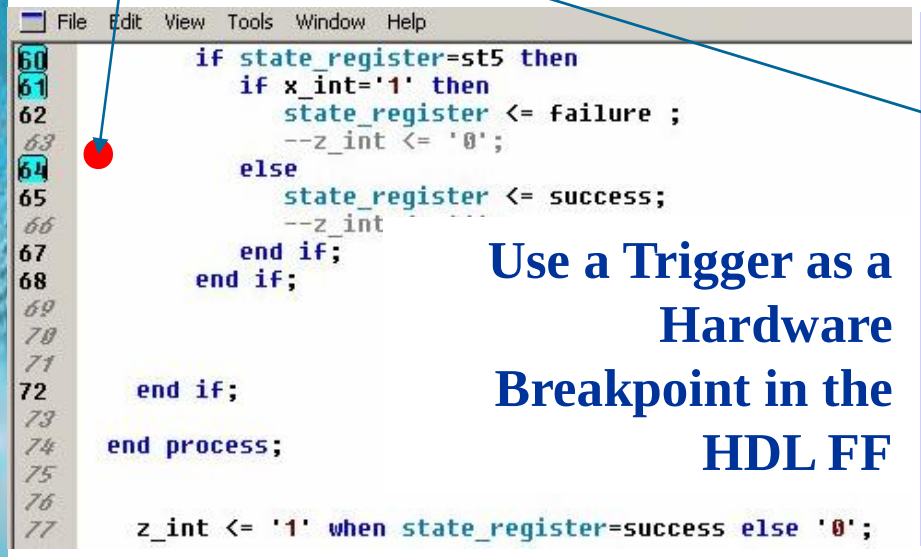
- **When a trigger condition happens, it becomes easy to find error into HDL code**

- **Using HDL FF, you're directly pointed to the error :**

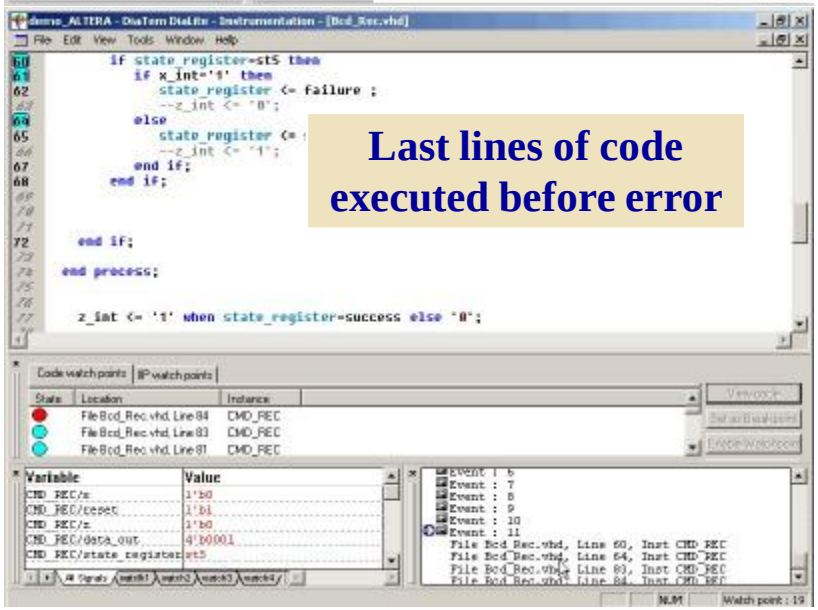




Signal view on trigger location

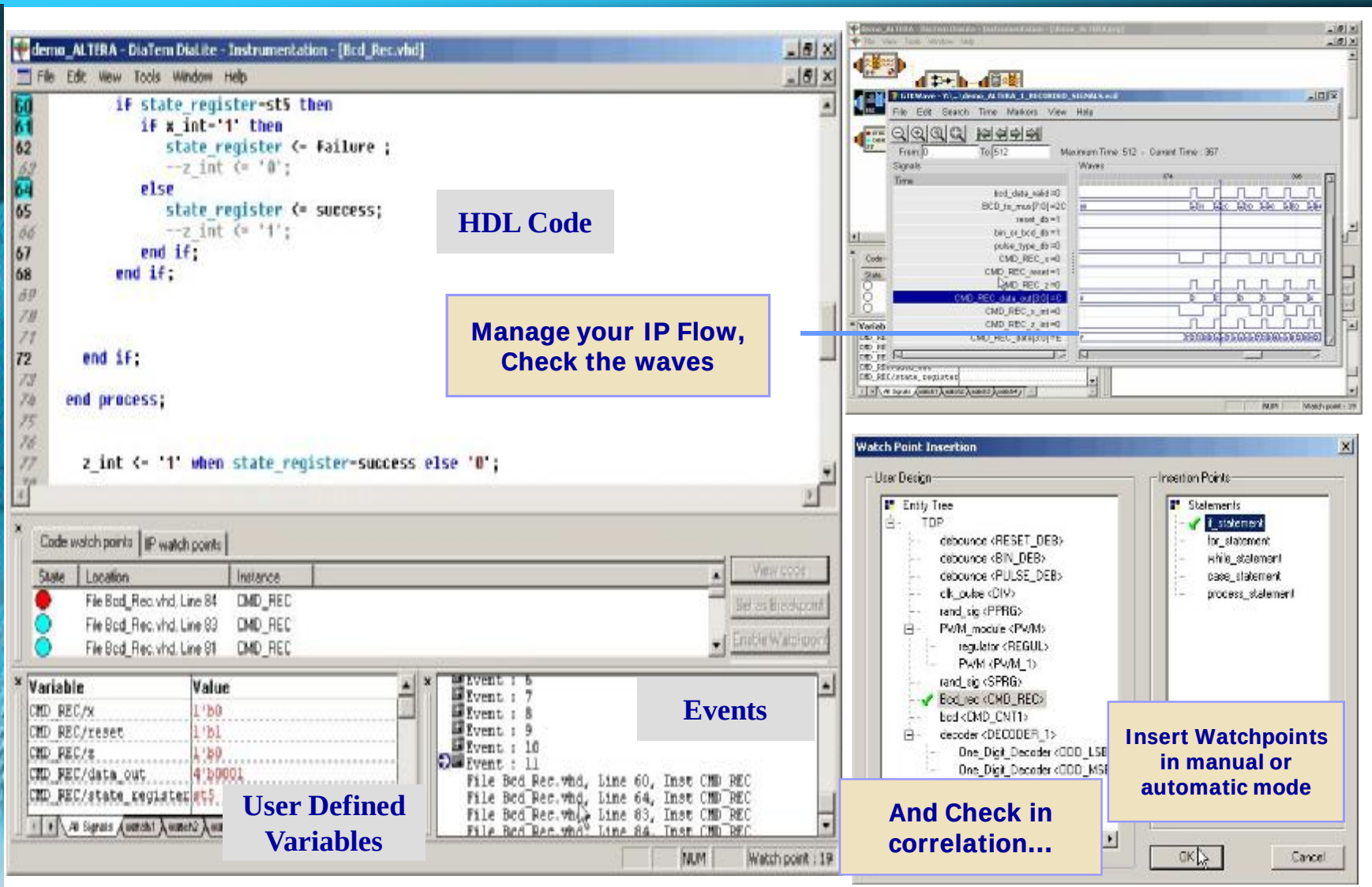


Use a Trigger as a Hardware Breakpoint in the HDL FF



Last lines of code executed before error

DiaLite Power Edge & the HDL FF



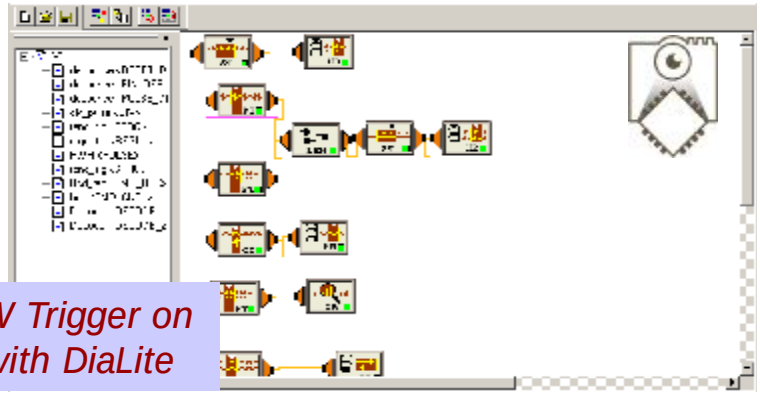
Innovative Provider of Debug and Verification Solutions

Temento systems

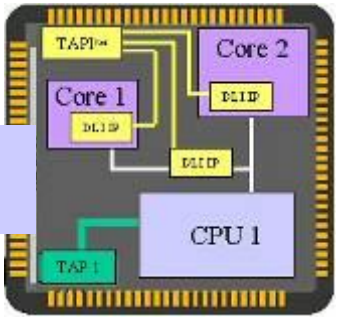
Hard / Soft Co-Debug

§ Hard/Soft Co-Debug is easily performed using DiaLite dedicated TAP option :

- Leave the native TAP to Soft Debug tools
- Use dedicated TAP (Altera, Xilinx) for DiaLite Instrumentation



Set up HW Trigger on CPU IT with DiaLite

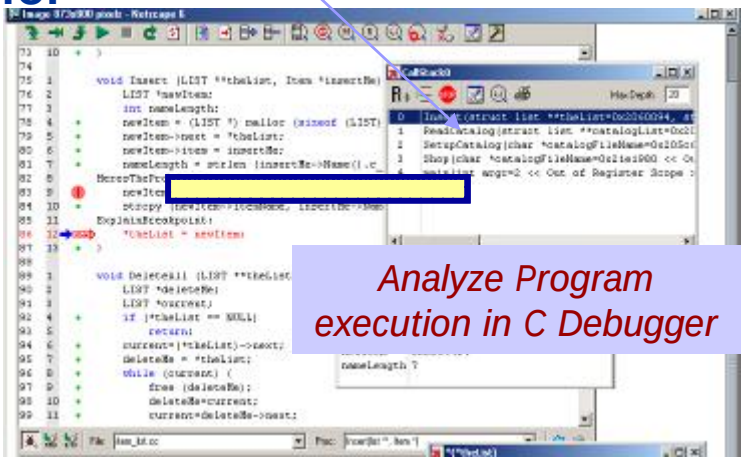


HW Trigger halts CPU execution

§ Link your C code to an HDL Debugger

§ Increase performance of instrumentation monitoring

§ Leave instruments in the production chip for acceptance or maintenance



Analyze Program execution in C Debugger

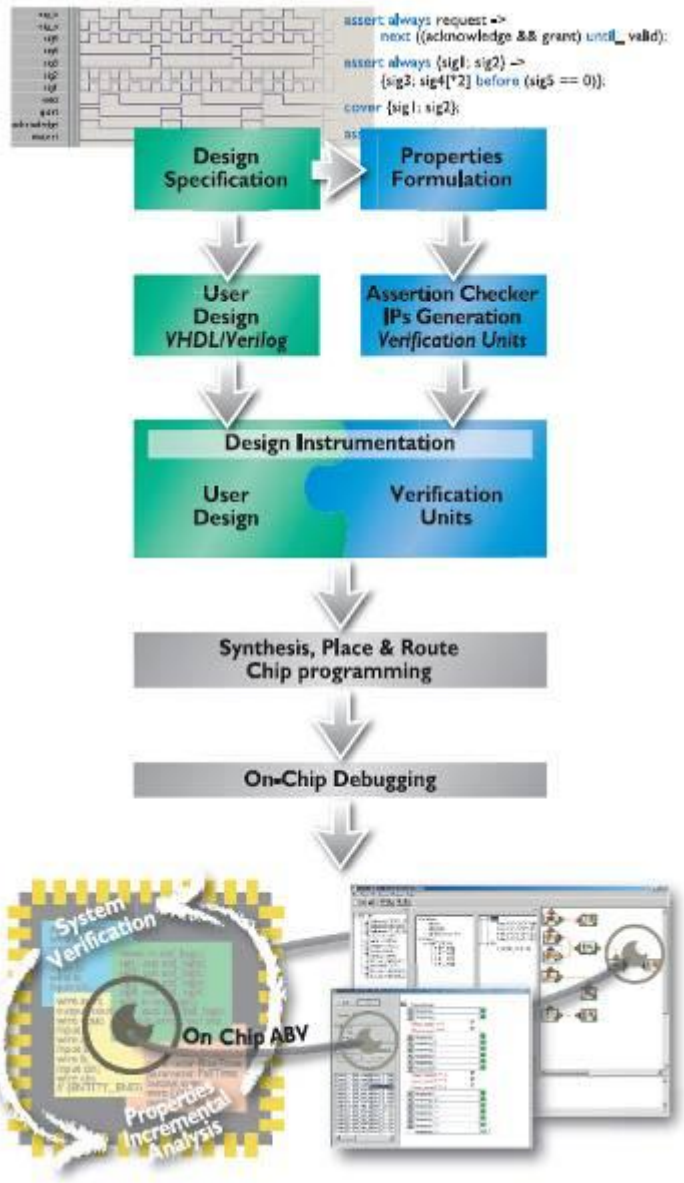
DiaLite Platform & the AC

Definition: An Assertion is the execution of a Property, which itself can be seen as a fragment of an executable specification

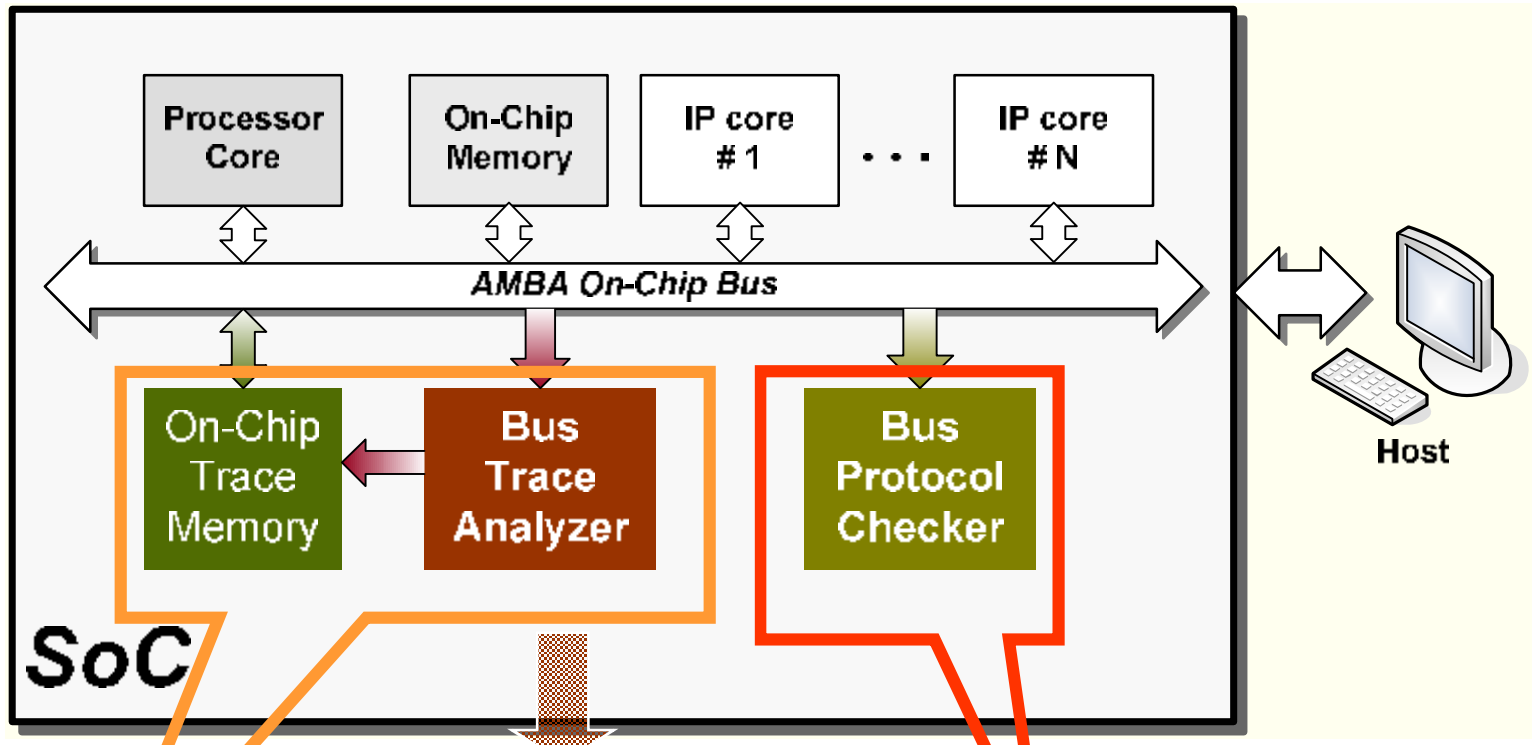
§ The Assertion Checker (AC) IP imports the assertions & embeds them into your chip

§ DiaLite Platform is the ONLY one to use your formal properties written during System Specification and to :

- § Run them On Silicon
- § Run them At Speed
- § Get Real-Time feedback & coverage



Instrumentation for bus analysis and debug

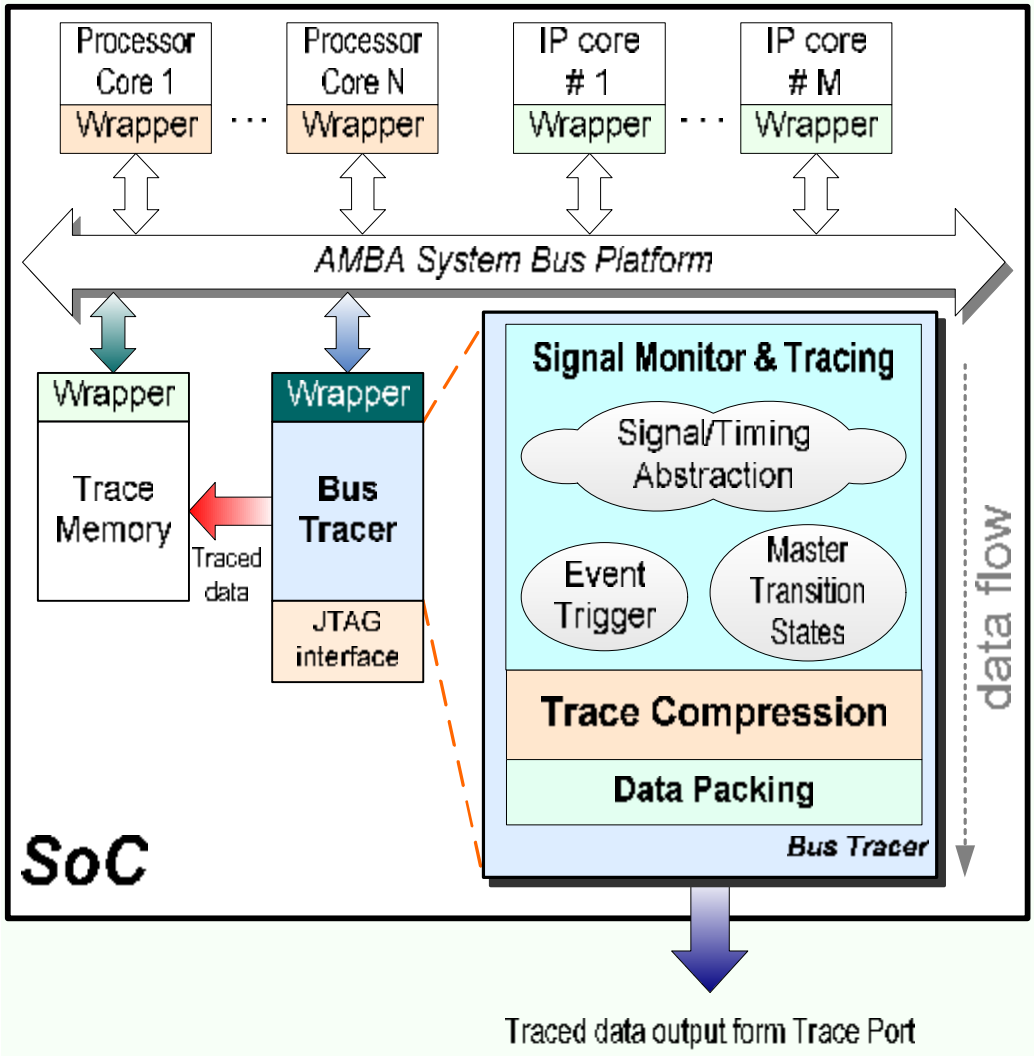


Bus Trace Analyzer

Bus Protocol Checker (1)

(1) under development

INTEGRATED TRACE AND ANALYSIS SOLUTIONS FOR EMBEDDED PROCESSORS

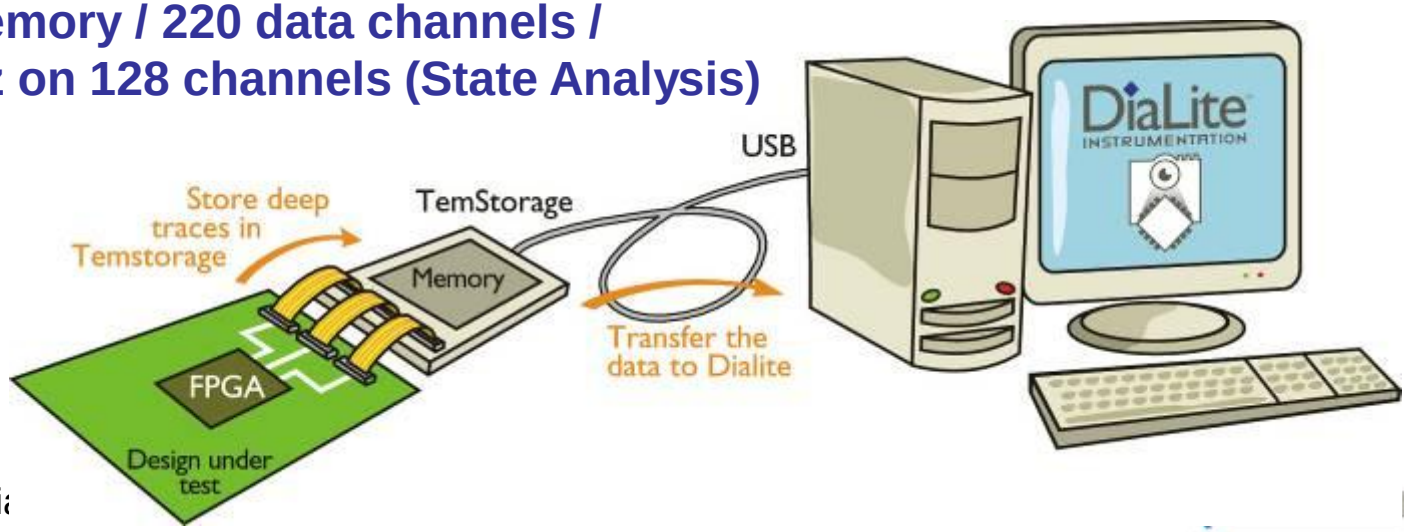


- **JTAG Interface**
  - **user can setup the tracer through JTAG port**
- **Signal Monitor & Tracing (Signal/Timing Abstraction)**
  - **to determine when and which signals should be monitored**
- **Trace Compression**
  - **to compress the trace size generated from timing/signals abstraction module**
- **Data Packing**
  - **packs the trace data generated from the data compression module and buffer the output data**
- **Trace Output**
  - **transfers the trace data to host (PC)**
  - **Stored in/out on-chip memory**

TemStorage & Off-Chip Data Record

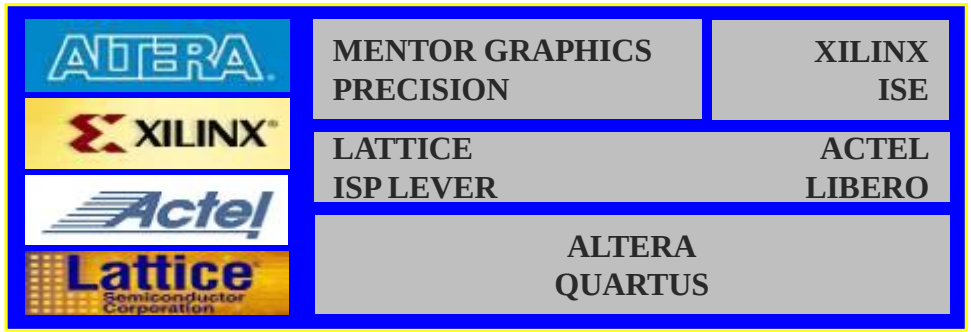
§ **TemStorage frees the FPGA resources of your Debug project !**

- **Store large amount of Data outside your DUT and stream them to the Host PC through USB**
- **Seen in DLI as a Memory device for Test IPs working with RAM or Registers (like History or Transaction Registers)**
- **TemStorage parameters can be customized from DiaLite GUI**
  - **1GB Memory / 220 data channels /**
  - **100 MHz on 128 channels (State Analysis)**



Device Independence

- Same Debug Possibilities whatever is your FPGA Manufacturer
- Same Debug Possibilities whatever is your Design Flow Provider
  - Start a project with a manufacturer, move to any other !
  - Split it between several FPGA targets, DiaLite is Multi-FPGA compatible !
  - DiaLite can run mixed VHDL / Verilog Designs
  - Assertions can be written in PSL or SVA
- Possibility to use a dedicated or the native TAP of the FPGA manufacturer

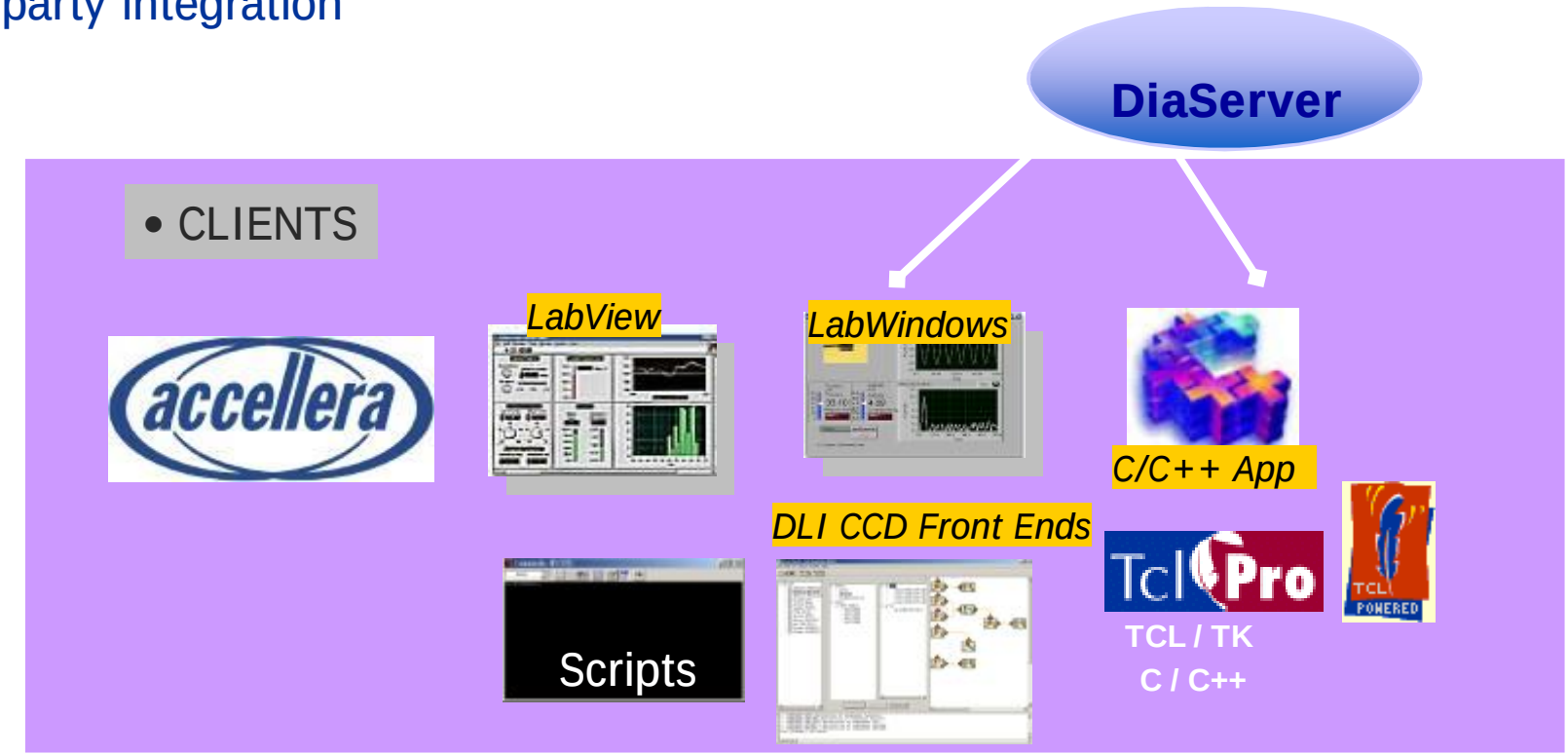


Support for Industry Standard Interfaces

§ DiaLite is based on popular Standards Verilog, VHDL, PSL, SVA, TCL, C++

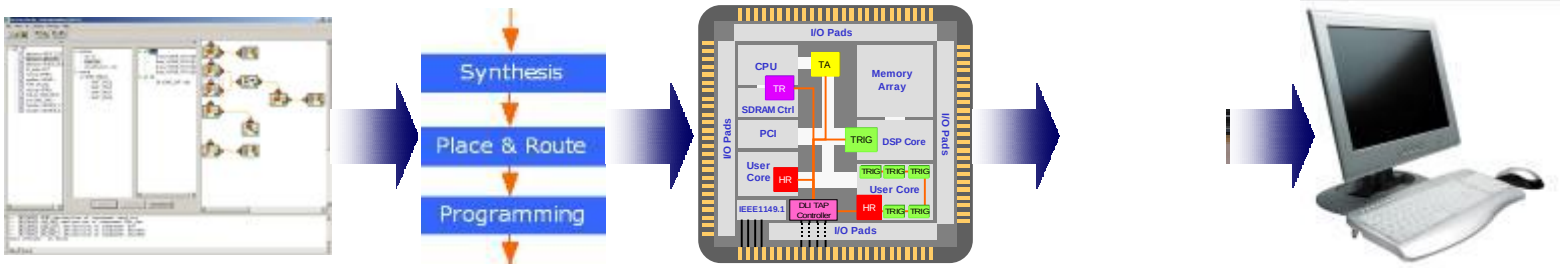
§ Easy integration into any EDA environment using script and extended API

§ DCOM based client-server architecture (DiaServer), enable rapid third party integration



DiaLite Benefits & Value

- Powerful platform verification through hardware methodology
  - Complete solution of advanced techniques now available in hardware
- High performance verification fully leveraging hardware
  - No software verification environment running with emulator or prototype
- Easy to use, consistent throughout flow, debug & verification process
  - Works throughout existing flow, easy to use instrumentation and analysis



Package	*Application*	
DiaLite LeadingEdge	FPGA Design	
DiaLite PowerEdge	FPGA Design & SoC Prototyping	
DiaLite Platform	FPGA Design, SoC Prototyping & SoC Design	
Hardware Storage	All	

DiaLite Across Multiple Methodologies

DiaLite makes a powerful addition to multiple methodologies

FPGA Verification

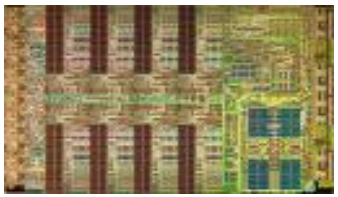
Enable platform verification throughout design flow

HDL Debug Extension

Extend HDL debug into systems, hardware integration, FPGA

DiaLite INSTRUMENTATION

SoC Verification



Transform hardware software, design to integration, verification

Emulation / Rapid Prototyping Acceleration

Inline verification increases performance and functionality

Temento systems

Competitive Landscape

ON CHIP INSTRUMENTATION (FPGA) - COMPETITIVE MATRIX

Competitive Matrix		Temento	Novas	Aldec	Mentor	Lattice	Altera	Xilinx	Synplicity	Actel
Validation & Verification	Assertion Checking o Hardware Assertion Instrumentation and Validation	DiaLite Platform								
Debug & Verification	Bus Analysis o ARM AHB Protocol o ARM AXI Protocol[1] o OCP Protocol[1] o IBM Core Connect[1]	All DiaLite	Debussy Verdi		Spiratech					
	RTL Debugger o C-Debugger Interface o State Machine Debugger	DiaLite Power Edge						Identify	Identify	Identify (AE)
Design Instrumentation	Instrumentation o Multi- Vendor FPGA Support o Multi Vendor Synthesis Support	DiaLite Leading Edge				ISP Tracy Reveal	SignalTap	ChipScope	Identify	Identify (AE)
Design Synthesis		Precision XST QUS Synplify		XST Precision Synplify	Precision	Precision Synplify	QIS	XST	Synplify	Synplify

Note 1 - Temento Development Roadmap

Multi-Vendor Support
Proprietary
Partial Solution

Temento is the only company with complete, portable solution

Temento systems

Customer Base

Canon

NEC

BAE SYSTEMS

Galileo Avionica

SUNPLUS

applications
>Powerful Logic Design
pld

SANYO

OKI
PRINTING SOLUTIONS

AIRBUS

HITACHI
Inspire the Next

TOSHIBA

- **40 DiaLite Stations running**
- **Broad range of electronic segments covered**
- **Strong presence in Japan and Europe**

Distribution Channels