CharFlo-Cell!™

Next-Generation Solution for Characterizing and Modeling Standard Cell and I/O Library

Agenda

- Introduction
- The Flow of CharFlo-Cell!
- The Applications and Features
- BiSection Methods for Setup/Hold Time
- Timing and Power models
- IBIS models
- CCS and ECSM models
- Building New .Lib for Custom Cells
- Validating Present .Lib for Existed Cells
- Conclusion

Legend’s Products

- IP Library Characterization/Verification Products
  - Charflo-Cell!™ : *Automatic Cell/IO Library Characterization*
  - Model Diagnoser™: *Cell Library QA, Diagnosis and Debugging*
  - Charflo-Memory!™: *Automatic Memory Characterization*
- Circuit Simulation Products
  - MSIM®: *Accurate-Spice Simulator for Analog/RF/Mixed-Signal IC and IP, LCD, and PCB/IBIS/Package*
  - PCB Design Manager: *Integrated Schematic & Simulation Environment with Test Bench Automation*
  - Turbo-MSIM™: *Fast-Spice Simulator*

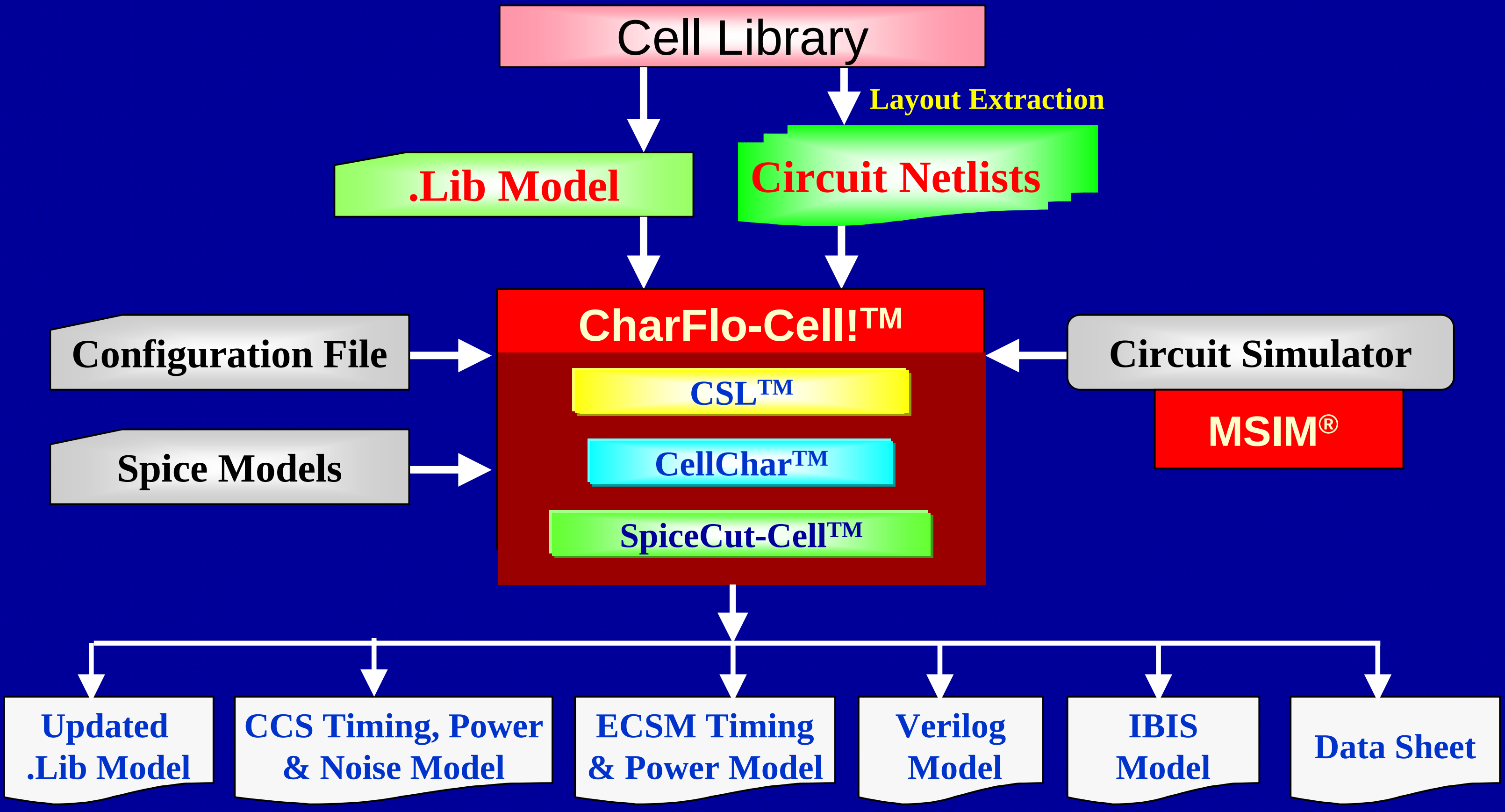
Inputs and Outputs

CharFlo-Cell!™

- **Inputs**
  - Existing Liberty (.lib) models
  - Layout-extracted cell netlists
  - Spice models
  - Configuration file (.csl)
- **Outputs**
  - Updated Liberty (.lib) models
  - Timing, power and noise models
  - CCS and ECSM models
  - SPDM table expansion, and monotonic modeling option
  - Verilog models
  - Reports and data sheet

The Characterization Flow

CharFlo-Cell!™



Technology Leader in IP Characterization and IC/PCB Simulation

Legend Design Technology

The Engines

CharFlo-Cell!™

- **CSL™ :**

  Automate the cell library characterization through programmable setup for '.Lib-in and .Lib-out'

- **SpiceCut-Cell™ :**

  Analyze the inside of cell for electrical verification, function validation and circuit partition

- **CellChar™ :**

  Perform cell library characterization with reliability check

SpiceCut-Cell Functions

CharFlo-Cell!™

- Locate the high-risk nodes inside the cells to monitor for ensuring the modeling quality
  - Example: Watch glitch and meta-stability on those internal nodes.
- Locate the appropriate nodes inside the cells to measure for enabling complex I/O cell characterization
  - Example: Measure pre-stage node of tri-state output
- Partition the cell to channel-connected block (CCB) for CCS noise model

Major Applications

CharFlo-Cell!™

- Library characterization
  - Standard cells and custom cells
  - I/O pads and complex cells
- Migration to new technology corners
  - Foundry to foundry
  - Process, Voltage and Temperature (PVT) variations

BiSection Method

Characterize Setup and Hold Time

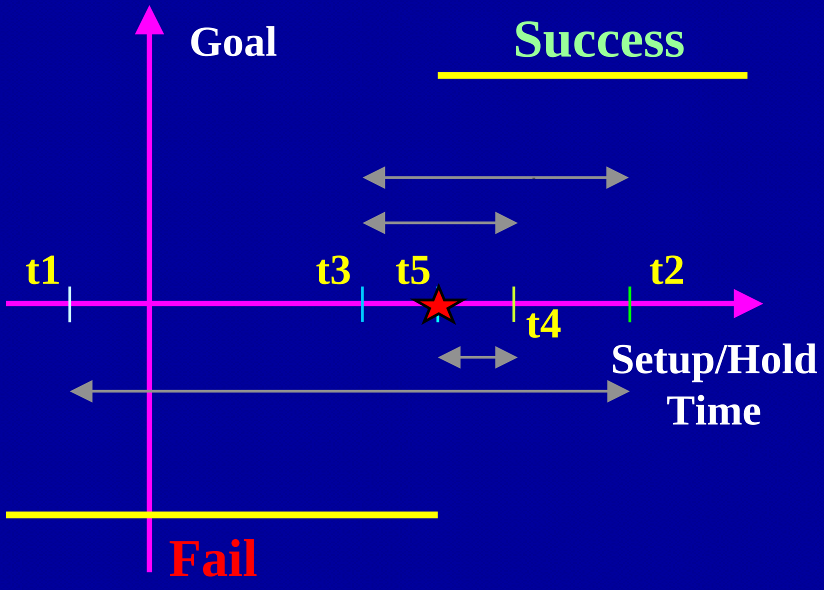
Setup and hold time characterization is based upon 'binary search' algorithm, i.e. BiSection method. The convergence will be controlled by the 'BiSect Error'

t1	Start
t2	Start

t3 = (t1 + t2) / 2

t4 = (t2 + t3) / 2

t5 = (t3 + t4) / 2



Time	Goal	BiSect Error
t1	Fail	
t2	Success	Norm(t2-t1)
t3	Fail	Norm(t3-t2)
t4	Success	Norm(t4-t3)
t5	Success	Norm(t5-t4)

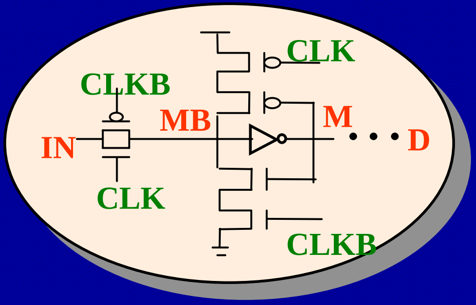
BiSection Methods

CharFlo-Cell!™

- Standard BiSection method
  - Based on ‘function’ success
  - Fast and simple
- Advanced BiSection method
  - Multi-goals BiSection based on
    - Success on output pins’ function, and
    - Success on internal nodes’ signal integrity
  - Setup/hold time are more conservative to make sure no glitch and meta-stability issues

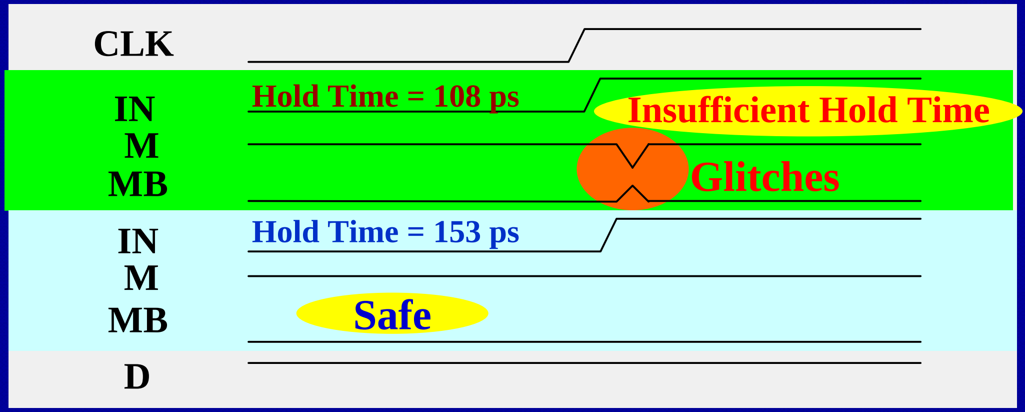
Prevent Glitch/Meta-Stability

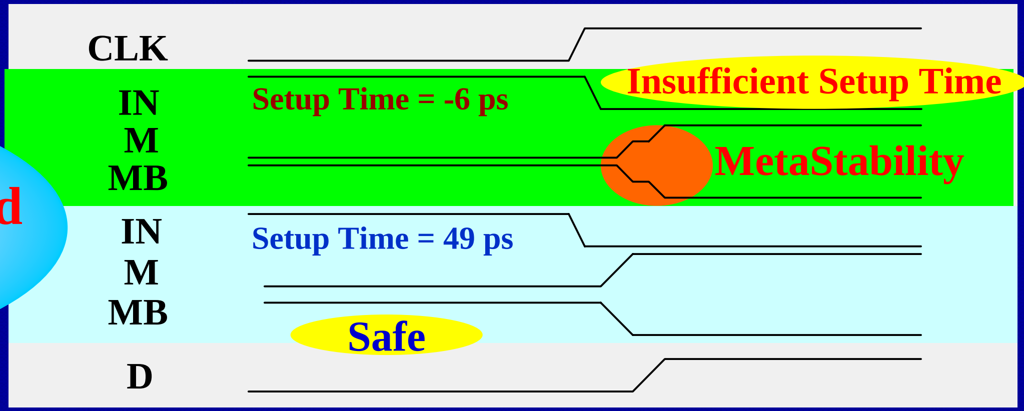
Advanced BiSection Method



Reliability Problem !

CharFlo-Cell!™ locates 'glitch-free' and 'meta-stability-free' setup/hold time





Legend Design Technology

The Features

CharFlo-Cell!™

- Reliability and manufacturability aware
  - Built-in SpiceCut to locate high-risk nodes inside cell
  - Monitor glitches/meta-stability during characterization
- Automatic setup for the characterization
  - Stimulus generation from functions or state-tables
  - Control generation from existing setup or adding new entries and options
  - Database generation for flexible outputs
- Distributed processing with multiple CPUs

Cell Types Supported

By CharFlo-Cell!™

- Single and multi-output combinational cells
- Complex latches and flip-flops
- I/O pads and Tri-state cells
- I/O cells with multiple voltage supplies
- I/O cells with differential inputs/outputs
- Special cells

Complex I/O Cell

Characterization by CharFlo-Cell!^{TM}

- Customize the measurements intelligently
- Enhance the configurations for simulation convergence
- Facilitate the measurements on internal node recognized by circuit pattern
- Renovate the characterization algorithms

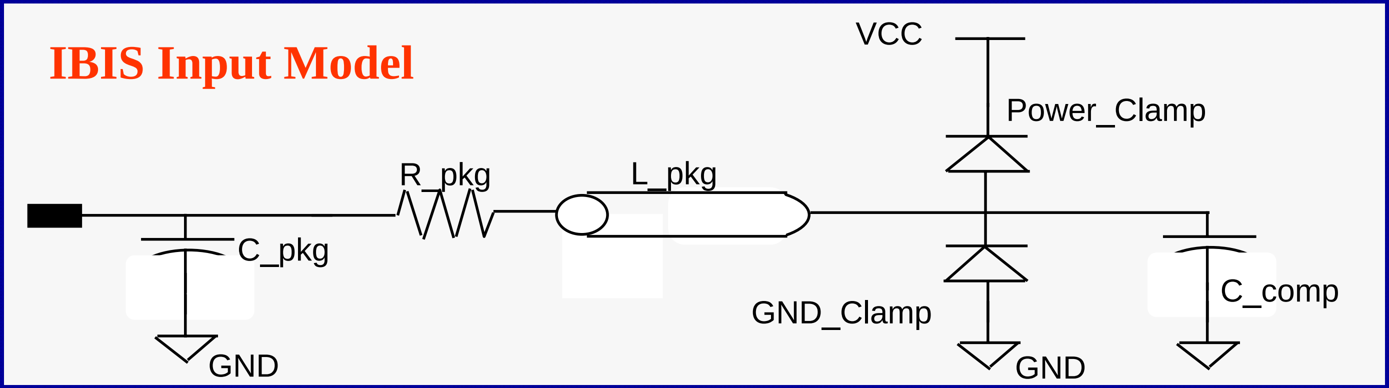
Timing and Power Models

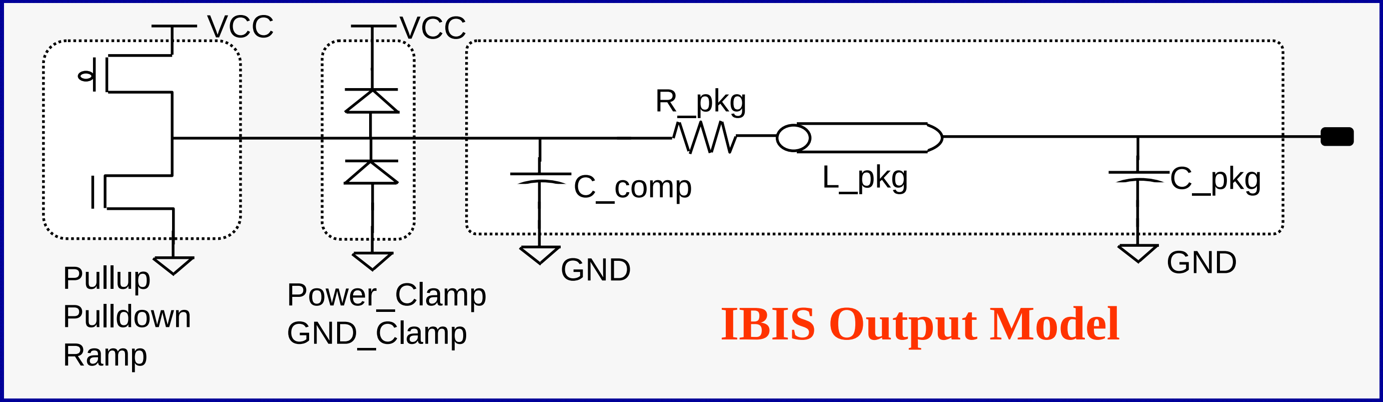
CharFlo-Cell!™

- Intrinsic delay and output transition time
- Effective input pin capacitance
- Minimum pulse widths
- Setup, hold, recovery and removal time
- Dynamic, leakage (static) and hidden power
- Constraint edge control
  - Independent setup and hold
  - Dependent setup and hold
- Constraint violation determination
  - Functional failure
  - Absolute, relative and user-defined delay or slew degradation
  - Output and internal node glitch checking

IBIS Models

I/O Buffer Information Specification





IBIS Models

Generated by CharFlo-Cell!^{TM}

```
[IBIS ver]        2.1
[File name]       bufx1.ibs
[Component]       buffer
[Package]
| variable     typ         min         max
R_pkg          2.00m       1.00m       4.00m
L_pkg          0.20nH      0.10nH      0.40nH
C_pkg          2.00pF      1.00pF      4.00pF
[Model]           driver
Model_type        Output
Polarity          Non-Inverting
C_comp         5.00pF      5.00pF      5.00pF
|[Temperature Range]  -40.00  100.00  0.000
[Voltage Range]      1.98V   2.00V   2.20V
[Pulldown]
| voltage      I(typ)      I(min)      I(max)
  -1.98       -62.97mA    -69.51mA    -64.64mA
      . . .
|[Pullup]
| voltage      I(typ)      I(min)     I(max)
-1.94          0.11mA     93.54uA     0.12mA
     . . .
[GND_clamp]
| voltage     I(typ)      I(min)      I(max)
-2.5000     -2.1200A    -2.1770A    -2.0890A
    . . .
```

```
[POWER_clamp]
| voltage    I(typ)      I(min)     I(max)
-2.5000   44.0300e-06 34.4500e-06 54.0100e-06
    . . .
[Ramp]
| variable    typ             min             max
dV/dt_r   14.75u/-14.54f 10.22u/-7.70f 15.79u/-13.42f
dV/dt_f   68.40m/0.17n   63.60m/0.22n  86.40m/0.17n
R_load = 0.50k
[Rising Waveform]
R_fixture = 0.50k
V_fixture = 0.000
| time      V(typ)      V(min)    V(max)
0.000S      0.16V       0.16V     0.18V
. . .
[Falling Waveform]
R_fixture = 0.50k
V_fixture = 1.98
| time      V(typ)      V(min)    V(max)
0.000S     -0.22V      -0.21V    -0.24V
. . .
```

Technology Leader in IP Characterization and IC/PCB Simulation

Legend
Design Technology

CCS and ECSM Models

CharFlo-Cell! supports

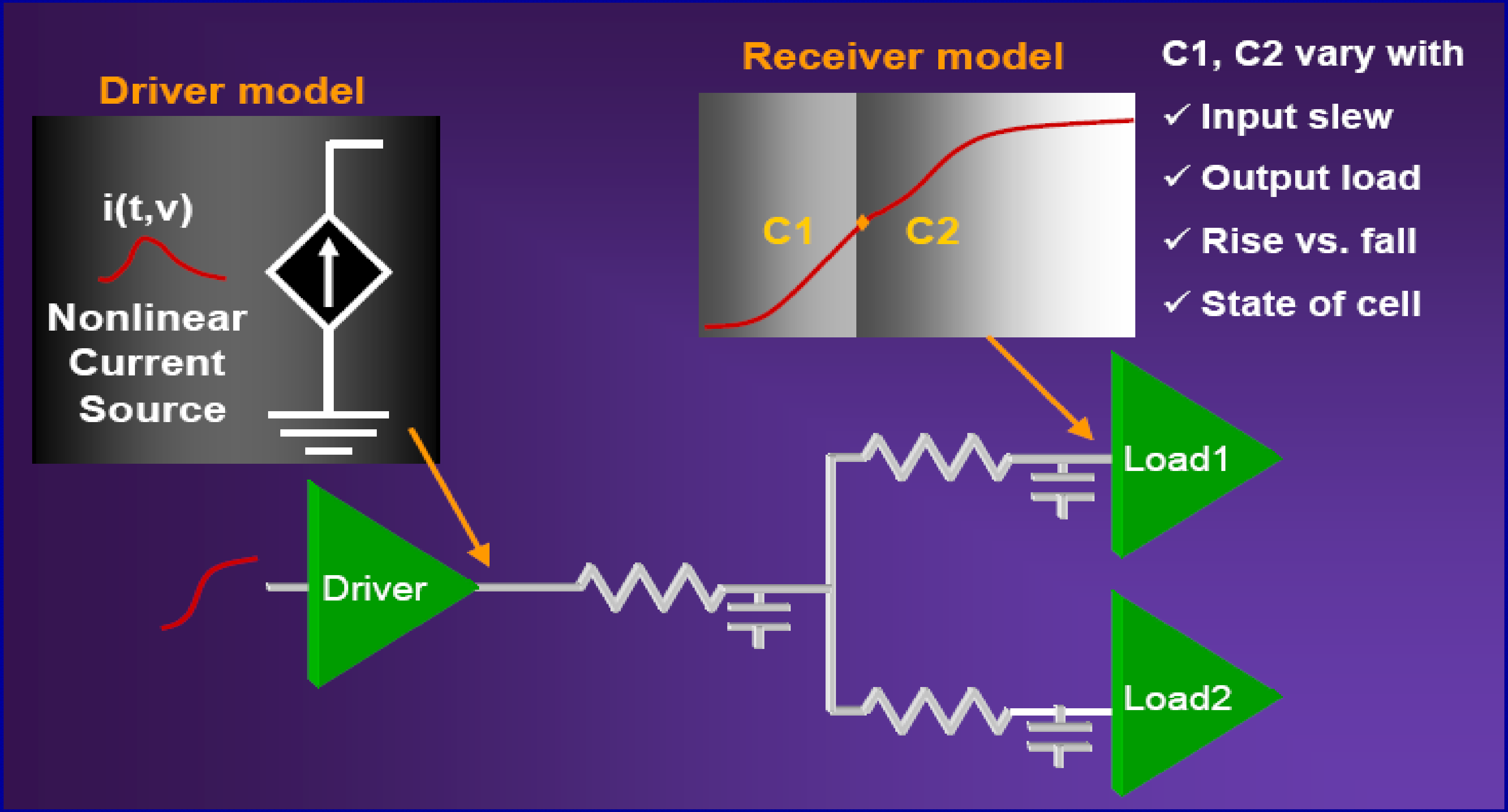
- CCS and ECSM current source timing model
  - Driver model

    Time-dependent voltage or current waveform for every combination of input slew rate and output loading
  - Receiver model

    Input pin capacitance for every combination of input slew rate and output loading
- CCS Power model
- CCS Noise model

CCS Timing Model

CharFlo-Cell!^{TM}

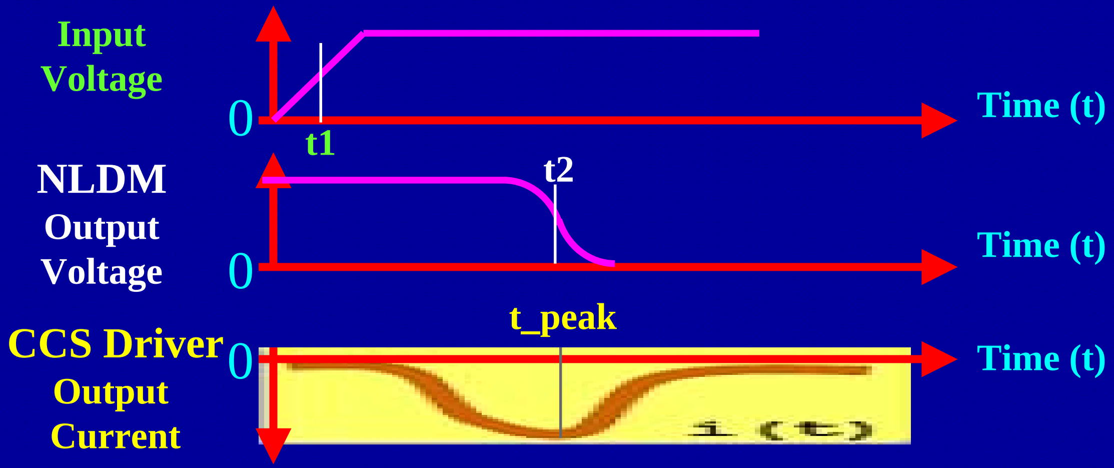


C1, C2 vary with

- ✓ Input slew
- ✓ Output load
- ✓ Rise vs. fall
- ✓ State of cell

CCS vs NLDM Delay

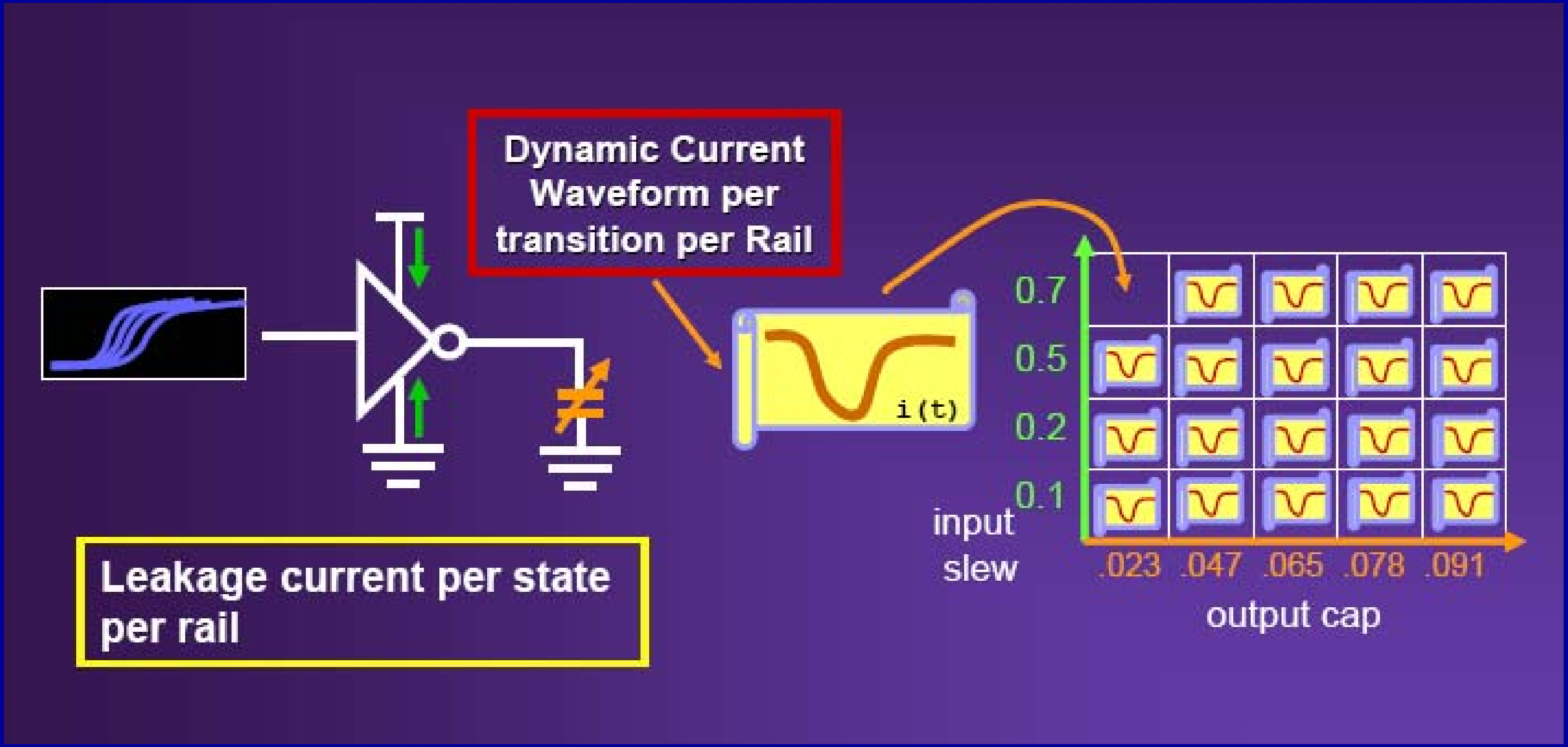
CCS vs NLDM Consistency Check



- NLDM_delay = t2 - t1
- CCS_delay from driver model = t_peak - t1
- CCS_delay and NLDM_delay could be well correlated with each other.

CCS Power Model

CharFlo-Cell!™


Dynamic Current Waveform per transition per Rail
i(t)
0.7
0.5
0.2
0.1
input slew
.023
.047
.065
.078
.091
output cap
Leakage current per state per rail

Dynamic CCS Power model can be characterized concurrently with CCS Timing model

CCS Noise Characterization

CharFlo-Cell!^{TM}

- CCS Noise is a structural boundary model
  - ccsn_first_stage* driven by input
  - ccsn_last_stage** driving output
- Each CCS Noise stage has 3 model components
  - DC current table
  - Dynamic behavior information
  - Parameters

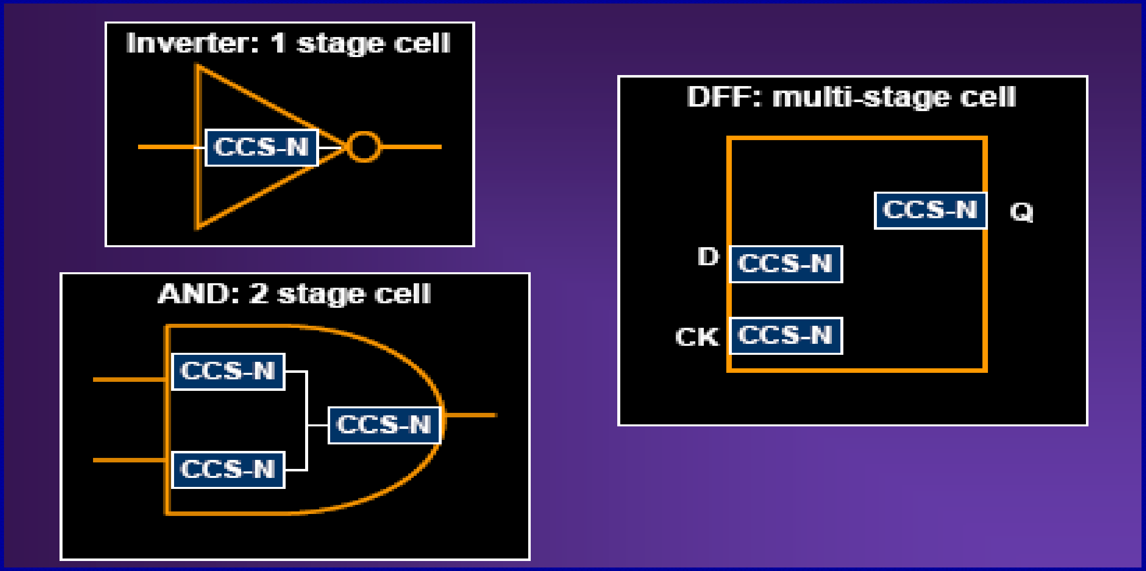
* First stage is the transistor Channel-Connected Block (CCB) partitioned for input pin.

** Last stage is the transistor Channel-Connected Block (CCB) partitioned for output pin.

Circuit Partition for Stages

CharFlo-Cell!^{TM}

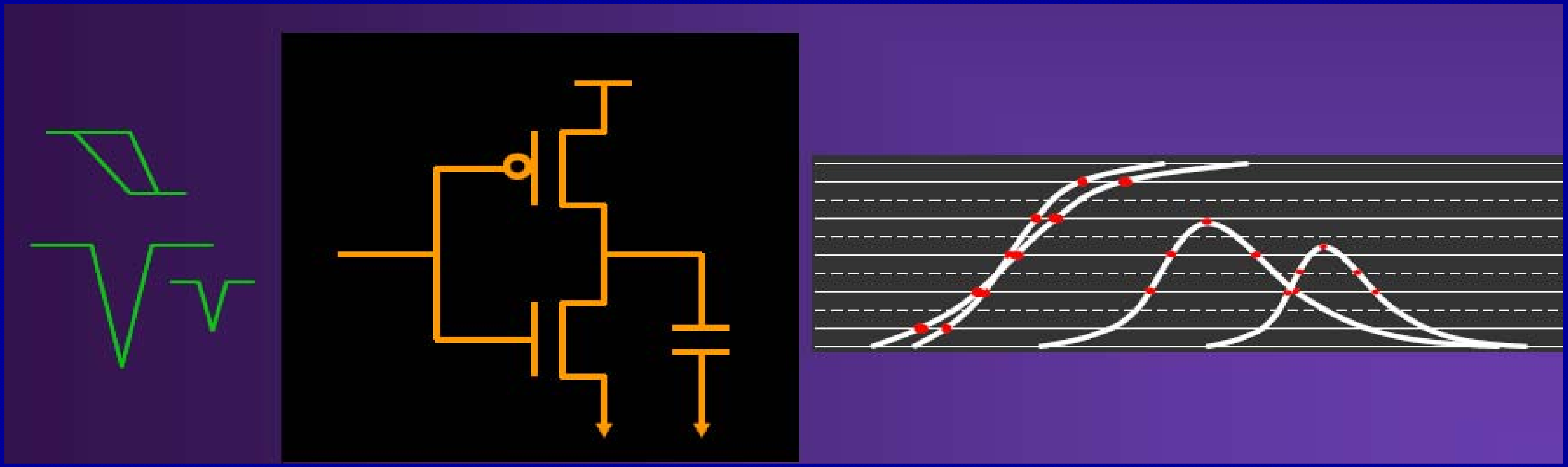
- Build in SpiceCut-Cell^{TM} to automatically partition each cell to channel-connected blocks (CCB) as the stages for all input pins and output pins



Dynamic Behavior

CCS Noise Stage Characterization

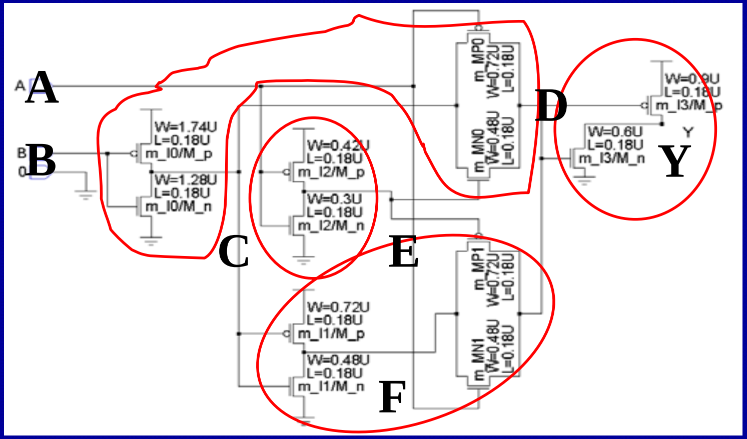
- Run a number of transient simulations on channel-connected block (CCB) created by SpiceCut-Cell
- ‘Ramps’ input for *output_voltage_rise/fall*
- ‘Glitches’ input for *propagated_noise_high/low*



Function Recognition

Directly from Cell Circuit Netlist

- Standard cells are normally by static designs. Their subcircuits and functions are quite straightforward.
- SpiceCut-Cell can partition/recognize those subcircuit patterns, and extract their corresponding functions.
- Example: Exclusive-OR (XOR) Cell



C = -B; F = -C = B; E = -A;

D = C * E + F * (-E)

= (-B) * (-A) + B * A

Y = (-A) * (-B) + A * B

Y = A ^ B

Function Verification

Compare Cell Netlist to .Function in .Lib

- From Spice circuit netlist, extract
  - Circuit functions and
  - All possible state patterns for each timing arc
- Based on .Function in .lib model, extract
  - All possible state patterns for each timing arc
- Validate the .Function in .lib model if both set of state patterns for each timing arc are equivalent.

New .Lib Model Creation
For New Cells without .Lib Models

- Minimal input specifications are required
  - Cell name, spice netlist and .Function to be in .lib
  - Latch() and FF() definitions with key pins
- Templates for .lib model are automatically generated
  - All possible timing arcs and their related_pin
  - Necessary conditions such as Timing_sense, When, and SDF_cond etc.
- Timing/power models are accurately characterized

Legend and Foundry

- Legend's tools have been adopted and silicon-proven by major foundries

* TSMC	* HHNEC
* UMC	* Jazz
* Dongbu	* Tower
* Vanguard	

- Direct access the updated SPICE models

* TSMC	* Chartered
* UMC	* SMIC
* IBM	* Tower
* Vanguard	* Jazz
* X-FAB	

Legend and Library Vendors

- Support memory IP re-characterization for

Artisan	Dolphin Technology
Virage	Faraday (UMC Alliance)
TSMC	VeriSilicon
Virtual-Silicon	Synopsys

- The memory instance models using Legend's tools have been silicon-proven by customers and major foundries.

Conclusion

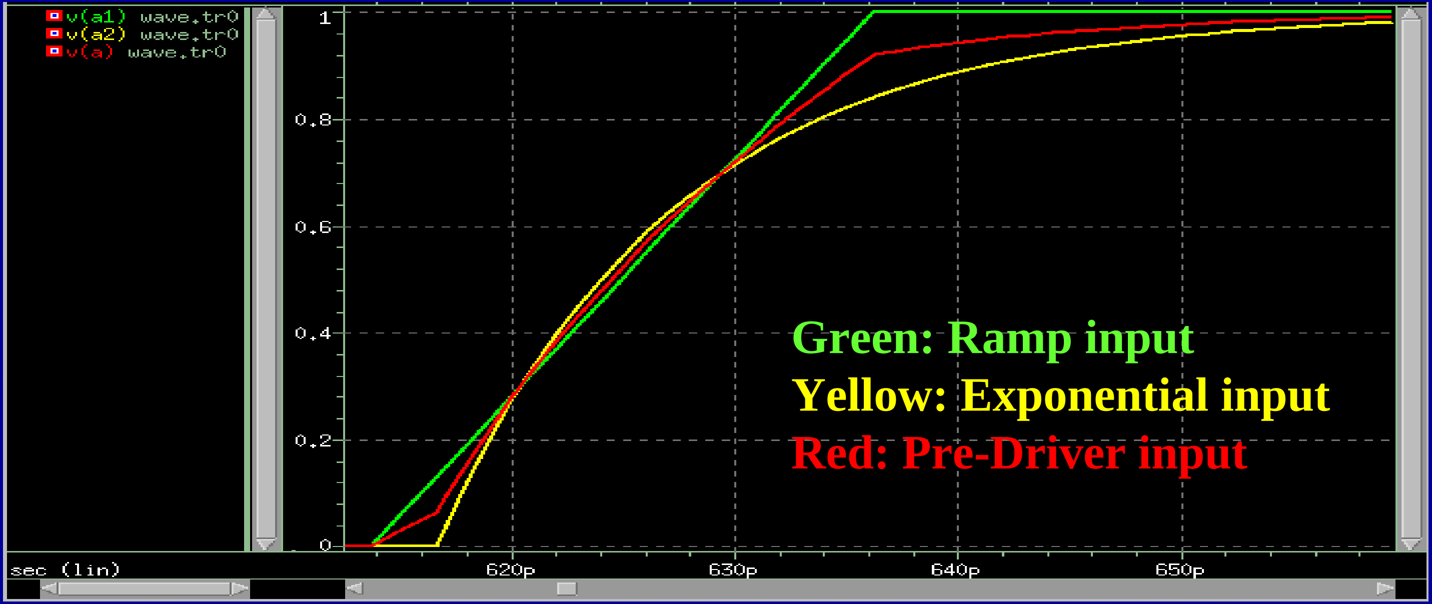
- CharFlo-Cell! is a next-generation cell/IO library characterization product, which is reliability and manufacturability aware
- Support CCS / ECSM models for nanometer designs
- Enable quick ‘time to market’
  - Fully automated and easy to set up
  - Short run time and excellent throughputs

Appendix

Pre-Driver Input Waveform

For 45nm Cell Characterization

- Pre-driver method is analogous to taking the output of a PWL source and passing it through a low-pass filter.
- Model Diagnoser supports both ramp and pre-driver input



Legend’s Patents

Cell/IO Library Characterization

- United States Patent 7231336

  "Glitch and metastability checks using signal characteristics“
- United States Patent 7131088

  "Reliability based characterization using bisection"
- United States Patent 7203918

  "Delay and signal integrity check and characterization"

Statistical Timing Model

Cell Library Characterization

- Systematic variations
  - Lithography could be the reason
  - Impact is uniform across a wide region on chip or wafer
  - Global parameters in statistical Spice models control the systematic variations
- Random variations
  - Gas doping could be the reason
  - Process variations apply to each MOSFET independently
  - MOSFET channel length (L) and threshold voltage (Vth) are the dominated parameter