The Industry-Leading Solution to Automate, Optimize, and Retarget Custom Circuit Design

Product Review
June 2010

Arsyn

- Analog Circuit Synthesis
- Circuit Optimization
- Circuit Re-Targeting
- Yield Improvement

Do Not Distribute
About Us

- Company Mission: To provide analog/RF design automation solutions which can
  - Reduce design cycle time 2X to 10X
  - Enable design innovation and first-pass success
- Two successful products
  - Arsyn - circuit synthesis an
  - Arana - behavioral modeling and design verification
- Products fully integrated with
  - Cadence (Connection); Mentor Graphics (Open Door); Synopsys (in-sync); Agilent ADS
- Privately funded and profitable since incorporation
Conventional Analog Design Process

- Knowledge and experience intensive
- Extensive user interaction
- Multiple silicon spins
- ad hoc design-Hard to reuse
- DFM not part of the design
What does Arsyn do?

- Critical design factors influence the performance of a circuit under certain environment are
  - Circuit topology/architecture (netlist)
  - Device performance (model)
  - Device parameters (w, l and other geometry)
  - Device parasitics and interconnect parasitics

- Arsyn takes above critical design factors as inputs and automatically find the best design values of such variables so that the circuit achieves performance expectation
Arsyn Overview

Key Benefits
- Reduce analog circuit design time
- Enable analog IP reuse
- Design for Manufacturability
- Design for Reliability

Key Features
- Any circuit topology and any process (CMOS, Bipolar, GaAs)
- Hierarchical synthesis
- Fast optimization engine
- Topology and sizing
- Parasitic-aware optimization
- Rapid yield optimization
Summary of Features I

◆ **Advanced Synthesis Flow**
  - Optimization-driven synthesis engine (multi-algorithms)
  - Multi-object optimization including circuit spec values and waveforms
  - Automatic constraint generation (10x speed-up in set up time), including device matching, OP Saturation, DFM metrics (max/min) and self-heating
  - Hierarchical optimization for large analog circuits as PLL/ADC etc
  - GUI-input and script-driven automation
  - Circuit Topology as Optimization Variable
  - Parasitic-aware synthesis from schematic down to post-layout circuit netlists

◆ **Parasitics Support for Silicon-Accurate Synthesis**
  - Device Parasitics + Interconnect Parasitics Update during Synthesis

◆ **Seamless CDS Integration – Automated Setup Procedure in Cadence**
  - ADE Testbench Manager
  - Goal Manager from ADE
  - Synthesis Parameter Selector from Schematic Editor
  - Backannotator to Schematic Editor
  - Callback device parasitic support

◆ **Open AMS Simulation Architecture**
  - Multi-simulator Support : Spectre, HSPICE, Eldo etc.
  - Multi-mode simulation support: Matlab, behavior and circuit simulator cosim
  - Simulation Pre/Post-Scripting, Testbench Sequencing
Summary of Arsyn Features II

- **Combined Local and Global Optimization**
  - Local optimization for fine tuning and design centering
  - Global optimization for IP reuse and re-targeting

- **Run Data Processing in Initial/Post-Optimization**
  - Analysis Plot + Radar Chart* + History Display for Multi-Objective Design Boundary Exploration
  - HTML/XML design data booking
  - Behavioral model/IP generation

- **PVT Corner Characterization and Optimization**
  - Easy Setup on Process, voltage, temperature or any custom variables
  - Supports up to 4000 corners during optimization

- **Robustness Design Exploration**
  - Automated setup of DFM (yield, variability/customized) metrics and goals
  - Parametric Yield/Taguchi Quality Loss Factor (On-Target Design)/ Performance Variability/Customized DFM Metrics

- **Various Foundry PDK Support**
  - IBM/JAZZ/UMC/TSMC/SMIC foundry design kits

- **Integrated with Arana for circuit modeling & analysis**
  - A complete automated design loop for analog/RF/full custom circuits
Arsyn Product Design Flow (Nominal Design)

Process Data ➔ Specifications ➔ 1/N Candidates ➔ Design Characterization

Meet specs?

- Yes ➔ Golden Design ➔ Design Characterization
- NO ➔ Design Optimization ➔ Knowledge Base ➔ Meet specs?
  - Yes ➔ Design Report
  - NO ➔ Design Analysis ➔ Layout & Extraction ➔ Meet specs?
    - Yes ➔ Golden Design ➔ Design Characterization
    - NO ➔ Design Optimization ➔ Knowledge Base

Arsyn Product Design Flow (Nominal Design)
## cktOPAMP Datasheet

<table>
<thead>
<tr>
<th>Testbench</th>
<th>Measurement Name</th>
<th>Measurement</th>
<th>Characterization</th>
<th>Synthesis</th>
<th>LPV</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC_xf_noise_27C</td>
<td>Avol_db</td>
<td>DC Gain</td>
<td>40.6/50 min</td>
<td>49 (21%)</td>
<td>39.7 (-2%)</td>
</tr>
<tr>
<td></td>
<td>GBP</td>
<td>Gain bandwidth product</td>
<td>320M/250M min</td>
<td>375M (17%)</td>
<td>289M (-9.6%)</td>
</tr>
<tr>
<td></td>
<td>Phase_margin</td>
<td>Phase margin</td>
<td>86/(65,95)</td>
<td>83 (-3%)</td>
<td>78.9 (-8.4%)</td>
</tr>
<tr>
<td></td>
<td>UGB</td>
<td>Unity Gain Bandwidth</td>
<td>286M/250 min</td>
<td>358M (25%)</td>
<td>285M (-11.3%)</td>
</tr>
<tr>
<td></td>
<td>CMRR</td>
<td>Common mode rejection ratio</td>
<td>319/200 min</td>
<td>451 (41%)</td>
<td>88.45 (-72.7%)</td>
</tr>
<tr>
<td></td>
<td>PSRR_VDDA_db</td>
<td>Power Supply Rejection Ratio</td>
<td>311/200 min</td>
<td>310 (0%)</td>
<td>74.63 (-76%)</td>
</tr>
<tr>
<td></td>
<td>PSRR_VSSA_db</td>
<td>Power Supply Rejection Ratio</td>
<td>316/200 min</td>
<td>299 (-5%)</td>
<td>61.25 (-81%)</td>
</tr>
<tr>
<td>TRAN_27C</td>
<td>Slewrate</td>
<td>Slew Rate</td>
<td>294M/200M min</td>
<td>278M (-5%)</td>
<td>272M (-7.3%)</td>
</tr>
<tr>
<td></td>
<td>Pos_Overshoot</td>
<td>Positive overshoot</td>
<td>60%/10% max</td>
<td>9.8% (-98%)</td>
<td>56% (-4.9%)</td>
</tr>
<tr>
<td></td>
<td>Neg_Overshoot</td>
<td>Negative overshoot</td>
<td>60%/10% max</td>
<td>9.8% (-84%)</td>
<td>54% (-8.2%)</td>
</tr>
<tr>
<td></td>
<td>Full_power_BW</td>
<td>f&lt;sub&gt;max&lt;/sub&gt;(SR)</td>
<td>54M /25M min</td>
<td>50.2M (-7%)</td>
<td>50M (-7.5%)</td>
</tr>
<tr>
<td></td>
<td>Pos_Sett_time_1per</td>
<td>Positive settling time@1%</td>
<td>6.7ns/7ns max</td>
<td>7.5ns (12%)</td>
<td>7.4ns (8.4%)</td>
</tr>
<tr>
<td></td>
<td>Neg_Sett_time_1per</td>
<td>Negative settling time@1%</td>
<td>6.8ns/7ns max</td>
<td>7.5ns (12%)</td>
<td>7.4ns (8.4%)</td>
</tr>
<tr>
<td>DC_CMR</td>
<td>IDDQ</td>
<td>IDD power current</td>
<td>1.84mA/20mA max</td>
<td>18.8mA (2%)</td>
<td>1.78mA (-3.0%)</td>
</tr>
<tr>
<td></td>
<td>CMR</td>
<td>Common-mode voltage range</td>
<td>374mV/300mV max</td>
<td>406mV (9%)</td>
<td>377mV (0.76%)</td>
</tr>
<tr>
<td></td>
<td>Cm_min</td>
<td>Common-mode voltage min</td>
<td>-87mV/-200mV min</td>
<td>-200mV (130%)</td>
<td>-92mV(12%)</td>
</tr>
<tr>
<td></td>
<td>Cm_max</td>
<td>Common-mode voltage max</td>
<td>287mV/200mV max</td>
<td>205mV (-29%)</td>
<td>279mV(-2.7%)</td>
</tr>
<tr>
<td>CMFB_27C</td>
<td>phMarginPcmdfbcl</td>
<td>CMFB PM (pos)</td>
<td>13/30 max</td>
<td>9 (-31%)</td>
<td>13.3(1.7%)</td>
</tr>
<tr>
<td></td>
<td>phMarginNcmdfbcl</td>
<td>CMFB PM (neg)</td>
<td>13/30 max</td>
<td>9 (-31%)</td>
<td>13(1.26%)</td>
</tr>
<tr>
<td></td>
<td>BWcmdfbP</td>
<td>CMFB BW (pos)</td>
<td>43M/50M max</td>
<td>50M (16%)</td>
<td>32M (-25%)</td>
</tr>
<tr>
<td></td>
<td>BWcmdfbN</td>
<td>CMFB BW (neg)</td>
<td>43M/50M max</td>
<td>50M (16%)</td>
<td>50.1M (18%)</td>
</tr>
<tr>
<td>Zout_27C</td>
<td>Zoutp_800M</td>
<td>Output impedance P</td>
<td>2630Ω/300Ω max</td>
<td>237Ω (-10%)</td>
<td>189 Ω (-28%)</td>
</tr>
<tr>
<td></td>
<td>Zoutm_800M</td>
<td>Output impedance M</td>
<td>2630Ω/300Ω max</td>
<td>237Ω (-10%)</td>
<td>188 Ω (-28.2%)</td>
</tr>
<tr>
<td>HD_27C</td>
<td>THD</td>
<td>Total Harmonic Distortion</td>
<td>7% /10% max</td>
<td>1.3% (-81%)</td>
<td>6.4 %</td>
</tr>
</tbody>
</table>
Visualization Analysis On One Example

- TdnDelay is a goal lagging behind the performance target
- The visualization on cost vs TdnDelay indicates 2.0-3.0 nS is the low cost region for TdnDelay. Current 2.0 ns threshold seems to be too stringent for the optimization
Arsyn-RPD Robust Product Design Flow

Statistical Process Data → RPD Spec → 1/n candidate → Design Characterization

If the best one meets RPD Spec?

Best Design

Yes → Layout & Extraction → Post-Layout Netlist → RPD Design Verification

Meet RPD Spec?

Yes → RPD Design Optimization

NO → DOE Design Analysis

NO → Data Book Generation

Knowledge Base
Performance Benchmarking from Customers

- Better solution quality
  - found out designs that meet the specs while competing tools fail)

- Less simulation runs
  - Use typically 10x less simulation runs

- Better design flow integration

- Is not a point tool but a complete automation solution for IP reuse, analog migration and analog design productivity improvements
Example: Opt Design Point ≠ Good Yield

- The optimized design point from other tool has every output hit the specs.
- The Monte Carlo simulation over with process variation and mismatch analysis indicates a poor yield by this design point (<60%) for some specs.
Arsyn Yield Enhancement

Arsyn gives out a high-quality design point which can not only meet the specs but also achieve high yield in this yield optimization process.

Current = 200uA
Parallelism in Arsyn

- Arsyn used multithreading technology to explore parallelism to speed up its optimization.
- Our experiment shows that the simulation speed per candidate is linearly proportional to user-defined parallel number.
- Result of simulation speed for 150 candidates (9 run/per candidate * 150 candidates = 1350 run in total)
  - Shows the speed linearity with parallel factor from 1 to 6
Design Optimization on IBM 90nm Custom Digital

- The design is IBM 90nm custom digital circuit and simulated with NanoSim to reduce the simulation time.
- This application uses model selection (lvt fet/hvt fet) to do power vs timing trade-off.
- Obtained 26% power reduction with minor timing sacrifice.

<table>
<thead>
<tr>
<th></th>
<th>After 1st GA+LMS</th>
<th>Final stop point</th>
</tr>
</thead>
<tbody>
<tr>
<td>time</td>
<td>~4 hours</td>
<td>~15 hours</td>
</tr>
<tr>
<td>Power*</td>
<td>20%</td>
<td>26%</td>
</tr>
<tr>
<td>timing</td>
<td>Worst -0.34ns</td>
<td>Worst -0.3ns relax</td>
</tr>
</tbody>
</table>
4GHz ADC Design

- Five time reduction in design time (reusable)
- Over 15% improvement in speed, power, SNR
- Cleaner eye diagrams

6x6 mm
> 6000 HBT Transistors
6 b @ 2.4 GSPS

 Arsyn automatically searches the design space that is otherwise not possible by designers.

-- Dr. M-J Choe
Mixed-Signal Group Manager

Chip Measurement:
performance yield improved to 77% from 36%

Designer optimized
Arsyn optimized
Arsyn Demo Outline

- **MDAC in 90nm pipelined ADC**
  - Arana Cadence interface, model generation and validation flow
  - Key features:
    - multiple testbench support and sequencing
    - PVT corners and DFM
    - CPS
    - PDK callback support
    - Synthesis result visualization
    - Candidate backannotation

- **90nm PLL**
  - Hierarchical optimization
  - Optimize the transistor-level PLL design in 3 days on a single machine
Arsyn Demo
Comparison with Other Tools

◆ Simulation-based tools

◆ Equation-based tools
  - Faster turn-around
  - Long preparation time/learning curve
  - Not able to optimize large system

◆ Arsyn architecture combines
  - Simulation based: Any simulator
  - Equation based: Automated equation generation
  - Knowledge based.
## Feature Comparison with Other Tools

<table>
<thead>
<tr>
<th>Feature</th>
<th>Competitor</th>
<th>Arsyn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cadence Interface</td>
<td>Not able to set two blocks</td>
<td>OK</td>
</tr>
<tr>
<td>Support CDS CB</td>
<td>OK</td>
<td>OK</td>
</tr>
<tr>
<td>BA to CDS</td>
<td>OK</td>
<td>OK</td>
</tr>
<tr>
<td>Support Simulators</td>
<td>Spectre</td>
<td>HSPICE/Spectre/others</td>
</tr>
<tr>
<td>Support CPS</td>
<td>-</td>
<td>OK</td>
</tr>
<tr>
<td>Visualization</td>
<td>-</td>
<td>OK</td>
</tr>
<tr>
<td>Characterization</td>
<td>-</td>
<td>OK</td>
</tr>
<tr>
<td>Sequencing</td>
<td>-</td>
<td>OK</td>
</tr>
<tr>
<td>Hierarchical Opt</td>
<td>-</td>
<td>OK</td>
</tr>
<tr>
<td>Sensitivity Analysis</td>
<td>-</td>
<td>OK</td>
</tr>
<tr>
<td>LPV</td>
<td>OK</td>
<td>OK</td>
</tr>
<tr>
<td>Scripting</td>
<td>-</td>
<td>OK</td>
</tr>
<tr>
<td>Parallelism/Dist Comp</td>
<td>OK</td>
<td>OK</td>
</tr>
</tbody>
</table>
**Design Candidate Search Capability**

**Arsyn:** constantly 10x less iterations than our competitors’ in multiple customer design evaluations

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC1.L</td>
<td>8.0E-8</td>
<td>2.0E-8</td>
</tr>
<tr>
<td>NC1.R</td>
<td>1.0E1</td>
<td>2.0E0</td>
</tr>
</tbody>
</table>

1421 iterations vs. 9963 iterations
Successful Test Cases

<table>
<thead>
<tr>
<th>Circuit Type</th>
<th>PDK</th>
<th>Process</th>
<th>Success</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain-boosted OPAMP</td>
<td>UMC</td>
<td>90nm</td>
<td>✓</td>
</tr>
<tr>
<td>LVDS – Transmitter</td>
<td>IBM</td>
<td>90nm</td>
<td>✓</td>
</tr>
<tr>
<td>PLL</td>
<td>IBM</td>
<td>90nm</td>
<td>✓</td>
</tr>
<tr>
<td>10 bit ADC</td>
<td>TSMC</td>
<td>65nm</td>
<td>✓</td>
</tr>
<tr>
<td>SerDes-TX</td>
<td>IBM</td>
<td>90nm</td>
<td>✓</td>
</tr>
<tr>
<td>6 bit DAC</td>
<td>IBM</td>
<td>90nm</td>
<td>✓</td>
</tr>
<tr>
<td>FC-OPAMP</td>
<td>JAZZ</td>
<td>0.18um</td>
<td>✓</td>
</tr>
<tr>
<td>Switch Circuit</td>
<td>AMIS</td>
<td>0.35um</td>
<td>✓</td>
</tr>
<tr>
<td>ADC</td>
<td>MAXIM</td>
<td>0.35um</td>
<td>✓</td>
</tr>
</tbody>
</table>

- Arsyn has been successfully used in the design of various analog circuit types with different foundry PDKs.
- The practice constantly shows that Arsyn can improve the design quality by 10-20% over the designers while saving significant amount of circuit corner tuning time.
Summary

- **Arsyn is a useful tool to help circuit designers to**
  - Increase analog/RF designers and custom digital developers productivity
  - Facilitate process migration, circuit topology and testbench reuse
  - Ease design trade-off in complex scenarios
  - Improve yields for sub-90nm technology node and below

- **Compared with other tools, Arsyn has shown**
  - Constant performance advantage
  - Better cadence interface
  - More features to analyze and synthesize circuit
  - More flexible 3 party tool interface (HPSICE/MATLAB/MSIM/NanoSim/Eldo etc)