RORA Design Technologies
Leading Analog Design Automation ™

The Industry-Leading Solution to Automate, Optimize, and Retarget Custom Circuit Design

Product Review
June 2010

Arsyn

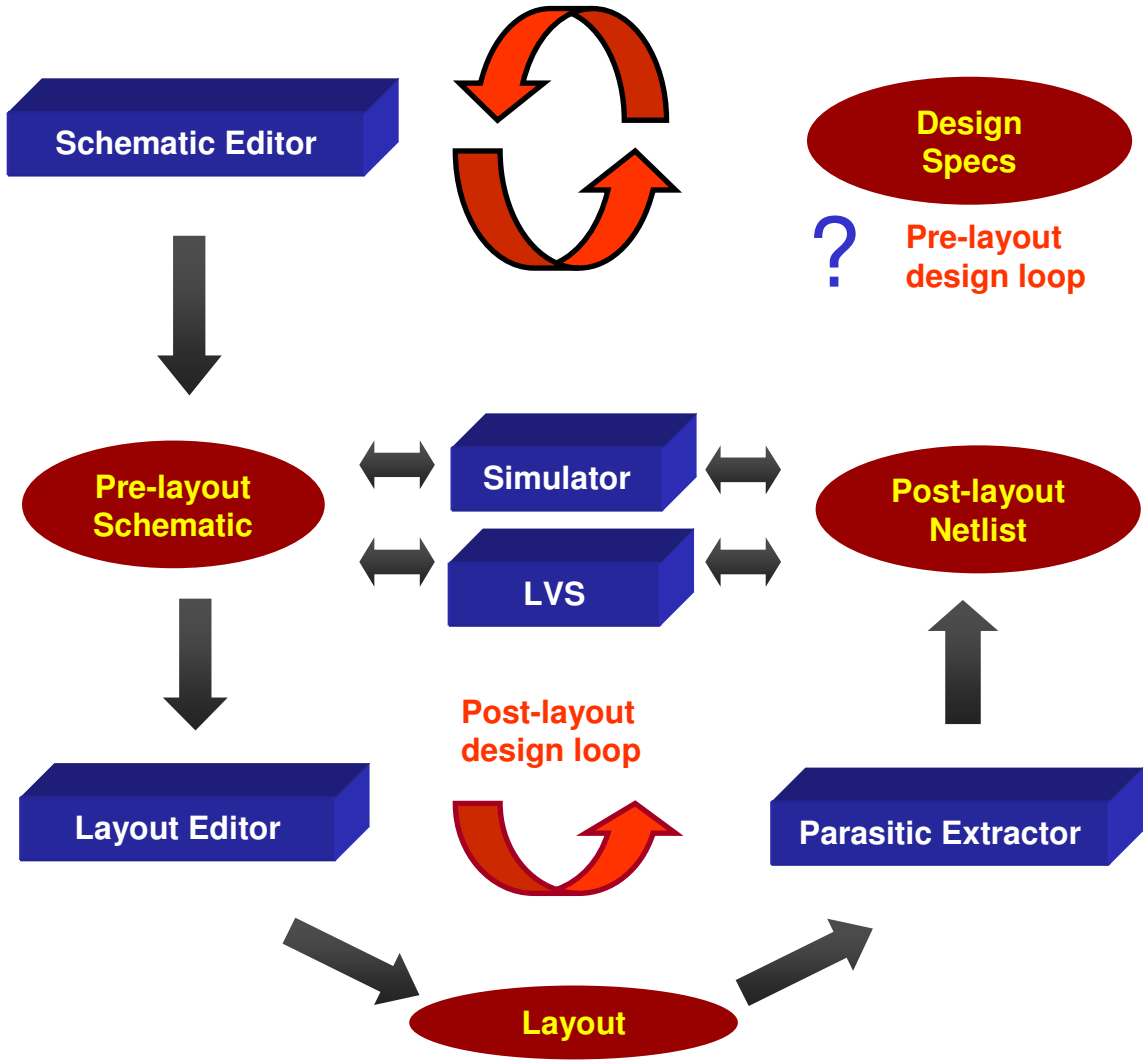
- → Analog Circuit Synthesis
- → Circuit Optimization
- → Circuit Re-Targeting
- → Yield Improvement

Do Not Distribute

About Us

- **Company Mission: To provide analog/RF design automation solutions which can**
  - **Reduce design cycle time 2X to10X**
  - **Enable design innovation and first-pass success**
- **Two successful products**
  - **Arsyn - circuit synthesis an**
  - **Arana - behavioral modeling and design verification**
- **Products fully integrated with**
  - Cadence (Connection); Mentor Graphics (Open Door) ; Synopsys (in-sync); Agilent ADS
- **Privately funded and profitable since incorproation**

Conventional Analog Design Process



- Knowledge and experience intensive
- Extensive user interaction
- Multiple silicon spins
- ad hoc design-Hard to reuse
- DFM not part of the design

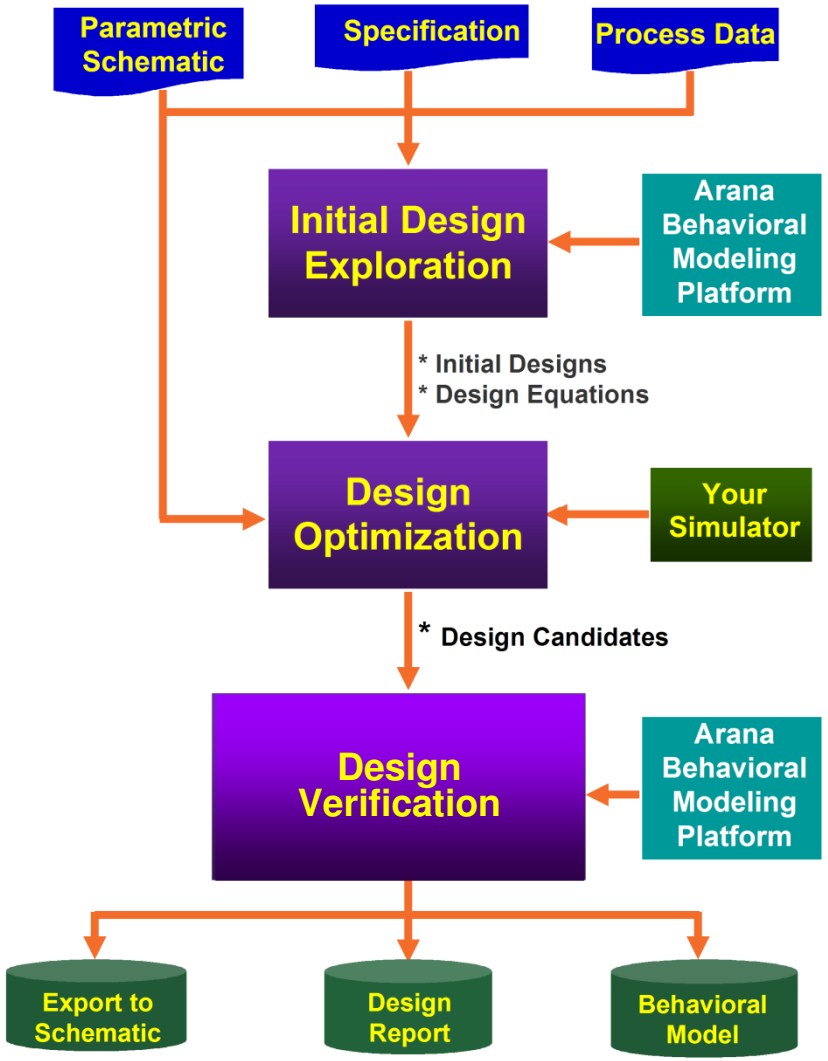
What does Arsyn do?

- **Critical design factors influence the performance of a circuit under certain environment are**
  - Circuit topology/architecture (netlist)
  - Device performance (model)
  - Device parameters (w, l and other geometry)
  - Device parasitics and interconnect parasitics
- **Arsyn takes above critical design factors as inputs and automatically find the best design values of such variables so that the circuit achieves performance expectation**

Arsyn Overview

- Key Benefits
  - Reduce analog circuit design time
  - Enable analog IP reuse
  - Design for Manufacturability
  - Design for Reliability

- Key Features
  - Any circuit topology and any process (CMOS, Bipolar, GaAs)
  - Hierarchical synthesis
  - Fast optimization engine
  - Topology and sizing
  - Parasitic-aware optimization
  - Rapid yield optimization



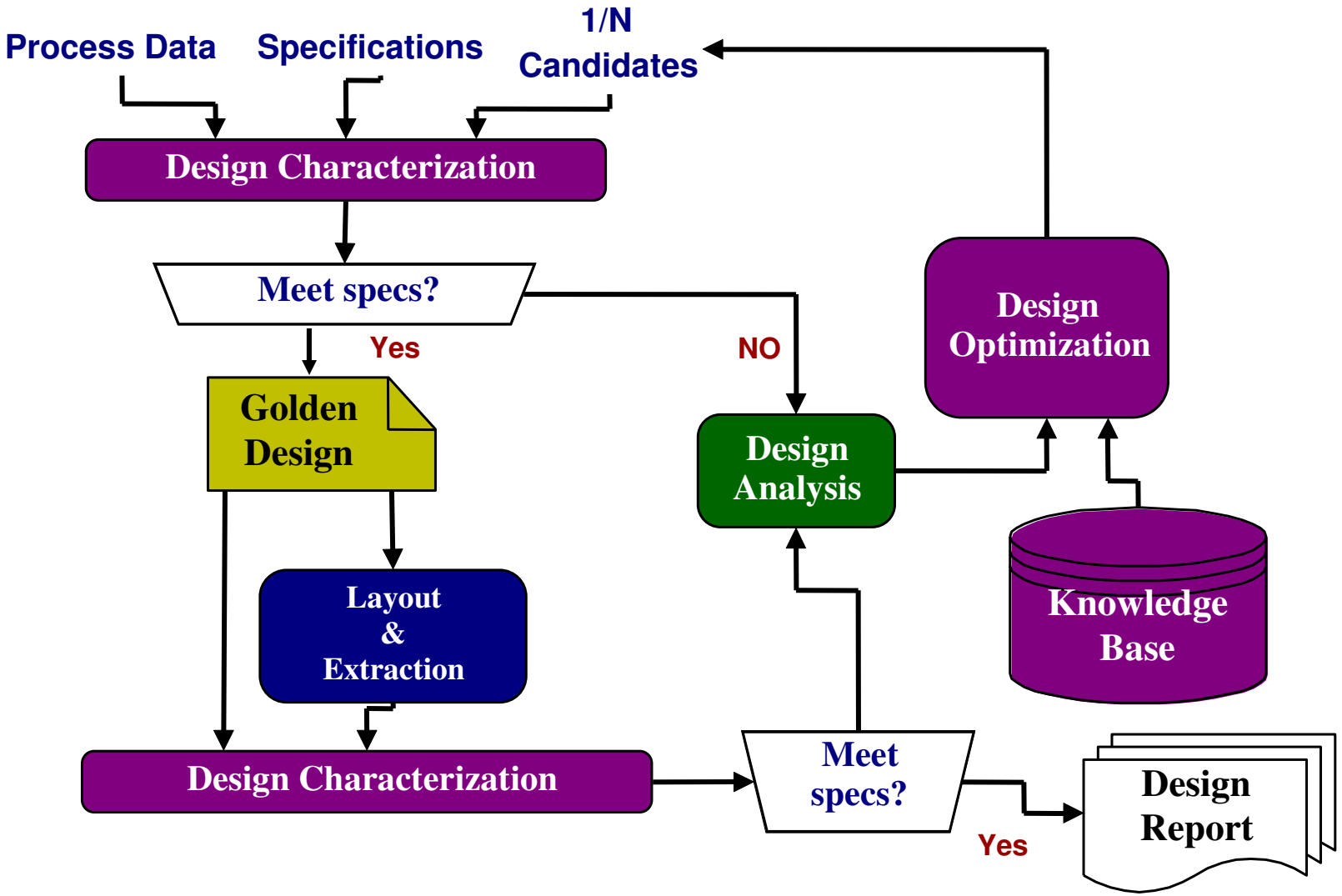
Summary of Features I

- **Advanced Synthesis Flow**
  - Optimization-driven synthesis engine (multi-algorithms)
  - Multi-object optimization including circuit spec values and waveforms
  - Automatic constraint generation (10x speed-up in set up time), including device matching, OP Saturation, DFM metrics (max/min) and self-heating
  - Hierarchical optimization for large analog circuits as PLL/ADC etc
  - GUI-input and script-driven automation
  - Circuit Topology as Optimization Variable
  - Parasitic-aware synthesis from schematic down to post-layout circuit netlists
- **Parasitics Support for Silicon-Accurate Synthesis**
  - Device Parasitics + Interconnect Parasitics Update during Synthesis
- **Seamless CDS Integration – Automated Setup Procedure in Cadence**
  - ADE Testbench Manager
  - Goal Manager from ADE
  - Synthesis Parameter Selector from Schematic Editor
  - Backannotator to Schematic Editor
  - Callback device parasitic support
- **Open AMS Simulation Architecture**
  - Multi-simulator Support : Spectre, HSPICE, Eldo etc.
  - Multi-mode simulation support: Matlab, behavior and circuit simulator cosim
  - Simulation Pre/Post-Scripting, Testbench Sequencing

Summary of Arsyn Features II

- **Combined Local and Global Optimization**
  - Local optimization for fine tuning and design centering
  - Global optimization for IP reuse and re-targeting
- **Run Data Processing in Initial/Post-Optimization**
  - Analysis Plot + Radar Chart* + History Display for Multi-Objective Design Boundary Exploration
  - HTML/XML design data booking
  - Behavioral model/IP generation
- **PVT Corner Characterization and Optimization**
  - Easy Setup on Process, voltage, temperature or any custom variables
  - Supports up to 4000 corners during optimization
- **Robustness Design Exploration**
  - Automated setup of DFM (yield, variability/customized) metrics and goals
  - Parametric Yield/Taguchi Quality Loss Factor (On-Target Design)/ Performance Variability/Customized DFM Metrics
- **Various Foundry PDK Support***
  - IBM/JAZZ/UMC/TSMC/SMIC foundry design kits
- **Integrated with Arana for circuit modeling & analysis**
  - A complete automated design loop for analog/RF/full custom circuits

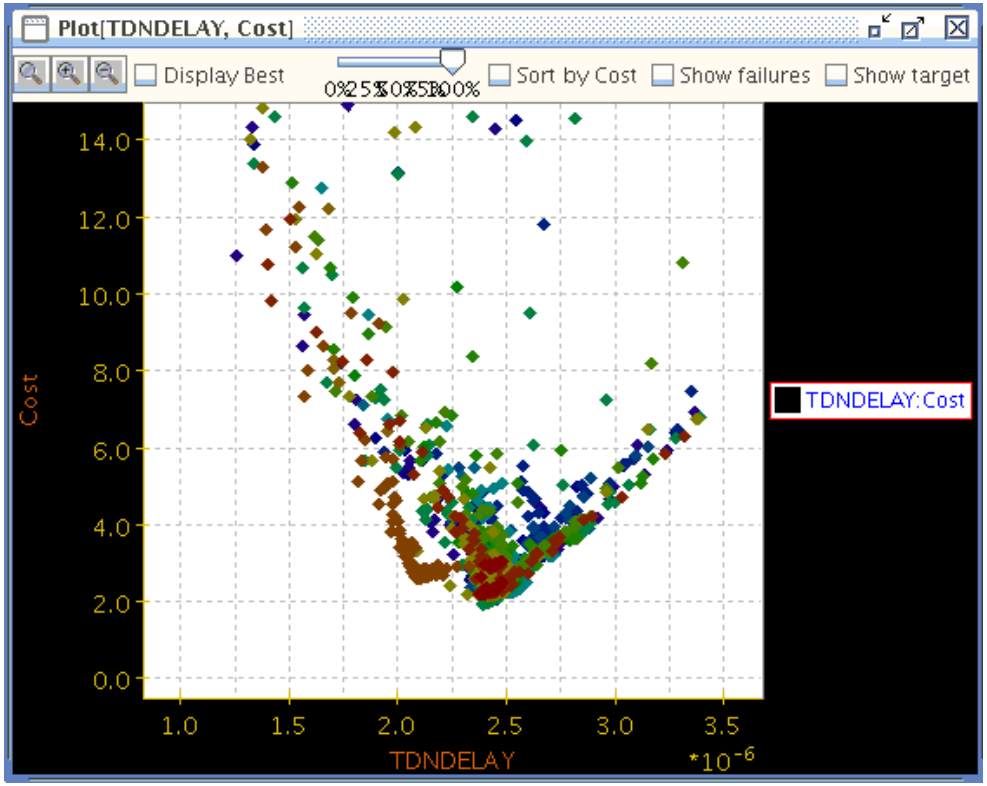
Arsyn Product Design Flow (Nominal Design)



cktOPAMP Datasheet

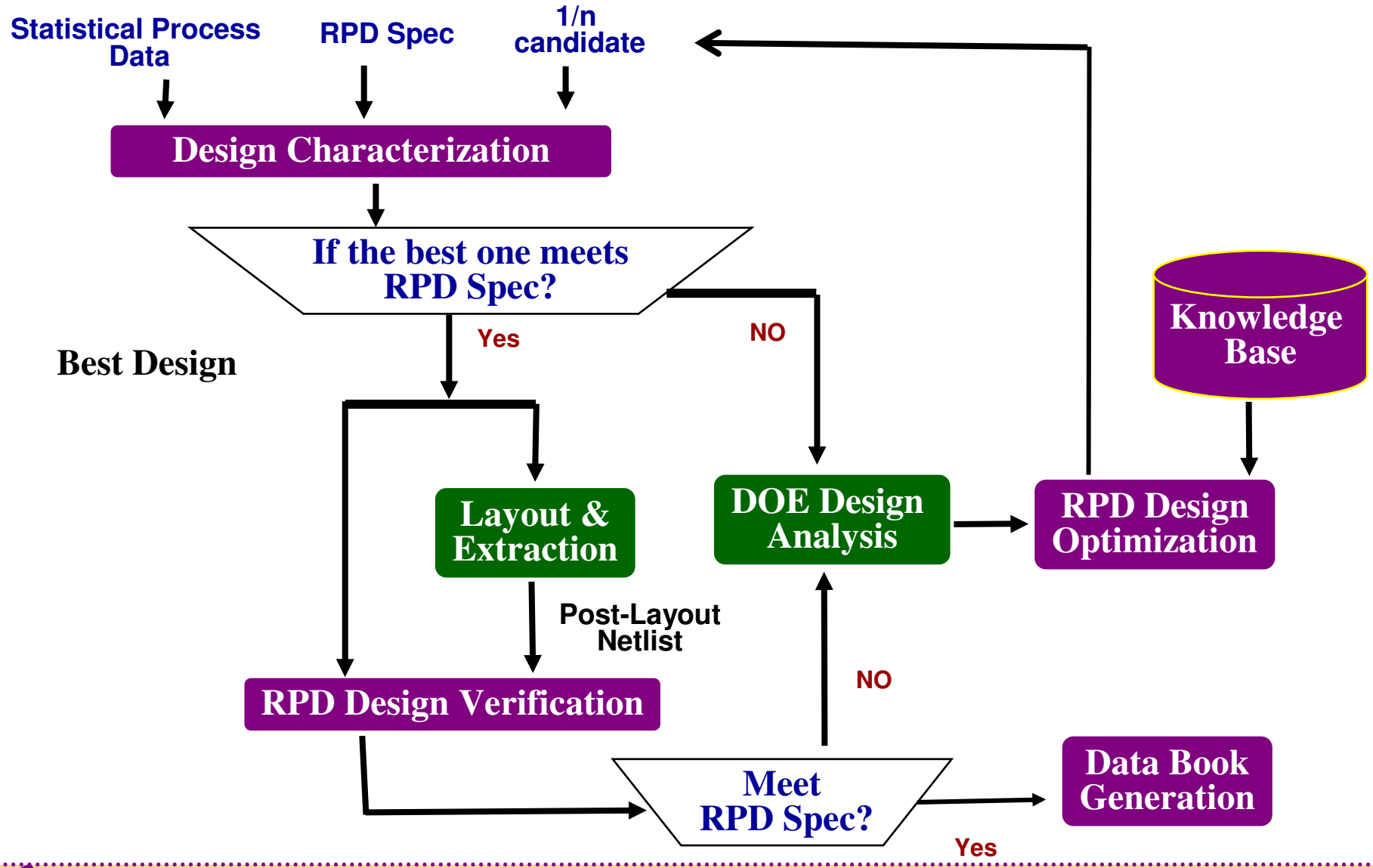
Testbench	Measurement Name	Measurement	Characterization	Synthesis	LPV
AC_xf_noise_27C	Avol_dB	DC Gain	40.6/50 min	49 (21%)	39.7 (-2%)
	GBP	Gain bandwidth product	320M/250M min	375M (17%)	289M (-9.6%)
	Phase_margin	Phase margin	86/(65,95)	83 (-3%)	78.9 (-8.4%)
	UGB	Unity Gain Bandwidth	286M/250 min	358M (25%)	285M (-11.3%)
	CMRR	Common mode rejection ratio	319/200 min	451 (41%)	88.45(-72.%)
	PSRR_VDDA_dB	Power Supply Rejection Ratio	311/200 min	310 (0%)	74.63(-76%)
	PSRR_VSSA_dB	Power Supply Rejection Ratio	316/200 min	299 (-5%)	61.25(-81%)
TRAN_27C	Slewrate	Slew Rate	294M/200M min	278M (-5%)	272M (-7.3%)
	Pos_Overshoot	Positive overshoot	60%/10% max	9.8% (-98%)	56%(-4.9%)
	Neg_Overshoot	Negative overshoot	60%/10% max	9.8% (-84%)	54%(-8.2%)
	Full_power_BW	f_{max}(SR)	54M /25M min	50.2M (-7%)	50M (-7.5%)
	Pos_Sett_time_1per	Positive settling time@1%	6.7ns/7ns max	7.5ns (12%)	7.4ns (8.4%)
	Neg_Sett_time_1per	Negative settling time@1%	6.8ns/7ns max	7.5ns (12%)	7.4ns (8.4%)
DC_CMR	IDDQ	IDD power current	1.84mA/20mA max	18.8mA (2%)	1.78mA (-3.0%)
	CMR	Common-mode voltage range	374mV/300mV max	406mV (9%)	377mV (0.76%)
	Cm_min	Common-mode voltage min	-87mV/-200mV min	-200mV (130%)	-92mV(12%)
	Cmin_max	Common-mode voltage max	287mV/200mV max	205mV (-29%)	279mV(-2.7%)
CMFB_27C	phMarginPcmdfbcl	CMFB PM (pos)	13/30 max	9 (-31%)	13.3(1.7%)
	phMarginNcmdfbcl	CMFB PM (neg)	13/30 max	9 (-31%)	13.1(0.26%)
	BWcmfbP	CMFB BW (pos)	43M/50M max	50M (16%)	32M (-25%)
	BWcmfbN	CMFB BW (neg)	43M/50M max	50M (16%)	50.1M (18%)
Zout_27C	Zoutp_800M	Output impedance P	263Ω/300Ω max	237Ω (-10%)	189 Ω (-28%)
	Zoutm_800M	Output impedance M	263Ω/300Ω max	237Ω (-10%)	188 Ω (-28.2%)
HD_27C	THD	Total Harmonic Distortion	7% /10% max	1.3% (-81%)	6.4 %

Visualization Analysis On One Example



- TdnDelay is a goal lagging behind the performance target
- The visualation on cost vs TdnDelay indicates 2.0-3.0 nS is the low cost region for TdnDelay. Current 2.0 ns threshold seems to be too stringent for the optimization

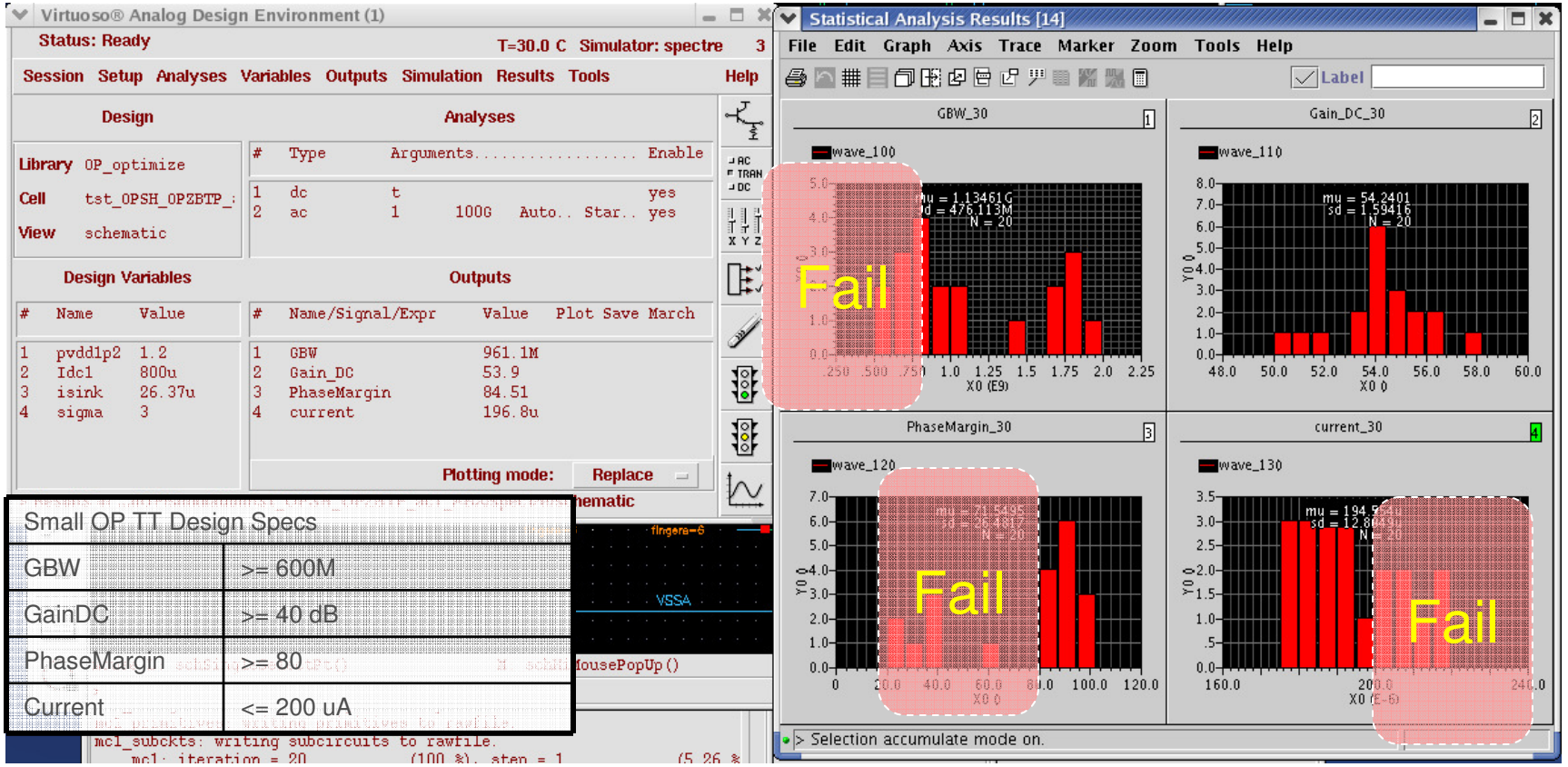
Arsyn-RPD Robust Product Design Flow



Performance Benchmarking from Customers

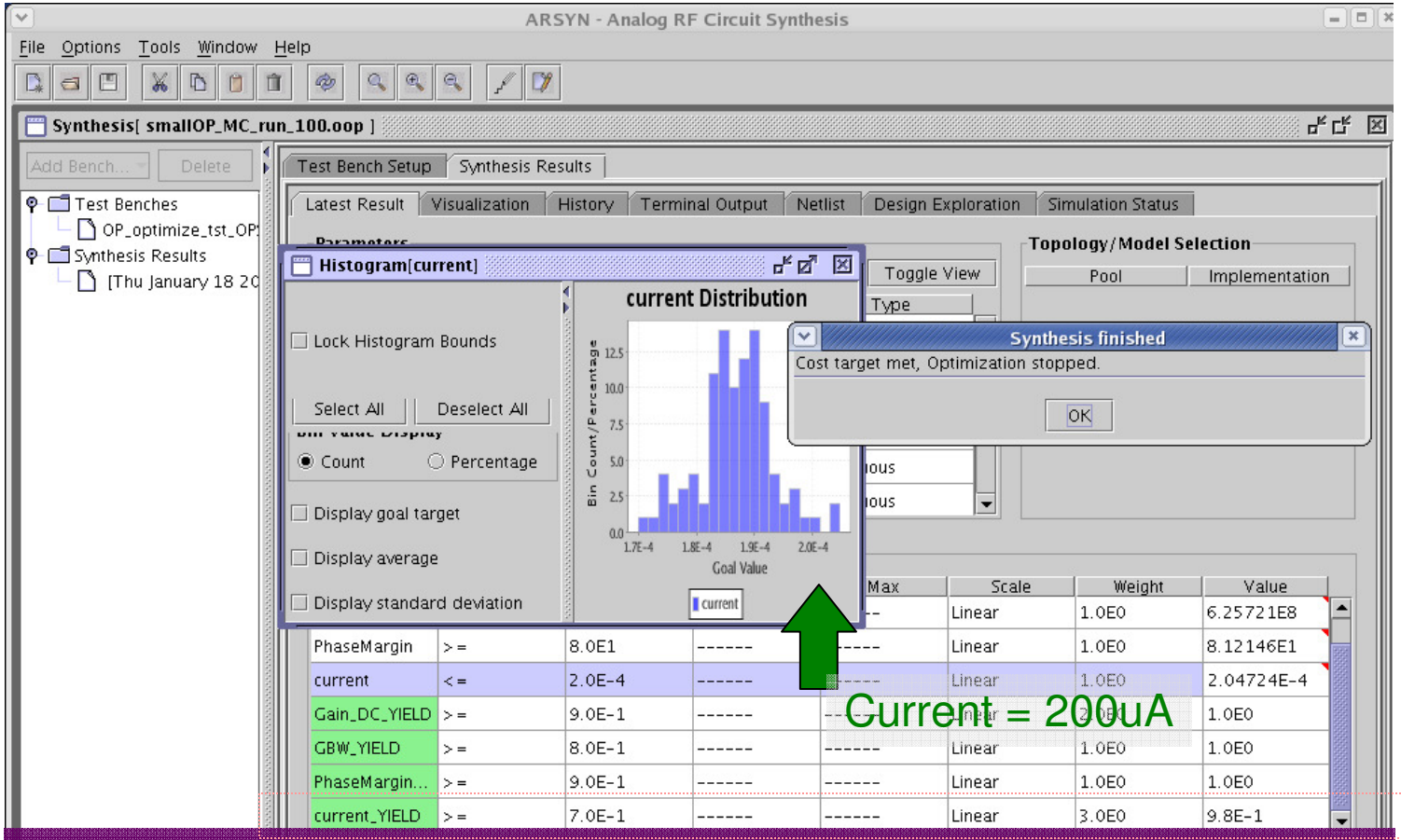
- **Better solution quality**
  - found out designs that meet the specs while competing tools fail)
- **Less simulation runs**
  - Use typically 10x less simulation runs
- **Better design flow integration**
- **Is not a point tool but a complete automation solution for IP reuse, analog migration and analog design productivity improvements**

Example: Opt Design Point ≠ Good Yield



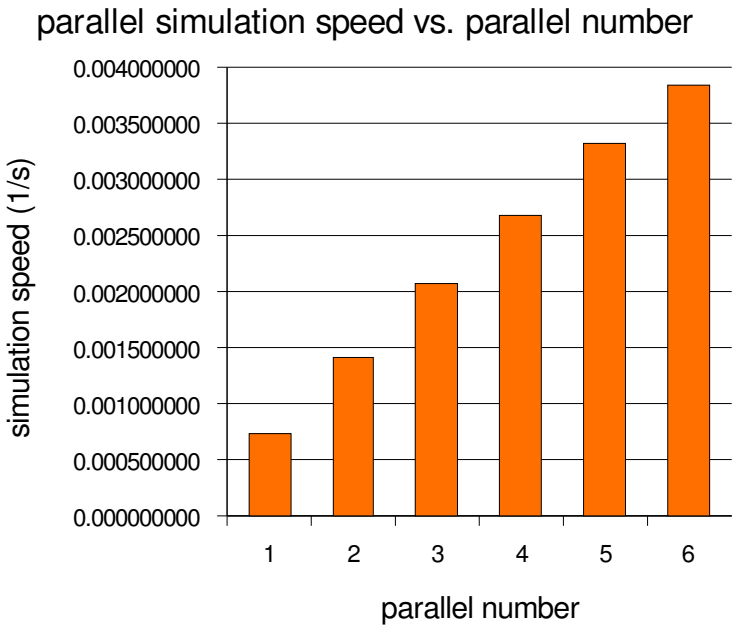
- The optimized design point from other tool has every output hit the specs.
- The Monte Carlo simulation over with process variation and mismatch analysis indicates a poor yield by this design point (<60%) for some specs

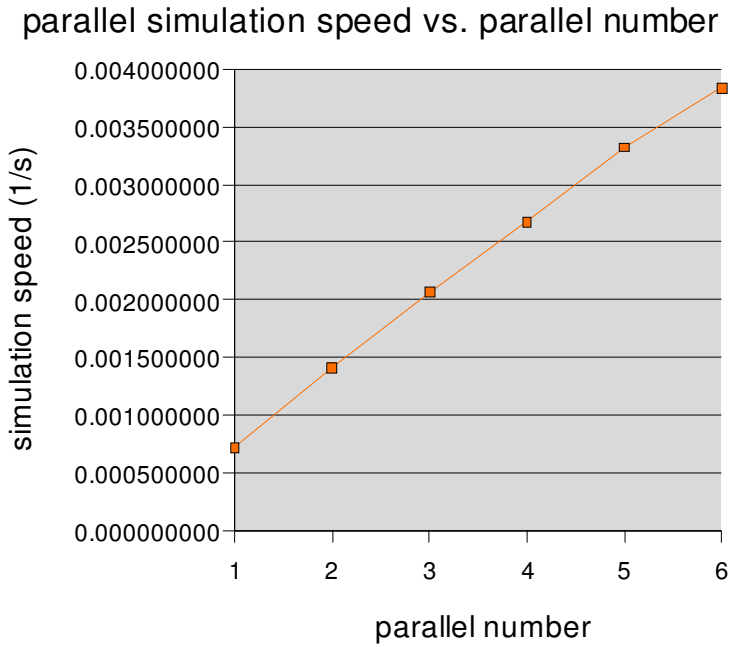
Arsyn Yield Enhancement



Arsyn gives out a high-quality design point
which can not only meet the specs but also achieve high yield
in this yield optimization process

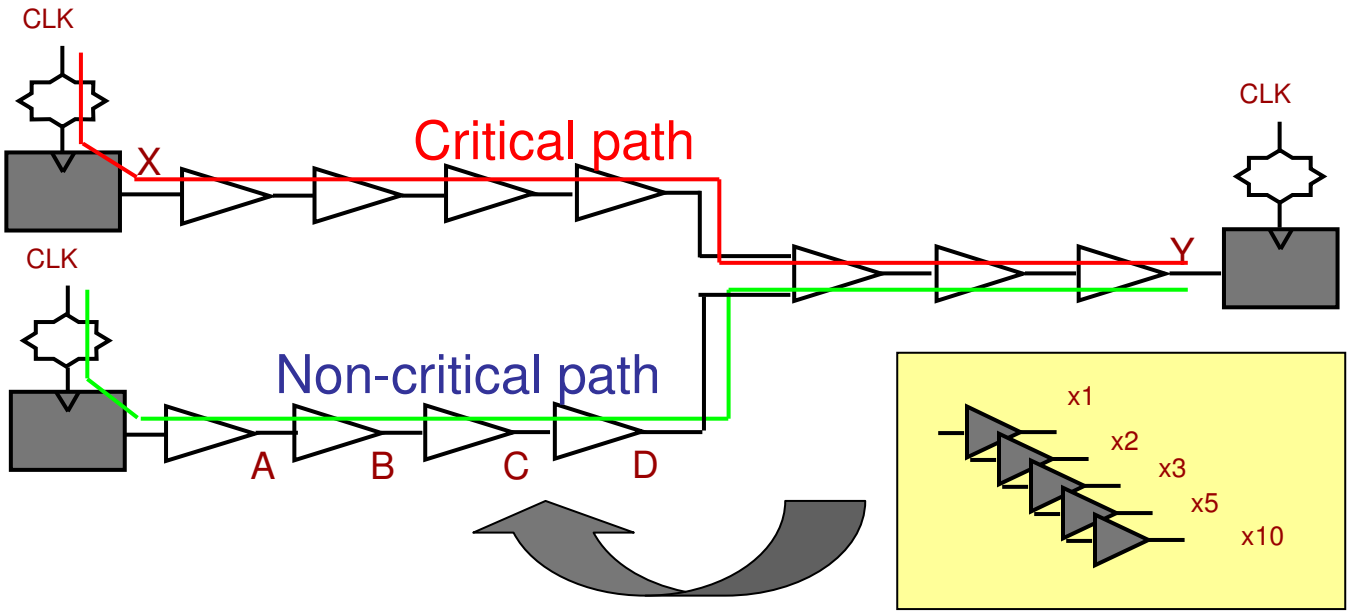
Parallelism in Arsyn





- **Arsyn used multithreading technology to explore parallelism to speed up its optimization.**
- **Our experiment shows that the simulation speed per candidate is linearly proportional to user-defined parallel number**
- **Result of simulation speed for 150 candidates (9 run/per candidate * 150 candidates = 1350 run in total)**
  - Shows the speed linearity with parallel factor from 1 to 6

Design Optimization on IBM 90nm Custom Digital

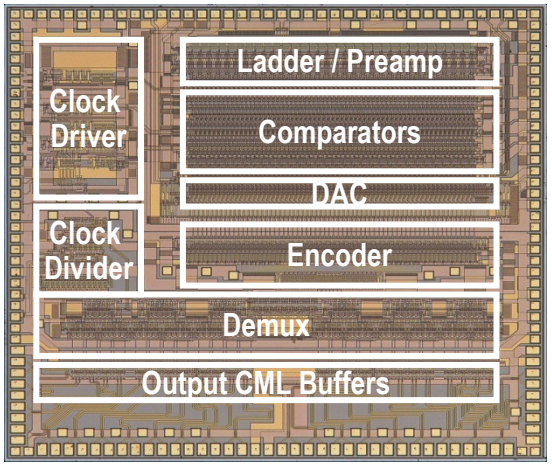


- The design is IBM 90nm custom digital circuit and simulated with NanoSim to reduce the simulation time
- This application uses model selection (lvt fet/hvt fet) to do power vs timing trade-off
- obtained 26% power reduction with minor timing sacrifice.

	After 1st GA+LMS	Final stop point
time	~4 hours	~15 hours
Power*	20%	26%
timing	Worst -0.34ns	Worst -0.3ns relax

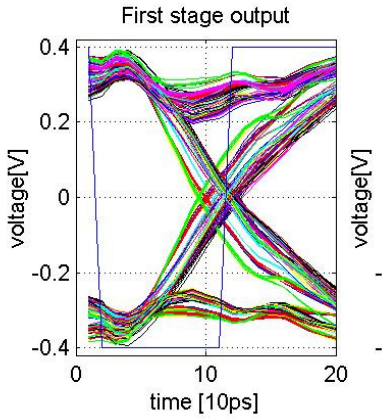
ROCKWELL SCIENTIFIC

4GHz ADC Design

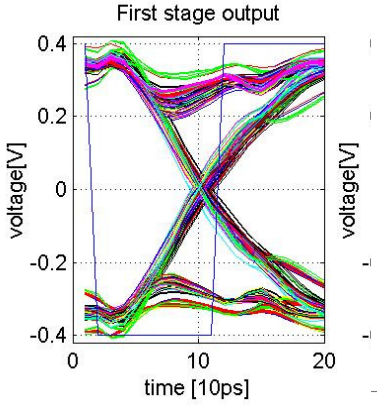


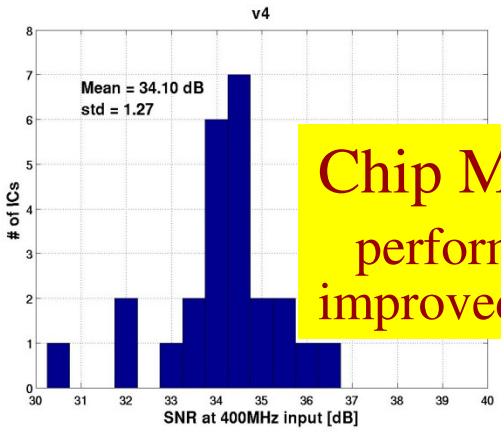
6x6 mm
> 6000 HBT Transistors
6 b @ 2.4 GSPS

- Five time reduction in design time (reusable)
- Over 15% improvement in speed, power, SNR
- Cleaner eye diagrams

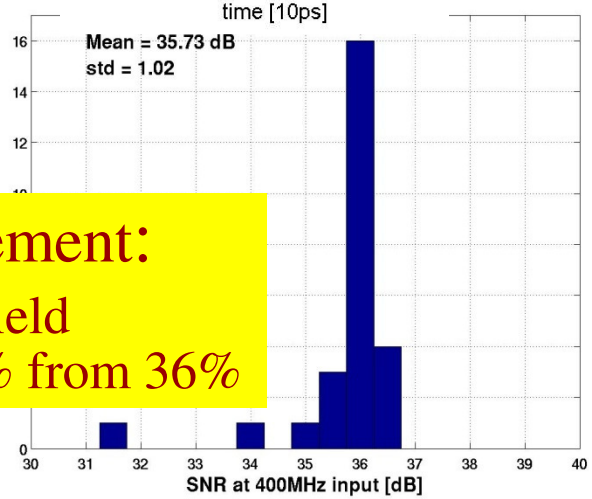


simulation





Designer optimized



Arsyn optimized

Chip Measurement:
performance yield
improved to 77% from 36%

Arsyn automatically searches the design space that is otherwise not possible by designers.
-- Dr. M-J Choe
Mixed-Signal
Group Manager

Arsyn Demo Outline

- **MDAC in 90nm pipelined ADC**
  - Arana Cadence interface, model generation and validation flow
  - Key features:
    - **multiple testbench support and sequencing**
    - **PVT corners and DFM**
    - **CPS**
    - **PDK callback support**
    - **Synthesis result visualization**
    - **Candidate backannotation**
- **90nm PLL**
  - Hierarchical optimization
  - Optimize the transistor-level PLL design in 3 days on a single machine

Arsyn Demo

Comparison with Other Tools

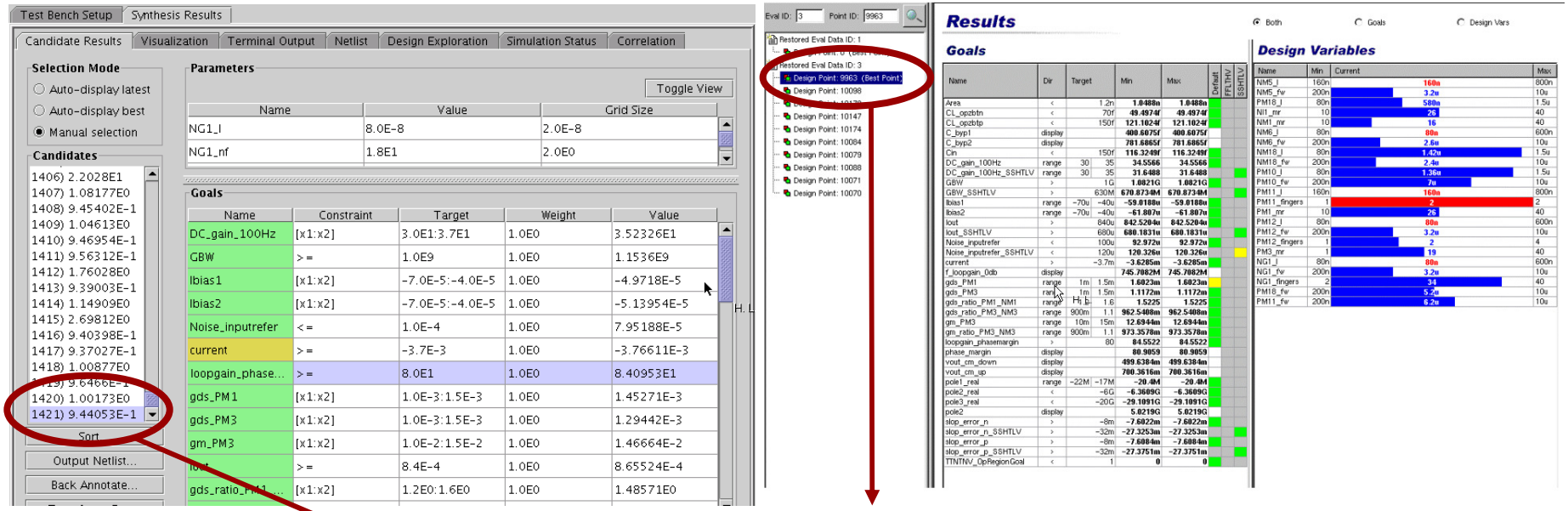
- **Simulation-based tools**
- **Equation-based tools**
  - Faster turn-around
  - Long preparation time/learning curve
  - Not able to optimize large system

- **Arsyn architecture combines**
  - Simulation based: Any simulator
  - Equation based: Automated equation generation
  - Knowledge based.

Feature Comparison with Other Tools

	Competitor	Arsyn
Cadence Interface	Not able to set two blocks	OK
Support CDS CB	OK	OK
BA to CDS	OK	OK
Support Simulators	Spectre	HSPICE/Spectre/others
Support CPS	-	OK
Visualization	-	OK
Characterization	-	OK
Sequencing	-	OK
Hierarchical Opt	-	OK
Sensitivity Analysis	-	OK
LPV	OK	OK
Scripting	-	OK
Parallelism/Dist Comp	OK	OK

Design Candidate Search Capability



1421 iterations

9963 iterations

Arsyn: constantly 10x less iterations than our competitors' in multiple customer design evaluations

Successful Test Cases

Circuit Type	PDK	Process	
Gain-boosted OPAMP	UMC	90nm	√
LVDS – Transmitter	IBM	90nm	√
PLL	IBM	90nm	√
10 bit ADC	TSMC	65nm	√
SerDes-TX	IBM	90nm	√
6 bit DAC	IBM	90nm	√
FC-OPAMP	JAZZ	0.18um	√
Switch Circuit	AMIS	0.35um	√
ADC	MAXIM	0.35um	√

- **Arsyn has been successfully used in the design of various analog circuit types with different foundry PDKs**
- **The practice constantly shows that Arsyn can improve the design quality by 10-20% over the designers while saving significant amount of circuit corner tuning time.**

Summary

- **Arsyn is a useful tool to help circuit designers to**
  - Increase analog/RF designers and custom digital developers productivity
  - Facilitate process migration, circuit topology and testbench re-use
  - Ease design trade-off in complex scenarios
  - Improve yields for sub-90nm technology node and below
- **Compared with other tools, Arsyn has shown**
  - Constant performance advantage
  - Better cadence interface
  - More features to analyze and synthesize circuit
  - More flexible 3 party tool interface (HPSICE/MATLAB/MSIM/NanoSim/Eldo etc)