RORA Design Technologies

Leading Analog Design Automation ™

The Industry-Unique Solution to Complex Mixed-Signal Design Verification

June 2010

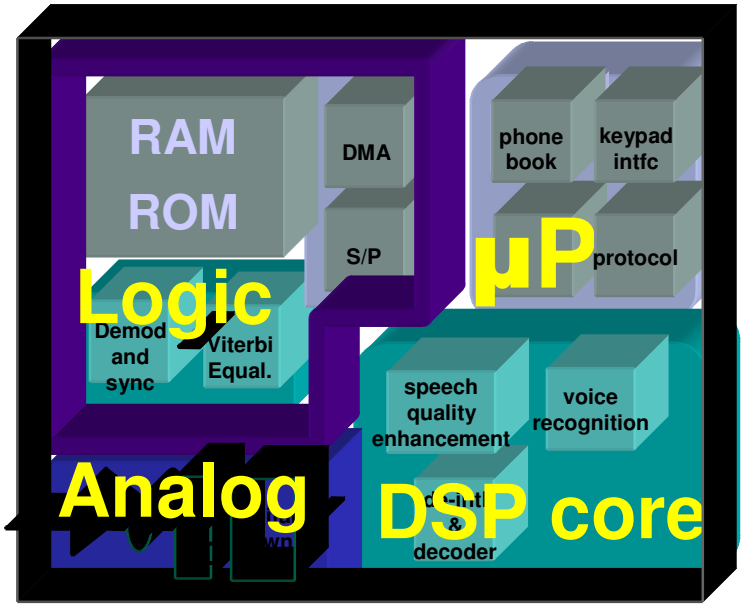
Arana

→ Automated Generation and Grading of Verification Intellectual Properties (VIPs) for Custom ICs

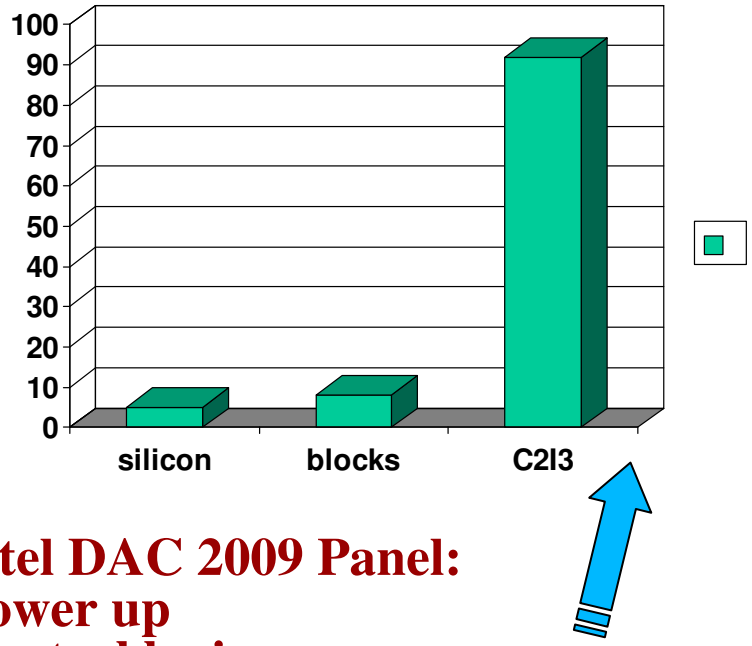
→ Turn Your SPICE into a Superfast SPICE

→ Enable Your Verilog Simulator to Simulate Analog Blocks

Mixed-Signal Verification Challenge



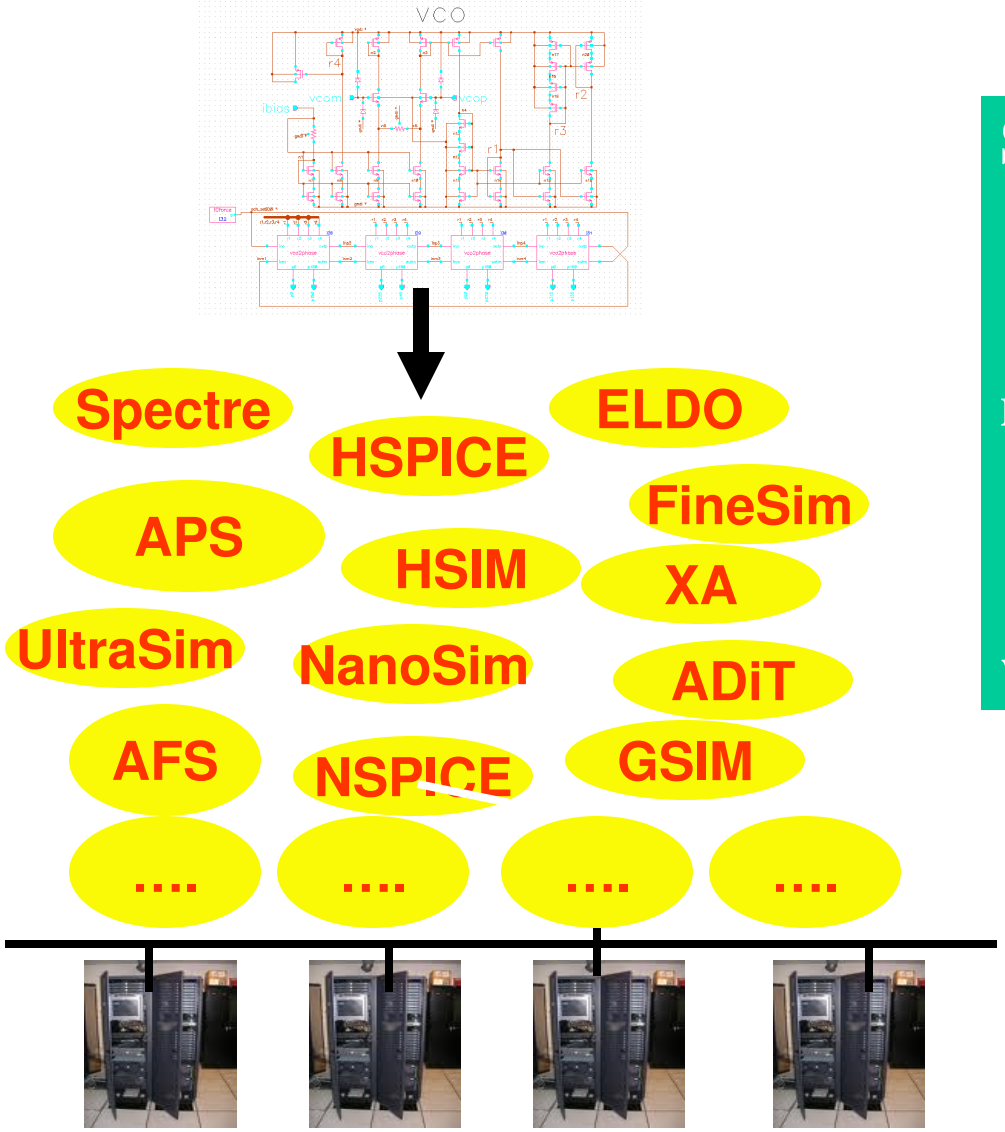
- ➔ Verification Cost Exceeds Design Cost
- ➔ Multiple Silicon Re-spins
- ➔ Delayed Product Roll Out



- ◆ Digital Function Bugs
- ◆ Sensitive Analog
- ◆ Power Management
- ◆ C2I3 errors: Control, Configuration, Interface, Integration, and Interconnect

TI/Intel DAC 2009 Panel:
(1) Power up
(2) Control logic
(3) MSB/LSB switch
(4) Bias wrong

Industry-Standard Practice: Buy Another Fast SPICE/Computer



Still Problems……

➔Still too slow: 10x-20x

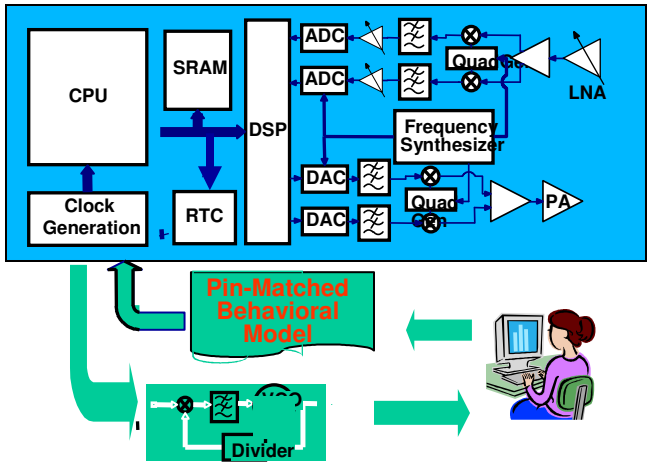
➔Costly: eval & support

➔Inconsistence among models, simulators

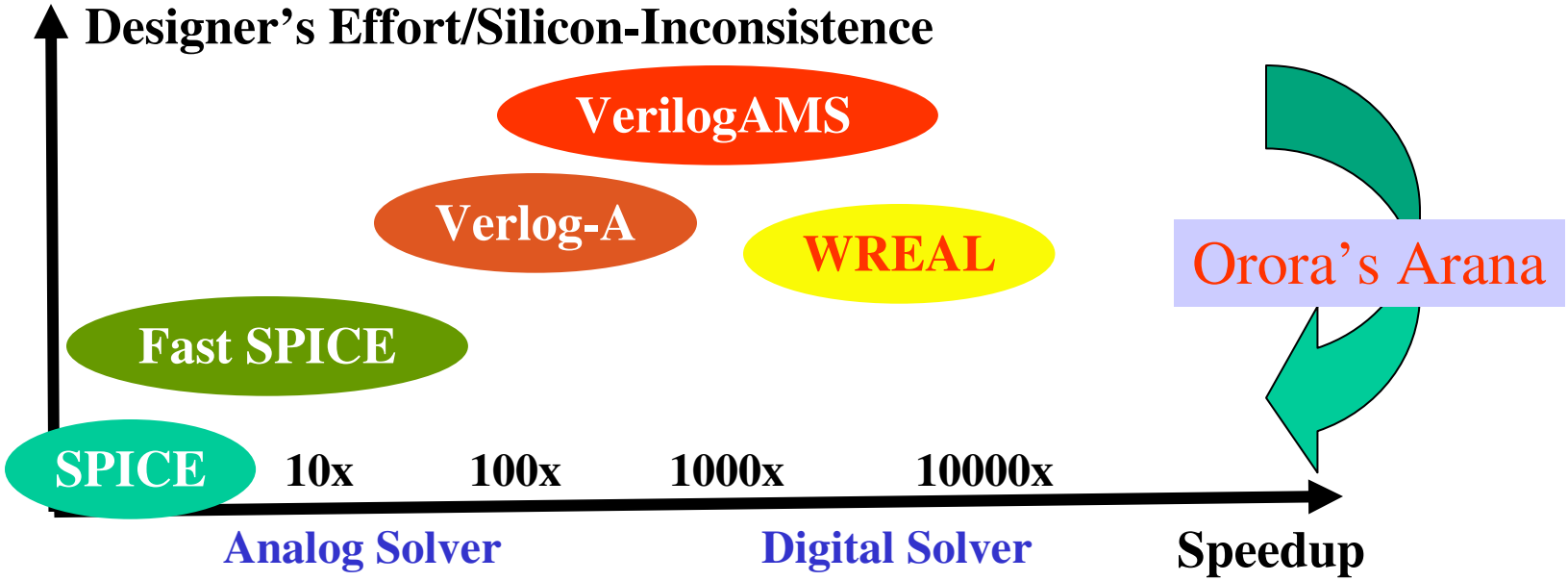
➔Too much data: 100Gb garbage in garbage out

➔How to debug if something wrong

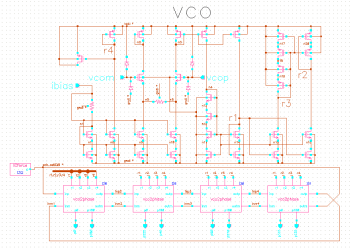
Industry Emerging Solution (Strategic)



- Manual writing models is too tedious, requires expert knowledge on circuits, test benches, systems, languages and simulators
- Inconsistence between silicon and models cause "false" verification



Arana: Automation, Verification-Smart, and Grading



Arana

uVIPs

Your SPICE
Your Verilog Simulator

*Y*our *V*erification *I*ntellectual *P*roperties

- → Silicon faithful and pin matched
- → Verification-Smart:
  - Self debug on C2I3 errors
  - Self-check on circuit operations
- → Efficiency: 100x-1000x faster
- → Compact: 100x-1000x less details (data)

- → Optimized simulatable/non-readabe form
  - * Avoid errors caused by human intervention
  - * Protect your intellectual property
  - * Maximal speed up

Accurate but with less details

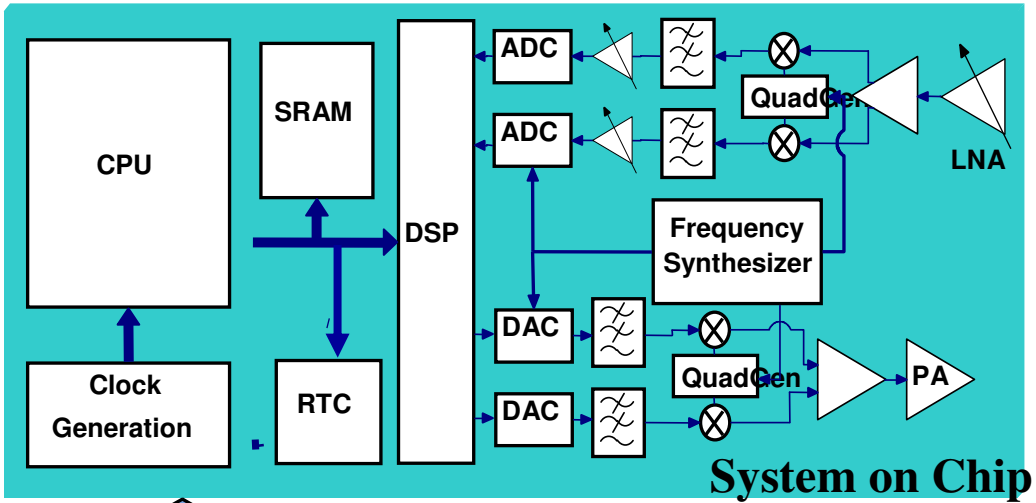
- → Point-matched SPICE: too much detail
- → Arana: abstract out un-wanted details

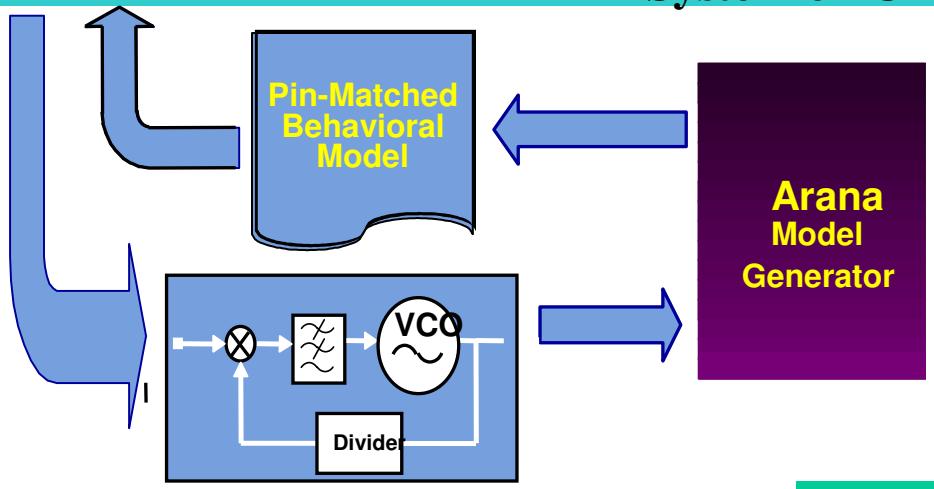
Automated uVIP Scoreboarding by Arana

	view1 (model1)	View2 (model 2)	view3 (model 3)	View4 (mode 4)
Power-aware	√	√	X	X
Load-aware	√	√	√	√
PVT-aware	√	√	X	X
Noise-aware	X	X	X	X
Interface assertion	√	√	√	X
Self checking	√	X	√	X
Spectre/HSPICE	√	√	√	X
IES(WREAL)	X	X	X	√
Speed				
Accuracy				
IOut				
Trise/Tfall				

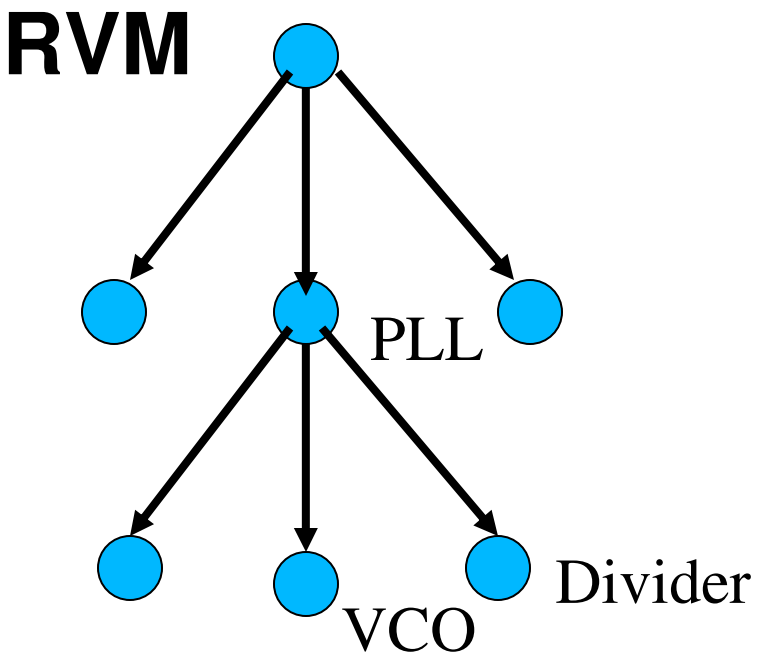
Confidence in models; Enable metric-driven mixed-signal verification

The RVM (Recursively Verifying and Modeling) Methodology





Benefits: Same Flow
Same Simulator/Same Test Bench



Automated bottom-up process
No need for templates

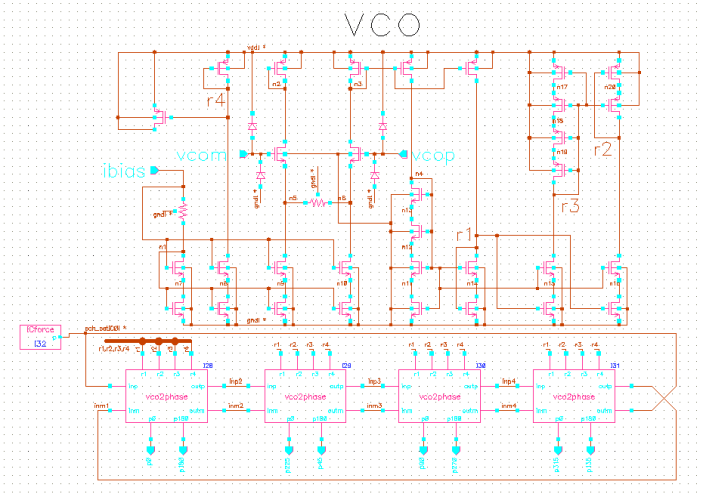
➔ **Enable sign off early in the design phase**
➔ **Enable incremental sign off**

Behavioral Models with “Analog Assertions”

```
`include "discipline.h"
`include "constants.h"


module OPAMP_TOP30(
AVD,AVS,CRS,DIESID,OFSCIRD,OPINL,OPINU,OPOUTL,OPOUTU,SIR,VGN1,VGN2,VGP1,VGP2,VGSN1,VGSP1,XDIESID,
input AVD,AVS,VGN1,VGN2,VGP1,VGP2,VGSN1,VGSP1,inh_inh_sub,CRS,DIESID,XDIESID,OFSCIRD,SIR,XEN;
inout OPINL,OPINU,OPOUTL,OPOUTU;
electrical
AVD,AVS,CRS,DIESID,OFSCIRD,OPINL,OPINU,OPOUTL,OPOUTU,SIR,VGN1,VGN2,VGP1,VGP2,VGSN1,VGSP1,XDIESID,

real DCSHIFT_c_0_OPINL
```



Differential pins

```
if( abs( V(DTESTD)+V(XDTESTD) - 15) > coef_diff*15 ) begin
    $strobe("Differential Pair DTESTD and XDTESTD are not in
differential mode.");
    $finish;
   end
```

Wrong bias

```
  if ( (V(AVD) > 16.500000) || (V(AVD) < -1.500000) ) begin
    $strobe("WARNING:Vsource Port AVD is out of boundary.
Result may not be correct. \n ");
  end
```

Automated inserted analog assertions will detect integration errors in run time!!!

Arana Unique Value Proposition

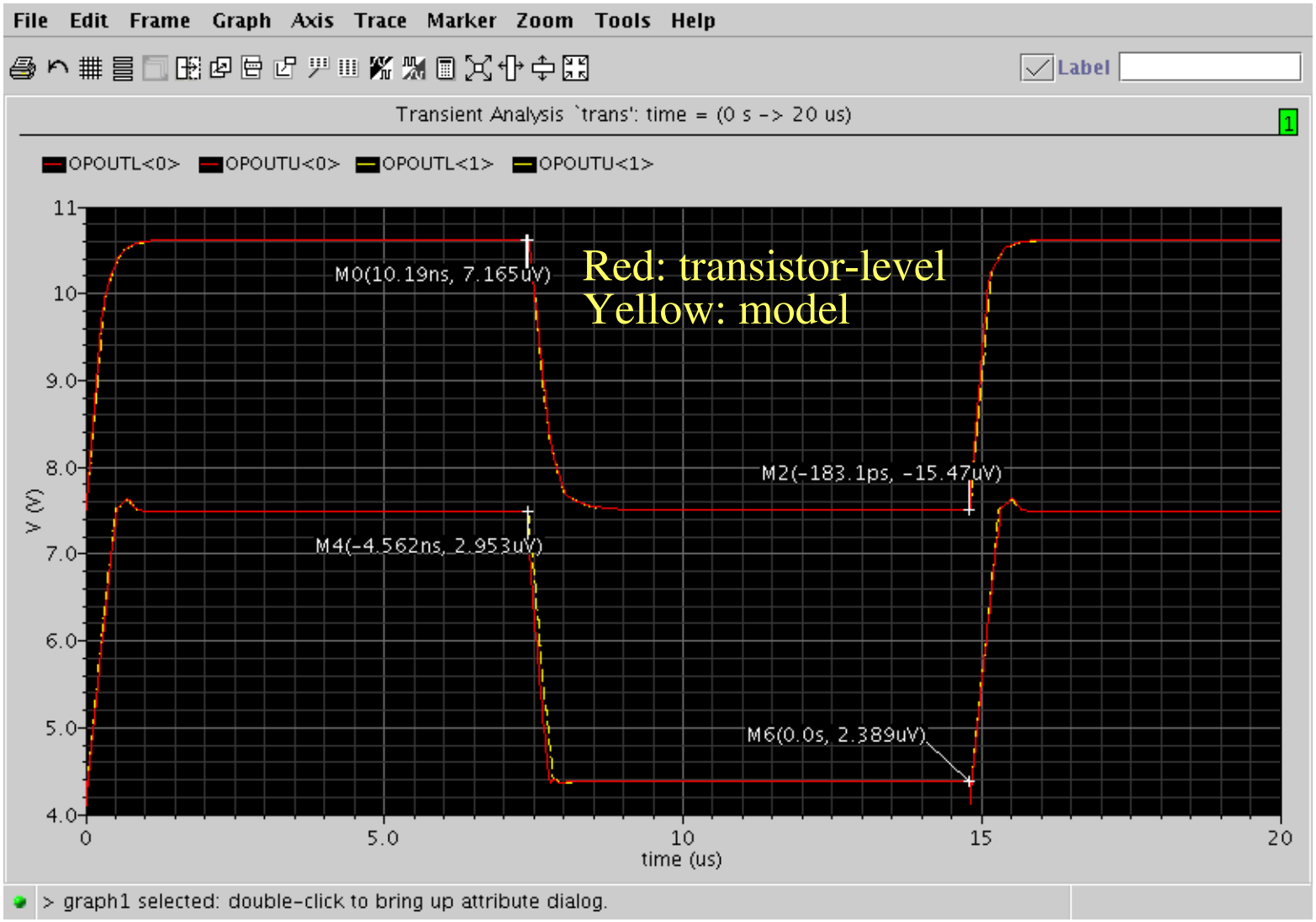
- **Enabler for Mixed-Signal SoC Functional Verification**
  - Most re-spins due to “simple/stupid” errors.
  - Analog simulation slows down everything
  - Can be100x-1000x speed up over SPICE
  - Automated bottom-up/automated process
    - **Silicon-faithful: pin-matched to pre-layout/post-layout netlists**
    - **Fundamentally resolve the inconsistence between behavioral models vs designs**
    - **Capture all control and configuration models**
    - **Capture Process-Voltage-Temperature variations**
  - Hierarchical (Fast SPICE does not cut)
    - **Mix and match behavioral models and netlsits**
    - **Fast**
    - **Small set of data to enable debugging**

Arana Industry Benchmark Results*

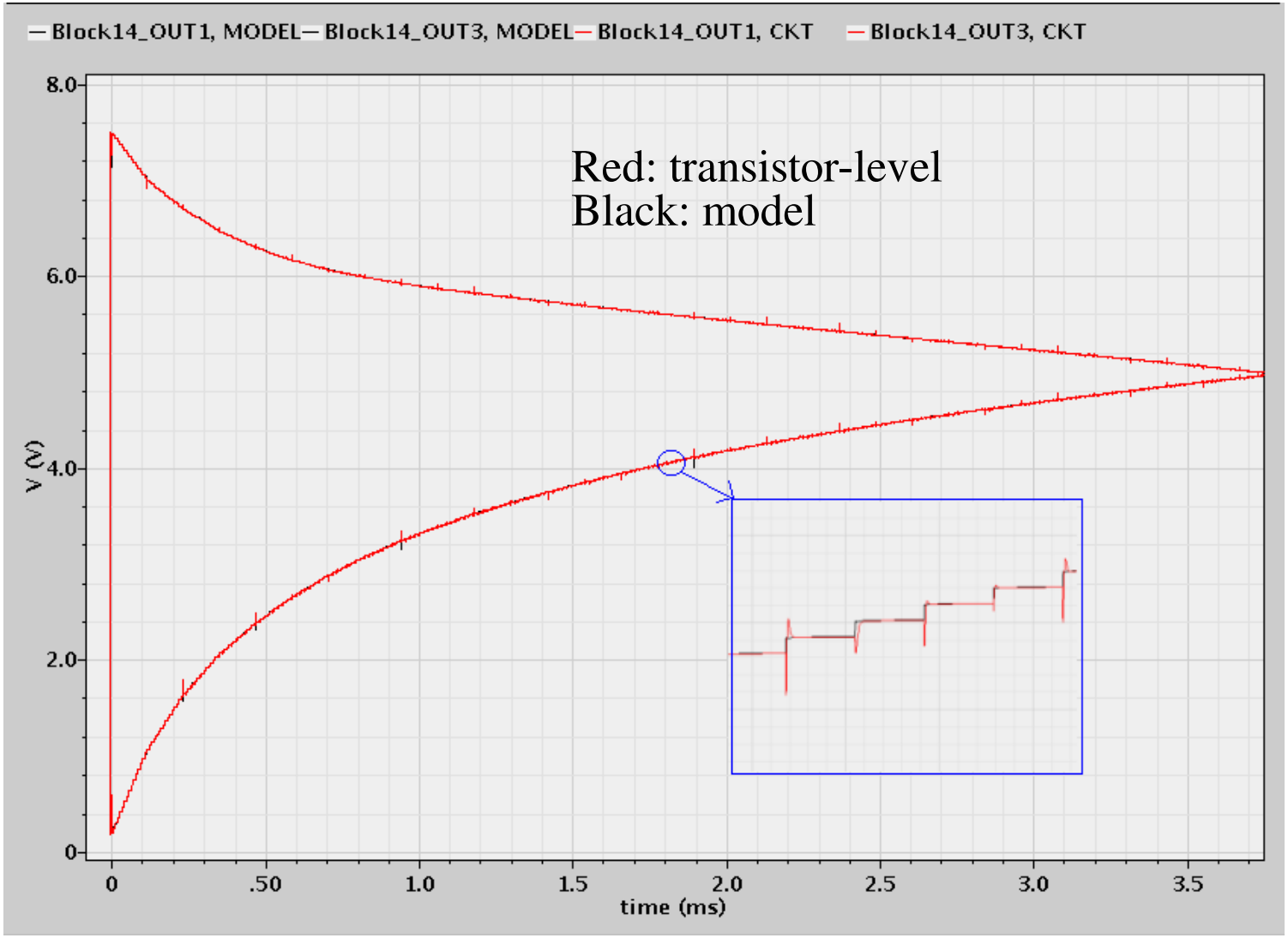
Circuits	Foundry Process	# transistors	Transistor-Level Simulation time	Model-Substituted Simulation Time	Speed Up	Accuracy Loss**
XAUI SerDes	IBM 90nm	15,000	>15 days	15 min (100 kbits)	1200X	5%
4-CH 10-bit Source Driver	Sony 16V 2u CMOS	6,000	>3 days	17 min	250X	0.1%
DC-DC Converter	Sony TFT	180	39 min	2 min	20X	0.3%
5^{th}-order Switched-Capacitor Filter	STARC 90nm	371	8 hr 45 m	(second-level) 154 sec	204	<0.6%
				(top-level) 12.7 sec	2480	<10%
8bit ΔΣ ADC	TSMC 90nm	--	1.8 hr	23 sec	250X	6%
Custom MCU	TSMC 90nm	12,000	12.3 hr	90 sec	500X	10%
PLL	Samsung 65nm	2109	11 hr 11 min	3 min 44 sec	180X	1%
High-Speed Comparator	IBM 90nm	780	1.5 hr	82 sec	100X	3%
10-bit DAC	DBH 0.13um	19465	1 day 10 hr 4 min	(second-level) 17 min 18 sec	120X	1.62%
				(top-level) 3 min	680X	0.5 %

*Cadence Spectre Simulator (Verilog-A behavioral models) **design specs

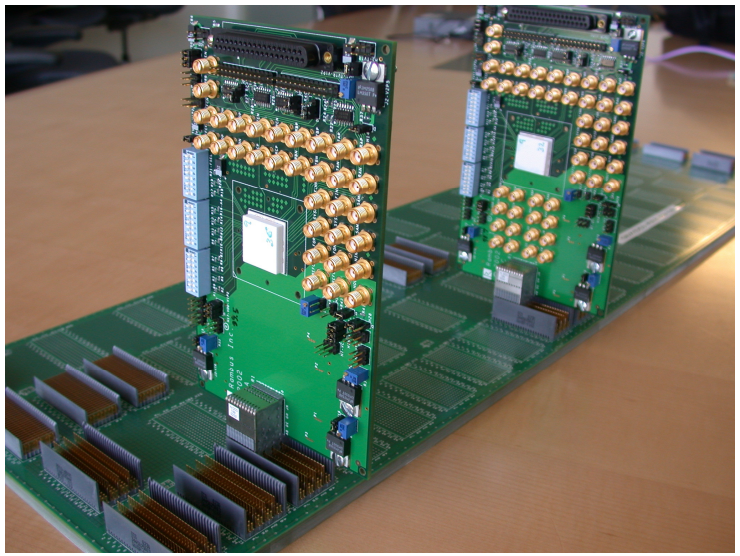
4-Channel 10-Bit Source Driver – Waveform Single Step



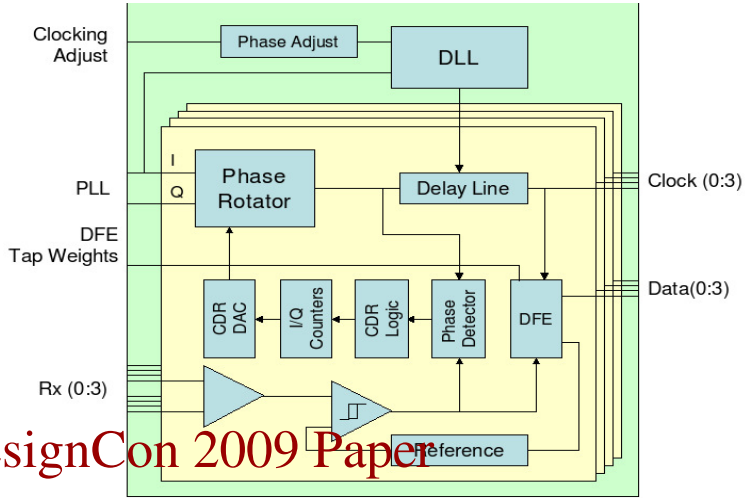
4-Channel 10-Bit Source Driver – Waveform Staircase



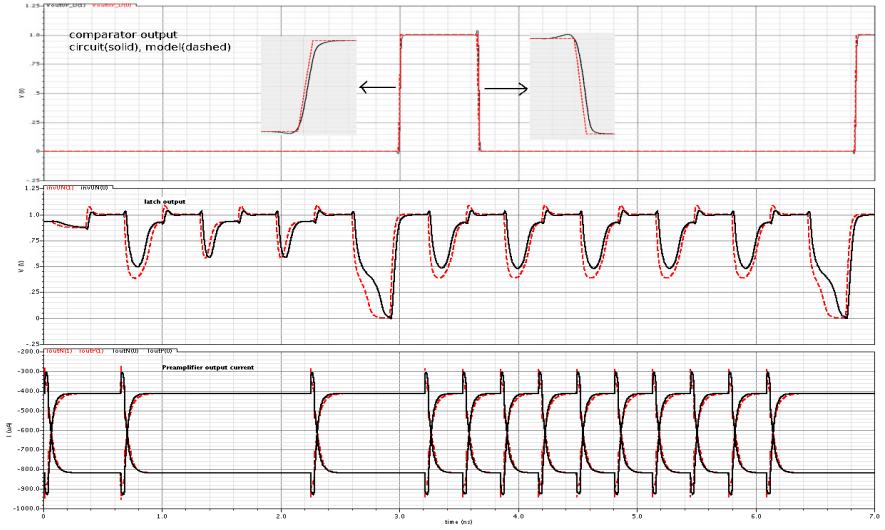
Boeing SerDes Design



Data communication link



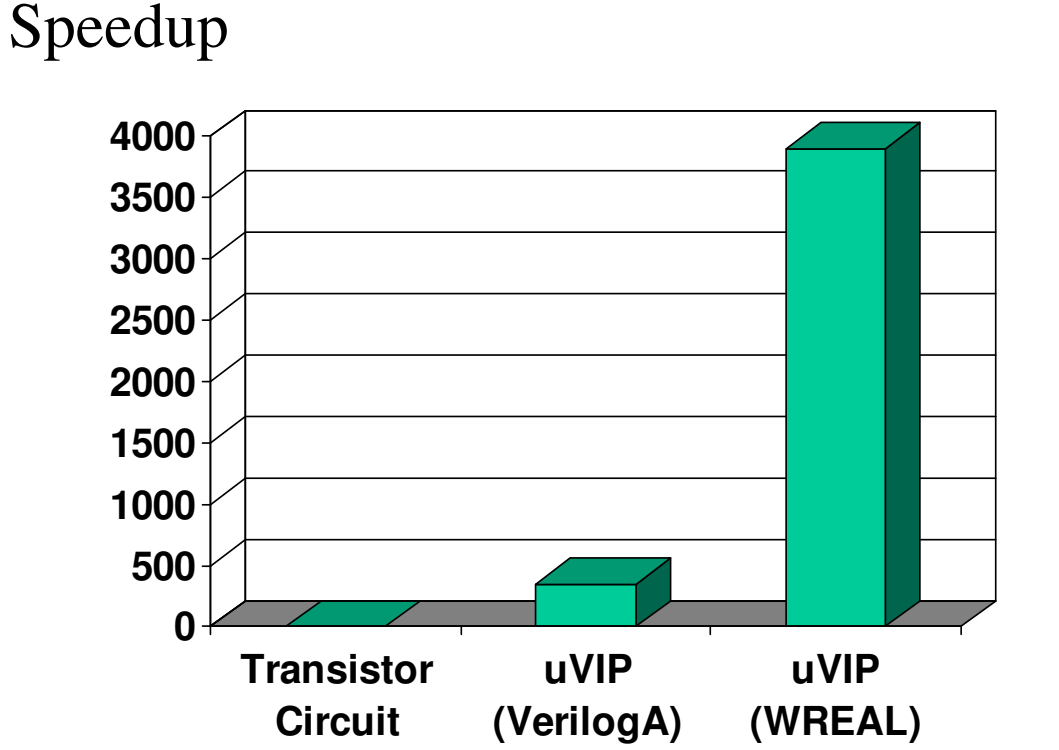
DesignCon 2009 Paper



Block	Silicon-Calibrated Spec-Driven Behavioral Model		Netlist-Driven Behavioral Model	
	Modeling error	Speedup	Modeling error	Speedup
VGA	Gain@DC: 0% Gain@full rate: 0%	25X	Gain@DC: 1.4% Gain@full rate: 4.7%	48X
Comparator	Delay time: 4% Rise/fall time: 3%	70X	Delay time: 4.1% Rise/fall time: 2.1%	10X
Phase Rotator	Phase shift: 4%	1260X	*Same Model*	
Tx Bias Generator	Settling time (90%): 2% Settling time (99%): 13% Final value: 0%	17X	Final value: 0.14%	31X
Tx DAC	Settling time (90%): 1% Settling time (99%): 5% DAC step: 0%	300X	Final value: 0.05%	42X
Tx output driver	Voltage level: 4%	6000X	Voltage level: 0.78%	100X
Rx top level	5%	2200X	5%	1200X
Tx top level	5%	500X	5%	120X

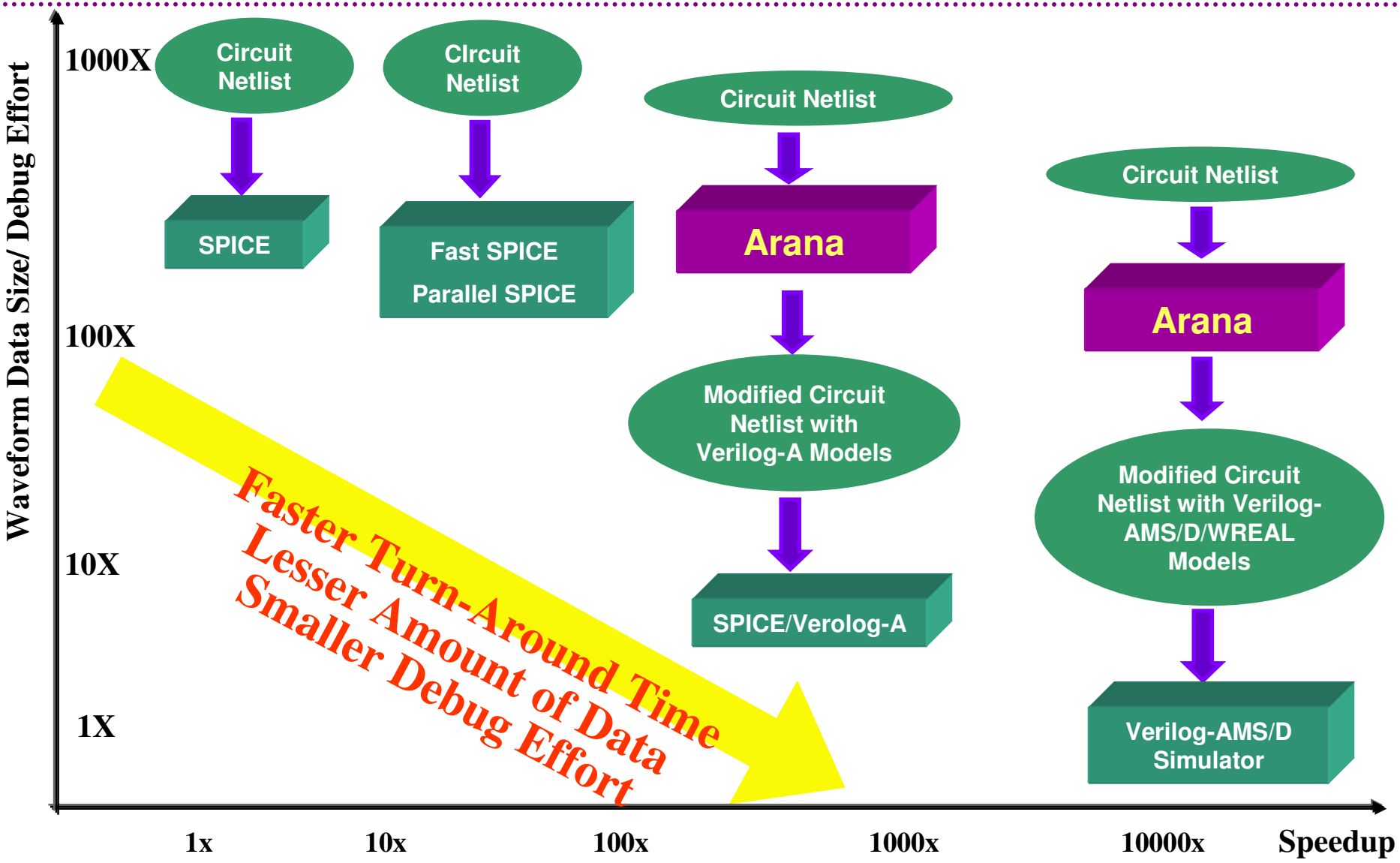
IBM 90nm PLL uVIP Results

Waveform Accuracy Picture here



(14 hours) **(2 mins 23 secs)** **(13 secs)**

Summary of Arana-Enabled Mixed-Signal Verification



Arana Road Map

Arana 4.5		**Q3, 2010**			
noise-aware					
Arana 4.6			**Q4 2010**		
post-layout hierarchical view					
Arana 4.7				**Q1 2011**	
time-domain noise modeling					
Arana 4.8					**Q2 2011**
post-layout flattern view					

Summary

- **Arana is industry-first designers' behavioral modeling platform for mixed-signal blocks**
  - Generation of verification IPs for custom design
- **Has been validated against 50+ benchmark circuits from 20+ customers**
  - DAC, ADC, PLL, SerDes, DC-DC Converter, …
- **Arana-enabled mixed-signal full-chip functional verification flow**
  - **Same simulator, same test bench (no need to change the flow)**
  - **100x-1000x faster for complex blocks**
  - **Analog assertion automated: compatible with digital verification flow**
  - **Delegate the time-consuming verification task to circuit designers**