The Industry-Unique Solution to Complex Mixed-Signal Design Verification

June 2010

Arana

- Automated Generation and Grading of Verification Intellectual Properties (VIPs) for Custom ICs
- Turn Your SPICE into a Superfast SPICE
- Enable Your Verilog Simulator to Simulate Analog Blocks
Mixed-Signal Verification Challenge

- Verification Cost Exceeds Design Cost
- Multiple Silicon Re-spins
- Delayed Product Roll Out

- Digital Function Bugs
- Sensitive Analog
- Power Management
- C2I3 errors: Control, Configuration, Interface, Integration, and Interconnect

TI/Intel DAC 2009 Panel:
1. Power up
2. Control logic
3. MSB/LSB switch
4. Bias wrong
Still Problems……
- Still too slow: 10x-20x
- Costly: eval & support
- Inconsistency among models, simulators
- Too much data: 100Gb
  garbage in garbage out
- How to debug if something wrong
Industry Emerging Solution (Strategic)

- Manual writing models is too tedious, requires expert knowledge on circuits, test benches, systems, languages and simulators
- Inconsistence between silicon and models cause “false” verification

Designer’s Effort/Silicon-Inconsistence

Fast SPICE

SPICE

10x

100x

1000x

10000x

Analog Solver

Digital Solver

Speedup

Orora’s Arana

VerilogAMS

Verilog-A

WREAL
**Arana: Automation, Verification-Smart, and Grading**

**Your Verification Intellectual Properties**
- Silicon faithful and pin matched
- Verification-Smart:
  - Self debug on C2I3 errors
  - Self-check on circuit operations
- Efficiency: 100x-1000x faster
- Compact: 100x-1000x less details (data)

- Optimized simulatable/non-readable form
  - Avoid errors caused by human intervention
  - Protect your intellectual property
  - Maximal speed up

**Accurate but with less details**
- Point-matched SPICE: too much detail
- Arana: abstract out un-wanted details
## Automated uVIP Scoreboarding by Arana

<table>
<thead>
<tr>
<th>Feature</th>
<th>view1 (model1)</th>
<th>View2 (model 2)</th>
<th>view3 (model 3)</th>
<th>View4 (mode 4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-aware</td>
<td>√</td>
<td>√</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>Load-aware</td>
<td>√</td>
<td>√</td>
<td>√</td>
<td>√</td>
</tr>
<tr>
<td>PVT-aware</td>
<td>√</td>
<td>√</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>Noise-aware</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>Interface assertion</td>
<td>√</td>
<td>√</td>
<td>√</td>
<td>×</td>
</tr>
<tr>
<td>Self checking</td>
<td>√</td>
<td>×</td>
<td>√</td>
<td>×</td>
</tr>
<tr>
<td>Spectre/HSPICE</td>
<td>√</td>
<td>√</td>
<td>√</td>
<td>×</td>
</tr>
<tr>
<td>IES(WREAL)</td>
<td>×</td>
<td>×</td>
<td>×</td>
<td>×</td>
</tr>
<tr>
<td>Speed</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Accuracy</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>IOut</td>
<td></td>
<td></td>
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<tr>
<td>Trise/Tfall</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

Confidence in models; Enable metric-driven mixed-signal verification
The RVM (Recursively Verifying and Modeling) Methodology

Benefits: Same Flow
Same Simulator/Same Test Bench

- Enable sign off early in the design phase
- Enable incremental sign off

Automated bottom-up process
No need for templates
Behavioral Models with “Analog Assertions”

```
`include "discipline.h"
`include "constants.h"

module OPAMP_TOP30(
    AVD, AVS, CRS, DTESTD, OFSCTRD, OPINL, OPINU, OPOUTL, OPOUTU, STR, VGN1, VGN2, VGP1, VGP2, VGSP1, VGSN1, XDTESTD, XEN, inh_inh_sub);

    input AVD, AVS, VGN1, VGN2, VGP1, VGP2, VGSP1, VGSN1, XDTESTD, XEN, inh_inh_sub;
    inout OPINL, OPINU, OPOUTL, OPOUTU;

real DCSHIFT_c_0_OPINL

if( abs( V(DTESTD)+V(XDTESTD) - 15) > coef_diff*15 ) begin
    $strobe("Differential Pair DTESTD and XDTESTD are not in differential mode.");
    $finish;
end

if ( (V(AVD) > 16.500000) || (V(AVD) < -1.500000) ) begin
    $strobe("WARNING:Vsource Port AVD is out of boundary. Result may not be correct.
    
end

Automated inserted analog assertions will detect integration errors in run time!!!
```
Arana Unique Value Proposition

- Enabler for Mixed-Signal SoC Functional Verification
  - Most re-spins due to “simple/stupid” errors.
  - Analog simulation slows down everything
  - Can be 100x-1000x speed up over SPICE
  - Automated bottom-up/automated process
    - Silicon-faithful: pin-matched to pre-layout/post-layout netlists
    - Fundamentally resolve the inconsistency between behavioral models vs designs
    - Capture all control and configuration models
    - Capture Process-Voltage-Temperature variations
  - Hierarchical (Fast SPICE does not cut)
    - Mix and match behavioral models and netlists
    - Fast
    - Small set of data to enable debugging
<table>
<thead>
<tr>
<th>Circuits</th>
<th>Foundry Process</th>
<th># transistor s</th>
<th>Transistor-Level Simulation time</th>
<th>Model-Substituted Simulation Time</th>
<th>Speed Up</th>
<th>Accuracy Loss**</th>
</tr>
</thead>
<tbody>
<tr>
<td>XAUI SerDes</td>
<td>IBM 90nm</td>
<td>15,000</td>
<td>&gt;15 days</td>
<td>15 min (100 kbits)</td>
<td>1200X</td>
<td>5%</td>
</tr>
<tr>
<td>4-CH 10-bit Source Driver</td>
<td>Sony 16V 2u CMOS</td>
<td>6,000</td>
<td>&gt;3 days</td>
<td>17 min</td>
<td>250X</td>
<td>0.1%</td>
</tr>
<tr>
<td>DC-DC Converter</td>
<td>Sony TFT</td>
<td>180</td>
<td>39 min</td>
<td>2 min</td>
<td>20X</td>
<td>0.3%</td>
</tr>
<tr>
<td>5th-order Switched-Capacitor Filter</td>
<td>STARC 90nm</td>
<td>371</td>
<td>8 hr 45 m</td>
<td>(second-level) 154 sec</td>
<td>204</td>
<td>&lt;0.6%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(top-level) 12.7 sec</td>
<td>2480</td>
<td>&lt;10%</td>
</tr>
<tr>
<td>8bit ∆Σ ADC</td>
<td>TSMC 90nm</td>
<td>--</td>
<td>1.8 hr</td>
<td>23 sec</td>
<td>250X</td>
<td>6%</td>
</tr>
<tr>
<td>Custom MCU</td>
<td>TSMC 90nm</td>
<td>12,000</td>
<td>12.3 hr</td>
<td>90 sec</td>
<td>500X</td>
<td>10%</td>
</tr>
<tr>
<td>PLL</td>
<td>Samsung 65nm</td>
<td>2109</td>
<td>11 hr 11 min</td>
<td>3 min 44 sec</td>
<td>180X</td>
<td>1%</td>
</tr>
<tr>
<td>High-Speed Comparator</td>
<td>IBM 90nm</td>
<td>780</td>
<td>1.5 hr</td>
<td>82 sec</td>
<td>100X</td>
<td>3%</td>
</tr>
<tr>
<td>10-bit DAC</td>
<td>DBH 0.13um</td>
<td>19465</td>
<td>1 day 10 hr 4 min</td>
<td>(second-level) 17 min 18 sec</td>
<td>120X</td>
<td>1.62%</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(top-level) 3 min</td>
<td>680X</td>
<td>0.5%</td>
</tr>
</tbody>
</table>

* Cadence Spectre Simulator (Verilog-A behavioral models)

** Design specs
4-Channel 10-Bit Source Driver – Waveform Single Step

Transient Analysis `trans`: time = (0 s -> 20 us)

- Red: transistor-level
- Yellow: model

MO(10.19ns, 7.185V)
M2(-183.1ps, -15.47V)
M4(-4.562ns, 2.953V)
M6(0.0s, 2.389V)

> graph1 selected: double-click to bring up attribute dialog.
4-Channel 10-Bit Source Driver – Waveform Staircase

Red: transistor-level
Black: model
Boeing SerDes Design

Data communication link

<table>
<thead>
<tr>
<th>Block</th>
<th>Silicon-Calibrated Spec-Driven Behavioral Model</th>
<th>Netlist-Driven Behavioral Model</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Modeling error</td>
<td>Speedup</td>
</tr>
<tr>
<td>VGA</td>
<td>Gain@DC: 0%</td>
<td>25X</td>
</tr>
<tr>
<td></td>
<td>Gain@full rate: 0%</td>
<td></td>
</tr>
<tr>
<td>Comparator</td>
<td>Delay time: 4%</td>
<td>70X</td>
</tr>
<tr>
<td></td>
<td>Rise/fall time: 3%</td>
<td></td>
</tr>
<tr>
<td>Phase Rotator</td>
<td>Phase shift: 4%</td>
<td>1260X</td>
</tr>
<tr>
<td>Tx Bias Generator</td>
<td>Settling time (90%): 2%</td>
<td>17X</td>
</tr>
<tr>
<td></td>
<td>Settling time (99%): 13%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Final value: 0%</td>
<td></td>
</tr>
<tr>
<td>Tx DAC</td>
<td>Settling time (90%): 1%</td>
<td>300X</td>
</tr>
<tr>
<td></td>
<td>Settling time (99%): 5%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DAC step: 0%</td>
<td></td>
</tr>
<tr>
<td>Tx output driver</td>
<td>Voltage level: 4%</td>
<td>6000X</td>
</tr>
<tr>
<td>Rx top level</td>
<td>5%</td>
<td>2300X</td>
</tr>
<tr>
<td>Tx top level</td>
<td>5%</td>
<td>500X</td>
</tr>
</tbody>
</table>
IBM 90nm PLL uVIP Results

<table>
<thead>
<tr>
<th></th>
<th>Transistor Circuit</th>
<th>uVIP (VerilogA)</th>
<th>uVIP (WREAL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Speedup</td>
<td>0</td>
<td>(14 hours)</td>
<td>(2 mins 23 secs)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(13 secs)</td>
</tr>
</tbody>
</table>

Waveform Accuracy Picture here
Summary of Arana-Enabled Mixed-Signal Verification

- **SPICE**
  - Circuit Netlist
  - Fast SPICE
  - Parallel SPICE
- **Arana**
  - Modified Circuit Netlist with Verilog-A Models
  - Modified Circuit Netlist with Verilog-AMS/D/WREAL Models
- **SPICE/Verilog-A**
  - Faster Turn-Around Time
  - Lesser Amount of Data
  - Smaller Debug Effort

**Orora Design Technologies, Inc.**

Leading Analog Design Automation

Orora Proprietary and Confidential
## Arana Road Map

<table>
<thead>
<tr>
<th>Arana 4.5</th>
<th>Q3, 2010</th>
</tr>
</thead>
<tbody>
<tr>
<td>noise-aware</td>
<td></td>
</tr>
<tr>
<td>Arana 4.6</td>
<td>Q4 2010</td>
</tr>
<tr>
<td>post-layout hierarchical view</td>
<td></td>
</tr>
<tr>
<td>Arana 4.7</td>
<td>Q1 2011</td>
</tr>
<tr>
<td>time-domain noise modeling</td>
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</tr>
<tr>
<td>Arana 4.8</td>
<td>Q2 2011</td>
</tr>
<tr>
<td>post-layout flattern view</td>
<td></td>
</tr>
</tbody>
</table>
Summary

- Arana is industry-first designers’ behavioral modeling platform for mixed-signal blocks
  - Generation of verification IPs for custom design
- Has been validated against 50+ benchmark circuits from 20+ customers
  - DAC, ADC, PLL, SerDes, DC-DC Converter, …
- Arana-enabled mixed-signal full-chip functional verification flow
  - Same simulator, same test bench (no need to change the flow)
  - 100x-1000x faster for complex blocks
  - Analog assertion automated: compatible with digital verification flow
  - Delegate the time-consuming verification task to circuit designers